PCIe-7396

96-Channel Digital I/O Card

User's Manual



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Revision History

Revision	Release Date	Description of Change(s)
1.0	2021-02-02	Initial release.

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Preface

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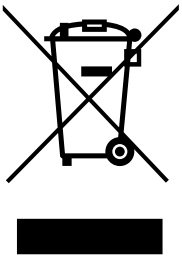
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Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE:

Additional information, aids, and tips that help users perform tasks.

CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.
ATTENTION: Informations destinées à prévenir les blessures corporelles mineures, les dommages aux composants, la perte de données et/ou la corruption de programme lors de l'exécution d'une tâche.

WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.
AVERTISSEMENT: Informations destinées à prévenir les blessures corporelles graves, les dommages aux composants, la perte de données et/ou la corruption de programme lors de l'exécution d'une tâche spécifique.

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1 Introduction

The PCIe-7396 is a 96-bit parallel digital input/output (DIO) card designed for industrial applications. The plug and play feature of PCI Express Bus architecture makes it easy for users to install the PCIe-7396 on their systems quickly.

The PCIe-7396 emulates two/four 8255 Programmable Peripheral Interface (PPI) chips. Each PPI offers three 8-bit DIO ports which can be accessed simultaneously. The total 6/12 ports can be programmed as input or output independently.

The PCIe-7396 supports external triggering to capture digital input data. The “Change of State” (COS) interrupt is provided so that when any digital input changes its state, an interrupt will be generated for the user to handle the external event.

1.1 Features

The PCIe-7396 Digital I/O board provides the following advanced features:

- Digital I/O ports
  - 96 TTL compatible digital I/O lines
  - SCSI-type 100-pin connector (AMP-787082-9)
  - 48mA high current driving capability per channel
  - Output status read-back
  - Supports external trigger to capture digital input data
- Timer, counter and interrupt system
  - Programmable 32-bit timer to generate timer interrupt
  - Programmable 16-bit event counter to generate event interrupt
  - 96-bit change of state (COS) interrupt
  - Dual interrupt system

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1.2 Applications

- Programmable mixed digital input and output
- Industrial monitoring and control
- LED indicator control
- Parallel data transfer
- TTL, DTL, and CMOS logic sensing

1.3 Specifications

Item	Specification
I/O channels	96-bit
Input Signal	Logic High Voltage: 2.0V to 5.25V Logic Low Voltage: 0.0V to 0.08V Logic High Current: 0.1 µA Logic Low Current: -8 mA
Output Signal	Logic High Voltage: Typical 5V, 2.4V min. Logic Low Voltage: 0.5V max. Logic High Current: -15.0 mA Logic Low Current: 48.0 mA
Operating Temperature	0˚C to 60˚C
Storage Temperature	-20˚C to 80˚C
Humidity	5% to 95% non-condensing
I/O Connector	100-pin SCSI connector
Bus	PCI Express x1
IRQ Level	Set by BIOS
I/O port address	Set by BIOS
Power Consumption	450mA (with no external devices)
Transfer Rate	1M bytes/sec (typical)
Dimensions	138.96 mm x 98.4 mm

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1.4 Software Support

ADLINK provides versatile software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW. ADLINK Measurement, Automation & Platform Service (MAPS) is a software service package designed for data acquisition, automation and PXI platforms.

By leveraging low-level kernel management and a user friendly API, users can easily manage devices under a Windows environment and focus on developing applications.

1.4.1 ADLINK MAPS Core

ADLINK MAPS Core is a software package that includes all the device drivers for Windows and ADLINK Connection Explorer (ACE), a system level management tool. With MAPS Core installed, the operating system can identify ADLINK devices correctly and assign the necessary resources for low-level access, such as IO read/write or direct memory access. MAPS/Core is necessary for all ADLINK DAQ modules. To ensure the user has the latest software, go to the ADLINK product webpage or contact ADLINK technical service.

Through ACE, users can discover and manage ADLINK DAQ modules to, for example, reserve a certain size of memory buffer for DMA operation or set the user alias name for operating the module in a LabVIEW environment.

ACE also provides a ready-to-use soft-front panel for digitizer products. By clicking the Launch button in the lowest utility block, this soft-front panel allows users to control digitizers through the UI and display the acquired waveform/data on the screen.

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1.4.2 ADLINK MAPS/LV, LabVIEW Support

For customers who develop their own programs in LabVIEW, the MAPS/LV software package must be installed. MAPS/LV, also called DAQ-LabVIEW Plus, includes the software library and sample program for LabVIEW. Download and install the latest MAPS/LV software and refer to the MAPS/LV manual for more information.

1.4.3 MAPS/C, C & C++ Support

For users who develop their own programs in C or C++ environments, the MAPS/C software package must be installed. MAPS/C includes all the software components required for developing applications in C/C++, such as header files, a device API library and versatile sample programs for understanding how to manipulate the device correctly. Find the latest version of MAPS/C on the ADLINK website.

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2 Getting Started



Diagrams and images of equipment are for reference only.

2.1 Package Contents

- PCIe-7396 96-bit Parallel Digital I/O Card
- Product Warranty Card



If any of the items in the contents list are missing or damaged, contact your ADLINK dealer.

2.2 Unpacking

The PCIe-7396 card contains sensitive electronic components that can be easily damaged by static electricity.

The card should be unpacked on a grounded anti-static mat while wearing a grounded anti-static wristband.

Inspect the card module carton for obvious damage, as shipping and handling may cause damage to the module. Be sure the module is not damaged before proceeding.



Do not apply power to the PCIE-7396 if it has been damaged.

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2.3 Board Layout

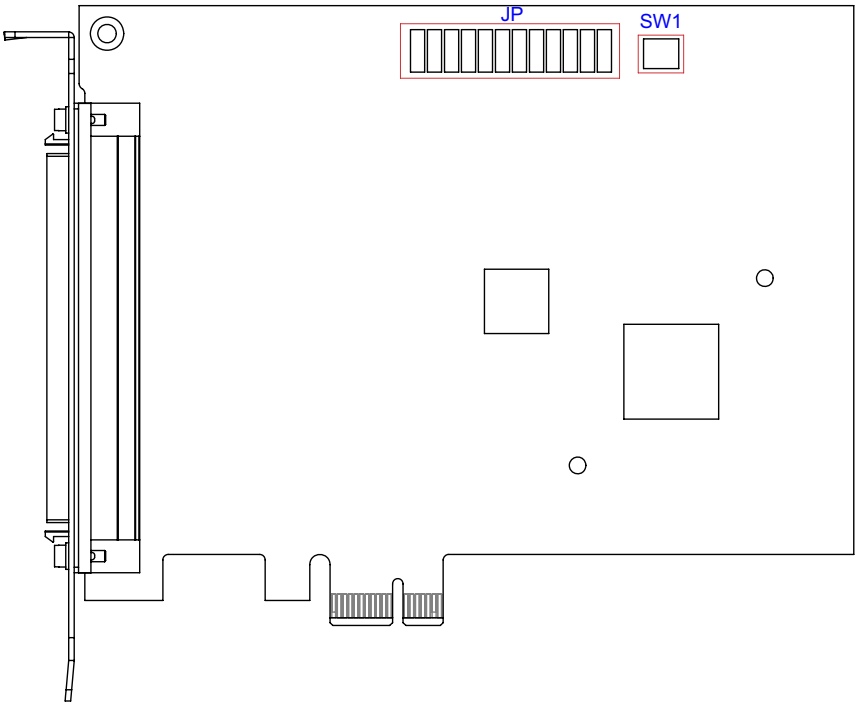


Figure 2-1: Board Layout

Item	Description
JP	Power-On State Selection Jumper
SW1	Card ID Selection Switch (Reserved)

Table 2-1: Board Features Legend

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2.4 Installation

2.4.1 Hardware Configuration

PCI Express cards are equipped with a plug and play PCI Express controller that can request base addresses and interrupts according to PCI Express standard. The system BIOS will configure resource based on the PCI Express cards' configuration registers and system parameters (set in the BIOS). Interrupt assignment and memory usage (I/O port locations) of the PCI Express cards can be assigned by the system BIOS only. These system resource assignments are done on a board-by-board basis. It is not suggested to assign the system resource by any other method.

2.4.2 PCI Express Slot Selection

The PCIe-7396 can be inserted into any PCI Express slot without the need to configure system resources.

2.4.3 Installation Procedures

1. Turn off the computer.
2. Turn off all peripheral devices connected to the computer.
3. Remove the cover from the computer.
4. Setup jumpers on the PCIe-7396. (See "Jumpers" on page 10.)
5. Select any available PCI Express x1/x4/x8/x16 slot.
6. Before handling the PCIe-7396, discharge any static buildup on your body by touching the metal case of the computer. Hold the edge and do not touch the components.
7. Position the PCIe-7396 into the PCI Express slot.
8. Secure the PCIe-7396 in place.

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2.5 SCSI Connector

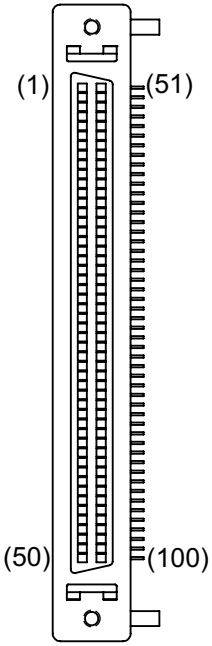


Figure 2-2: SCSI Connector

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Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
(1)	P1A0	(26)	P2A0	(51)	P3A0/ EVENT	(76)	P4A0
(2)	P1A1	(27)	P2A1	(52)	P3A1	(77)	P4A1
(3)	P1A2	(28)	P2A2	(53)	P3A2	(78)	P4A2
(4)	P1A3	(29)	P2A3	(54)	P3A3	(79)	P4A3
(5)	P1A4	(30)	P2A4	(55)	P3A4	(80)	P4A4
(6)	P1A5	(31)	P2A5	(56)	P3A5	(81)	P4A5
(7)	P1A6	(32)	P2A6	(57)	P3A6	(82)	P4A6
(8)	P1A7	(33)	P2A7	(58)	P3A7	(83)	P4A7
(9)	P1B0	(34)	P2B0	(59)	P3B0	(84)	P4B0
(10)	P1B1	(35)	P2B1	(60)	P3B1	(85)	P4B1
(11)	P1B2	(36)	P2B2	(61)	P3B2	(86)	P4B2
(12)	P1B3	(37)	P2B3	(62)	P3B3	(87)	P4B3
(13)	P1B4	(38)	P2B4	(63)	P3B4	(88)	P4B4
(14)	P1B5	(39)	P2B5	(64)	P3B5	(89)	P4B5
(15)	P1B6	(40)	P2B6	(65)	P3B6	(90)	P4B6
(16)	P1B7	(41)	P2B7	(66)	P3B7	(91)	P4B7
(17)	P1C0	(42)	P2C0	(67)	P3C0	(92)	P4C0
(18)	P1C1	(43)	P2C1	(68)	P3C1	(93)	P4C1
(19)	P1C2	(44)	P2C2	(69)	P3C2	(94)	P4C2
(20)	P1C3	(45)	P2C3	(70)	P3C3	(95)	P4C3
(21)	P1C4	(46)	P2C4	(71)	P3C4	(96)	P4C4
(22)	P1C5	(47)	P2C5	(72)	P3C5	(97)	P4C5
(23)	P1C6	(48)	P2C6	(73)	P3C6	(98)	P4C6
(24)	P1C7	(49)	P2C7	(74)	P3C7	(99)	P4C7/ EXTTRG
(25)	GND	(50)	GND	(75)	GND	(100)	GND

Table 2-2: SCSI Connector Pin Assingments

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NOTE:

- The DIO pin names are specified as PnXb, where n: means the PPI number of the PCIe-7396, n=1-4
- X: means the port name of the PPI, X= ‘A’ , ‘B’ or ‘C’
- b: means the bit number of the port, b=0-7. For example, P1C4 means bit 4 of port C on PPI1.
- EXTTRG: External trigger signal to capture digital input data
- EVENT: External event source for counter 0
- GND: Ground

2.6 Jumpers

The PCIe-7396 is a ‘plug and play’ add-on card using the PCI Express bus. It is unnecessary to set up its base address and IRQ level to fit the hardware of the computer system. However, there are some jumpers to set the power-on-states of all I/O ports.

2.6.1 Power-on-state

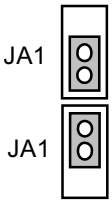
For all I/O ports on the PCIe-7396, the power-on-states are either pulled high, pulled low, or floating, depending on the jumper settings. The table below lists the reference numbers of the jumpers and their corresponding port names.

Jumper	Port Name	Jumper	Port Name
JA1	P1A	JA3	P3A
JB1	P1B	JB3	P3B
JC1	P1C	JC3	P3C
JA2	P2A	JA4	P4A
JB2	P2B	JB4	P4B
JC2	P2C	JC4	P4C

Table 2-3: Jumpers and Port Names

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The power-on-state of each port can be set independently. To pull all signals low is the default setting. The following diagram uses JA1 as an example to show the possible settings.



Port A of PPI1 is pulled low.(default setting)

Port A of PPI1 is pulled high.

When the jumper cap is removed, the power-on-state is floating.

2.7 Terminal Board Support

The PCIe-7396 can be connected to several different daughter boards, including the DIN-100S, DIN-96DI, and DIN-96DO (EOL). The functionality and connections are specified as follows.

2.7.1 DIN-100S Terminal Board

The DIN-100S is a direct connector for an add-on card that is equipped with a SCSI-100 connector. It is suitable for simple applications that do not need an isolated connection in front of the digital inputs or outputs of the PCIe-7396.

2.7.2 DIN-96DI Terminal Board

The DIN-96DI digital input terminal board features high-voltage opto-isolation on all inputs to prevent floating potential and ground loop problems from damaging the system. It is composed of one TB-96 baseboard, one TB-96DI daughter board, and one DIN socket for easy maintenance, wiring, and installation. It provides 96 channels that are accessed through a SCSI-100 connector.

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2.7.3 DIN-96DO Terminal Board (EOL)

The DIN-96DO digital output termination board features high-voltage opto-isolation on all outputs to prevent floating potential and ground loop problems from damaging the system. It is composed of one TB-96 baseboard, one TB-96DO daughter board, and one DIN socket for easy maintenance, wiring, and installation. It provides 96 channels that are accessed through a SCSI-100 connector.

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3 Register Format

Detailed descriptions of the register format are specified in this chapter. This information is useful for programmers wanting to handle the PCIe-7396 with low-level programming. In addition, this chapter can help users understand how to use software drivers to manipulate the PCIe-7396.

3.1 I/O Address Map

Most of the PCIe-7396 registers are 32 bits. Users can access these registers with 32-bit I/O instructions. The following table shows the register map, including descriptions and their offset addresses relative to the base address.

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Offset	Write	Read
0x00	P1ABC	P1ABC
0x04	P1Control	Not used
0x08	P1EXTTRG Enable	Not used
0x0C	P1EXTTRG Disable	Not used
0x10	P2ABC	P2ABC
0x14	P2Control	Not used
0x18	P2EXTTRG Enable	Not used
0x1C	P2EXTTRG Disable	Not used
0x20	P3ABC	P3ABC
0x24	P3Control	Not used
0x28	P3EXTTRG Enable	Not used
0x2C	P3EXTTRG Disable	Not used
0x30	P4ABC	P4ABC
0x34	P4Control	Not used
0x38	P4EXTTRG Enable	Not used
0x3C	P4EXTTRG Disable	Not used
0x40	Timer/Counter #0	Timer/Counter #0
0x44	Timer/Counter #1	Timer/Counter #1
0x48	Timer/Counter #2	Timer/Counter #2
0x4C	Timer/Counter Mode Control	Timer/Counter Mode Status
0x50	ISC: Interrupt Source Control	Not used
0x54	Clear Interrupt	Not used
0x60	P1 COS Control	Not used
0x64	P2 COS Control	Not used
0x68	P3 COS Control	Not used
0x6C	P4 COS Control	Not used

Table 3-1: Register Map

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3.2 PPI Registers

The PCIe-7396 has 2/4 PPIs onboard. Each PPI contains 5 registers, including a Digital Data Register, Control Register, External Trigger Enable Register, External Trigger Disable Register, and COS Interrupt Control Register, detailed in the following sections.

3.2.1 Digital Data Register

The 24-bit I/O data of the PCIe-7396 is accessed from/to this register by software. The digital data can also be read back through this register.

Address: BASE + 00h

Attribute: read and write

Data Format:

Bit	7	6	5	4	3	2	1	0
BASE+00h	P1A 7	P1A 6	P1A 5	P1A 4	P1A 3	P1A 2	P1A 1	P1A 0
BASE+01h	P1B 7	P1B 6	P1B 5	P1B 4	P1B 3	P1B 2	P1B 1	P1B 0
BASE+02h	P1C 7	P1C 6	P1C 5	P1C 4	P1C 3	P1C 2	P1C 1	P1C 0
BASE+03h	X	X	X	X	X	X	X	X

NOTE:

P1X7-P1X0: Digital I/O data
X: A-C

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3.2.2 Control Register

Each PPI's control register is used to set its three ports to be as input or output independently.

Address: BASE + 04h

Attribute: write only

Data Format:

Bit	7	6	5	4	3	2	1	0
BASE+04h	X	X	X	X	X	P1C	P1B	P1A
BASE+05h	X	X	X	X	X	X	X	X
BASE+06h	X	X	X	X	X	X	X	X
BASE+07h	X	X	X	X	X	X	X	X


NOTE:

P1n: n: port number
Set to '0' for input port, '1' for output port.

3.2.3 External Trigger Enable Register

Users can write anything to this register to enable the external trigger to capture input data of ports A, B and C simultaneously. Note that when this register is enabled, the settings of the previous control register are disabled.

Address: BASE + 08h

Attribute: write only

Data Format:

Bit	7	6	5	4	3	2	1	0
BASE+08h	X	X	X	X	X	X	X	X
BASE+09h	X	X	X	X	X	X	X	X
BASE+0Ah	X	X	X	X	X	X	X	X
BASE+0Bh	X	X	X	X	X	X	X	X

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3.2.4 External Trigger Disable Register

Users can write anything to this register to disable the function of external trigger.

Address: BASE + 0Ch

Attribute: write only

Data Format:

Bit	7	6	5	4	3	2	1	0
BASE+0Ch	X	X	X	X	X	X	X	X
BASE+0Dh	X	X	X	X	X	X	X	X
BASE+0Eh	X	X	X	X	X	X	X	X
BASE+0Fh	X	X	X	X	X	X	X	X

3.2.5 Change of State (COS) Interrupt Control Register

This register is used to configure the COS interrupt.

Address: BASE + 60h

Attribute: write only

Data Format:

Bit	7	6	5	4	3	2	1	0
BASE+60h	X	X	X	X	X	P1C	P1B	P1A
BASE+61h	X	X	X	X	X	X	X	X
BASE+62h	X	X	X	X	X	X	X	X
BASE+63h	X	X	X	X	X	X	X	X



P1n: n: port number
Set to ‘0’ to disable COS, ‘1’ to enable COS.

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3.3 Interrupt Source Control (ISC) Register

The PCIe-7396 has a dual interrupt system. Two interrupt sources can be generated and be distinguished by software settings. This register is used to select the interrupt sources.

Address: BASE + 50h

Attribute: write only

Data Format:

Bit	7	6	5	4	3	2	1	0
BASE+50h	X	X	X	X	C2_ 1	C2_ 0	C1_ 1	C1_ 0
BASE+51h	X	X	X	X	X	X	X	X
BASE+52h	X	X	X	X	X	X	X	X
BASE+53h	X	X	X	X	X	X	X	X

NOTE:

C1_0, C1_1: Select source INT 1
C2_0, C2_1: Select source INT 2

INT1	C1_1	C1_0	IRQ Sources	IRQ Trigger Condition
Mode 1	0	0	COS P1&P2 (48 bits)	Change of State for PCIe-7396 P1 & P2
Mode 2	0	1	P1C0 OR -P1C3	(see Table 4-2 on page 26)
Mode 3	1	0	-P1C0	Falling edge of P1C0
Mode 4	1	1	Event Counter	Counter countdown to 0

INT2	C2_1	C2_0	IRQ Sources	IRQ Trigger Condition
Mode 1	0	0	COS P3&P4 (48 bits)	Change of State for PCIe-7396 P3 & P4
Mode 2	0	1	P2C0 OR -P2C3	(see Table 4-2 on page 26)
Mode 3	1	0	-P2C0	Falling edge of P2C0
Mode 4	1	1	32-bit Timer	Timer countdown to 0

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3.4 Clear Interrupt Register

Users can write anything to this register to clear the interrupt request of the PCIe-7396.

Address: BASE + 54h

Attribute: write only

Data Format:

Bit	7	6	5	4	3	2	1	0
BASE+54h	X	X	X	X	X	X	X	X
BASE+55h	X	X	X	X	X	X	X	X
BASE+56h	X	X	X	X	X	X	X	X
BASE+57h	X	X	X	X	X	X	X	X

3.5 Timer/Counter Register

The 8254 chip occupies 4 I/O addresses in the PCIe-7396. Refer to NEC's or Intel's datasheet for the full description of the 8254's operations.

Address: BASE + 40h to BASE + 4Ch

Attribute: read/write

Data Format:

Address	Data Format
BASE+40h	Bit 7 to Bit 0: Counter 0 Register
BASE+41h	Bit 7 to Bit 0: Counter 1 Register
BASE+42h	Bit 7 to Bit 0: Counter 2 Register
BASE+43h	Bit 7 to Bit 0: Control Register

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3.6 High Level Programming

You can bypass the detailed register structures of the PCIe-7396 with a high-level application programming interface (API).

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4 Functional Operations

Functional operations are described in this chapter in order to help users understand how to manipulate or program the PCIe-7396.

4.1 Digital I/O Ports

The PCIe-7396 has 2/4 onboard PPIs. Each 24-bit PPI is divided into three 8-bit I/O ports: A, B, and C. All of these 6/12 ports can be programmed as input or output independently.

4.1.1 External Trigger

Pin-99 EXTTRG allows users to receive an external trigger to capture input data. User can use the _7396_Set_Event_Edge function to set the EXTTRG pin to be active high or active low.

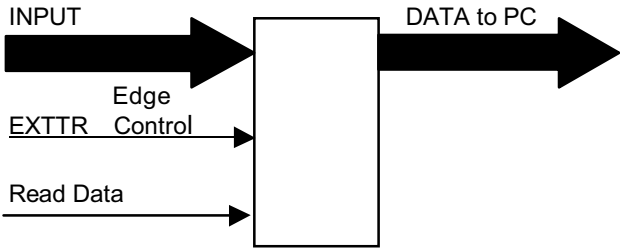


Figure 4-1: External Trigger Function Block Diagram

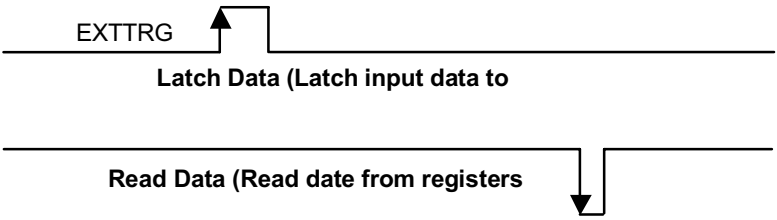


Figure 4-2: Read Data Using External Trigger Diagram

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4.2 8254 Timer/Counter Operation

One 8254 programmable timer/counter chip is installed on the PCIe-7396. There are three counters and six possible operation modes for each counter.

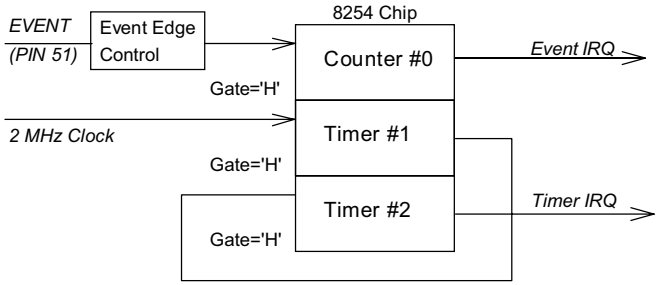


Figure 4-3: Timer/Counter System Block Diagram

4.2.1 Cascaded 32-bit Timer

The base frequency of the input clock for the cascaded timer is 2MHz. The output is sent as the timer interrupt. To set the maximum and minimum frequency of the timer, refer to the _7396_Cascaded_Timer function.

4.2.2 Event Counter and Edge Control

Counter #0 of the 8254 is used as an event counter. The input is Pin-51 of CN1. The trigger edge of the counter clock is programmable. The gate control fixs high when enabled. The output is send as the event interrupt, so that if counter #0 is set as 8254 mode 0, the event IRQ asserts as the counter counts down to zero.

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4.3 Interrupt Circuit

4.3.1 System Architecture

The PCIe-7396 has a dual interrupt system, meaning the hardware can generate two interrupt request signals at the same time and the software can service these two request signals by ISR. Note that the dual interrupt does not mean the card occupies two IRQ levels.

The two interrupt request signals (INT1 and INT2) come from digital inputs or the timer/counter outputs. Two multiplexers (MUX) are used to select the IRQ sources. Figure 4-4 shows the interrupt system.

4.3.2 IRQ Level Setting

There is only one IRQ level needed in the PCIe-7396, although it is a dual interrupt system, because it uses INT #A interrupt request signal on the PCI Express bus. The motherboard circuits transfer INT #A to one of the AT bus IRQ levels. The IRQ level is set by the BIOS and saved in the PCI Express controller. It is not necessary for users to set the IRQ level. Users can get the IRQ level from the software library.

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4.3.3 Dual Interrupt System

The PCI Express controller can receive two hardware IRQ requests. However, only one IRQ will be sent to the PCI Express bus, the two IRQ requests must be distinguished by an interrupt service routine (ISR).

The two IRQ requests are INT1 and INT2. INT1 comes from COS P1 & P2, P1C0, P1C3, or the event counter interrupt. INT2 comes from COS P3 & P4, P2C0, P2C3, or the timer interrupt. The sources of INT1 and INT2 is selectable by using the Interrupt Source Control (ISC) Register.

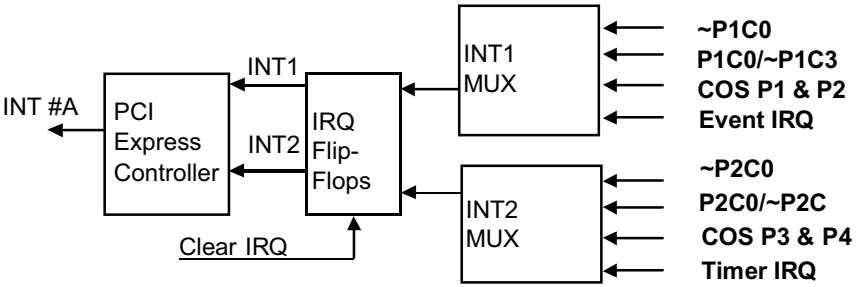


Figure 4-4: Dual Interrupt System

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4.3.4 Interrupt Source Control (ISC)

There are four bits to control the IRQ sources of INT1 and INT2. Table 4-1 shows the selection of the IRQ sources and the interrupt trigger condition.

If the application needs one IRQ only, you can disable one of the IRQ sources by software. You can also disable both interrupts If you do not need any IRQ source. However, the BIOS still assigns an IRQ level to the PCI Express card and occupies the PC resource if you only disable the IRQ sources without changing the initial condition of the PCI Express controller.

INT1	C1	C2	IRQ Sources	IRQ Trigger Condition
Disable	4	X	INT1 disable	--
Mode 1 (default)	0	X	COS P1&P2 (48 bits)	Change of State for PCIe-7396
Mode 2	1	X	P1C0 OR -P1C3	(see Table 4-2 on page 26)
Mode 3	2	X	-P1C0	Falling edge of P1C0
Mode 4	3	X	Event Counter	Counter countdown to 0

INT2	C1	C2	IRQ Sources	IRQ Trigger Condition
Disable	X	4	INT2 disable	--
Mode 1 (default)	X	0	COS P3&P4 (48 bits)	Change of State for PCIe-7396
Mode 2	X	1	P2C0 OR -P2C3	(see Table 4-2 on page 26)
Mode 3	X	2	-P2C0	Falling edge of P2C0
Mode 4	X	3	Timer Output	Timer countdown to 0

Table 4-1: ISC Register Format


NOTE:

"Mode 1" is the default setting.

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When the IRQ sources is set as “P1C0 OR -P1C3” or “P2C0 OR -P2C3”, the IRQ trigger conditions are summarized in Table 4-2.

P1C0	P1C3	IRQ Trigger Condition
High	X	P1C0=‘H’ disable all IRQ
X	Low	P1C3=‘L’ disable all IRQ
Low	1->0	P1C3 falling edge trigger when P1C0=L
0->1	High	P1C0 rising edge trigger when P1C3=H

P2C0	P2C3	IRQ Trigger Condition
High	X	P2C0=‘H’ disable all IRQ
X	Low	P2C3=‘L’ disable all IRQ
Low	1->0	P2C3 falling edge trigger when P2C0=L
0->1	High	P2C0 rising edge trigger when P2C3=H

Table 4-2: IRQ Trigger Conditions

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4.3.5 Change of State (COS) Interrupt

A Change of State (COS) occurs when the input state (logic level) is changed from low to high, or from high to low. The COS detection circuit will detect the edge of level change. On the PCIe-7396, the COS detection circuit is applied to all the input channels. When any channel changes its logic level, the COS detection circuit generates an interrupt request to the PCI Express controller.

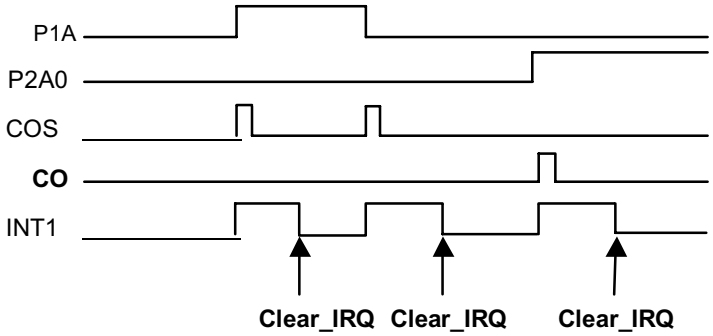


Figure 4-5: Change of State (COS) Interrupt

4.3.5.1 COS Detection

The following timing is an example of COS operation. All the DI signal level changes will be detected and then use an 'OR' operation to generate the INT1 or INT2 IRQ request.

If an INT1 or INT2 IRQ request is generated, the signal will be captureed. Use the _7396_CLR_IRQ function to reset the state after the corresponding ISR is finished.

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Important Safety Instructions

For user safety, please read and follow all instructions, Warnings, Cautions, and Notes marked in this manual and on the associated device before handling/operating the device, to avoid injury or damage.

- Read these safety instructions carefully.
- Keep the User's Manual for future reference.
- Read the Specifications section of this manual for detailed information on the recommended operating environment.
- The device can be operated at an ambient temperature of 45ºC with DC input, and 35ºC with adapter input.
- It is recommended that the device be installed in Information Technology Rooms that are in accordance with Article 645 of the National Electrical Code and NFPA 75.
- To avoid electrical shock and/or damage to device:
  - Keep device away from water or liquid sources.
  - Keep device away from high heat or humidity.
  - Keep device properly ventilated (do not block or cover ventilation openings).
  - Always use recommended voltage and power source settings.
  - Always install and operate device near an easily accessible electrical outlet.
  - Secure the power cord (do not place any object on/over the power cord).
  - Only install/attach and operate device on stable surfaces and/or recommended mountings.
  - The power cord must be connected to a socket or outlet with a ground connection.
- If the device will not be used for long periods of time, turn off and unplug from its power source.
- Never attempt to repair the device, which should only be serviced by qualified technical personnel using suitable tools.

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- A Lithium-type battery may be provided for uninterrupted backup or emergency power.



Risk of explosion if battery is replaced with one of an incorrect type; please dispose of used batteries appropriately.

- This equipment is not suitable for use in locations where children are likely to be present.
- The device must be serviced by authorized technicians when:
  - The power cord or plug is damaged
  - Liquid has entered the device interior
  - The device has been exposed to high humidity and/or moisture
  - The device is not functioning or does not function according to the User's Manual
  - The device has been dropped and/or damaged and/or shows obvious signs of breakage
- Disconnect the power supply cord before loosening the thumbscrews and always fasten the thumbscrews with a screwdriver before starting the system up
- It is recommended that the device be installed only in a server room or computer room where access is:
  - Restricted to qualified service personnel or users familiar with restrictions applied to the location, reasons therefor, and any precautions required
  - Only afforded by the use of a tool or lock and key, or other means of security, and controlled by the authority responsible for the location



BURN HAZARD

Hot surface! Do not touch! Touching this surface could result in bodily injury. To reduce risk, allow the surface to cool before touching.

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Consignes de Sécurité Importante

S'il vous plaît prêter attention stricte à tous les avertissements et mises en garde figurant sur l'appareil, pour éviter des blessures ou des dommages.

- *Lisez attentivement ces consignes de sécurité.*
- *Conservez le manuel de l'utilisateur pour pouvoir le consulter ultérieurement.*
- *Lisez la section Spécifications de ce manuel pour des informations détaillées sur l'environnement d'exploitation recommandé.*
- *L'appareil peut être utilisé à une température ambiante de 45°C avec entrée CC pour les série MVP-61; 35ºC avec entrée adaptateur pour la série MVP-61.*
- *Il est recommandé d'installer l'appareil dans des salles de technologie de l'information conformes à l'article 645 du National Electrical Code et à la NFPA 75.*
- *Pour éviter les chocs électriques et/ou d'endommager l'appareil:*
  - *Tenez l'appareil à l'écart de toute source d'eau ou de liquide.*
  - *Tenez l'appareil à l'écart d'une forte chaleur ou d'une humidité élevée.*
  - *Maintenez l'appareil correctement ventilé (n'obstruer ou ne couvrez pas les ouvertures de ventilation).*
  - *Utilisez toujours les réglages de tension et de source d'alimentation recommandés.*
  - *Installez et utilisez toujours l'appareil près d'une prise de courant facilement accessible.*
  - *Fixez le cordon d'alimentation (ne placez aucun objet sur le cordon d'alimentation).*
  - *Installez/fixez et utilisez l'appareil uniquement sur des surfaces stables et/ou sur les fixations recommandées.*
  - *Le cordon d'alimentation doit être connecté à une prise ou à une prise de courant avec mise à la terre.*

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- Si l'appareil ne doit pas être utilisé pendant de longues périodes, éteignez-le et débranchez-le de sa source d'alimentation
- *N'essayez jamais de réparer l'appareil, qui ne doit être réparé que par un personnel technique qualifié à l'aide d'outils appropriés*
- *Une batterie de type Lithium peut être fournie pour une alimentation de secours ininterrompue ou d'urgence.*



ATTENTION: Risque d'explosion si la pile est remplacée par une autre de type incorrect. Veuillez jeter les piles usagées de façon appropriée.

- *Cet équipement ne convient pas à une utilisation dans des lieux pouvant accueillir des enfants.*
- *L'appareil doit être entretenu par des techniciens agrees lorsque:*
- *Le cordon d'alimentation ou la prise est endommagé(e)*
- *Un liquide a pénétré à l'intérieur de l'appareil.*
- *L'appareil a été exposé à une forte humidité et/ou de la buée.*
- *L'appareil ne fonctionne pas ou ne fonctionne pas selon le manuel de l'utilisateur.*
- *L'appareil est tombé et/ou a été endommagé et/ou présente des signes évidents de dommage.*
- *Débranchez le cordon d'alimentation avant de desserrer les vis à oreilles et serrez toujours les vis à oreilles avec un tournevis avant de mettre le système en marche.*
- *Il est recommandé d'installer l'appareil uniquement dans une salle de serveurs ou une salle informatique où l'accès est:*
  - *Réservé au personnel de service qualifié ou aux utilisateurs familiarisés avec les restrictions appliquées à l'emplacement, aux raisons de ces restrictions et toutes les précautions requises*
  - *Uniquement autorisé par l'utilisation d'un outil, d'une serrure et d'une clé, ou d'un autre moyen de sécurité, et contrôlé par l'autorité responsable de l'emplacement.*

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	***RISQUE DE BRÛLURES*** ***Partie chaude!*** *Ne touchez pas cette surface, cela pourrait entraîner des blessures. Pour éviter tout danger, laissez la surface refroidir avant de la toucher.*

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