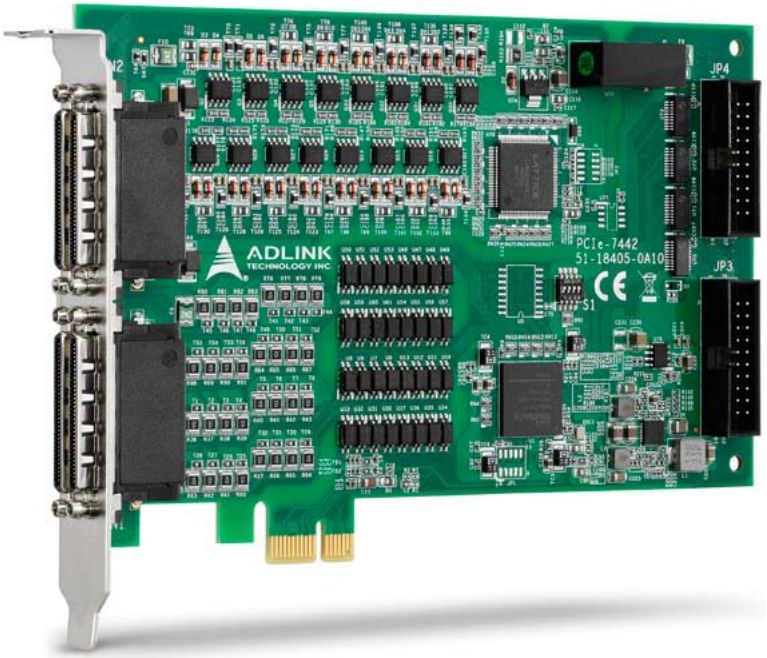
PCIe-7442

64CH Isolated DI/64CH Isolated DO PCIe Card

User's Manual



Manual Rev.: 2.00

Revision Date: Dec. 30, 2016

Part No: 50-11264-1000

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Revision History

Revision	Release Date	Description of Change(s)
2.00	Dec. 30, 2016	Initial release

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Preface

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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.


NOTE:

Additional information, aids, and tips that help users perform tasks.


CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.


WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

ADLINK'S PCIe-7442 is a basic digital I/O card for PCIe bus computers in industrial applications.

All digital input channels are identical non-polar and opto-isolated, suitable for collecting digital input in noisy environments. COS (Change of state) interrupt is supported, whereby when any digital input changes state, an interrupt is generated to allow management of the event. The input common junction can be common ground or common power, dependent on the user environment. Accordingly, the digital input can be a current source or current sink. When isolated digital output is ON, sink current is conducted through the transistors, and when OFF, none is.


NOTE:

When multiple PCIe-7442 cards are installed, board ID provides convenient identification of each via switch jumper for quick troubleshooting and easy maintenance.

1.1 Features

- PCI Express x1, Plug and Play
- Isolated digital input channels
- Isolated digital output channels
- Change-of-state (COS) detection
- Channels with 28 V voltage protection
- Channels with 250 mA sink current
- Channels with digital output status read back
- DO value retained after hot system reset
- Programmable power-up DO status
- Programmable safety DO status function after WDT interrupt
- Watchdog timer
- TTL I/O channels
- 1250 VRMS isolation
- Board ID capability

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1.2 Applications

- Industrial ON/OFF control
- External high power relay driving, signal switching
- Laboratory automation
- Industrial automation
- Switch contact status detection and limit switch monitoring & control systems

1.3 Specifications

Digital Input	
Input channels	64
Photocoupler	PC3H4
Input current	10 mA rated 50 mA max. for isolated input
Input voltage	Up to 28V, non-polarity Logic Low: 0 to 1.5V Logic High: 5 to 28V
Input impedance	4.7kΩ@0.5W
Interrupt sources	Change of State (COS)
Isolated voltage	1,250 Vrms channel-to-system
Digital Output	
Output channels	64
Output type	Open drain power MOSFET driver
Output voltage	5V DC min, 40V DC maximum
Throughput	1kHz (CPU: DualCore Intel Pentium D 925,3.00GHz)
Isolated voltage	1,250 Vrms channel-to-system
Isolated +5V Power Supply	
Output voltage	+5V
Output current	100mA max. (@ 40°C)
Physical	
Dimensions	175 mm x 107 mm, standard PCIe half size

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Operating temperature	0 to 60°C
Storage temperature	-20 to 80 °C
Humidity	5 to 95% non-condensing
Bus	1x PCI Express
Power consumption	+12V@170mA (typical) 300mA (Max.) +3.3V@ 1mA (typical) 1.5mA (Max.) (when all relays are activated simultaneously)

1.4 Software Support

ADLINK provides comprehensive software solutions for all system building requirements. In addition to programming libraries such as DLLs for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW®.

Ensure the driver and utility are installed before using the PCIe-7442.

PCIS-DASK

PCIS-DASK consists of advanced 32/64-bit kernel drivers and SDK for customized DAQ application development, enabling detailed operations, superior performance, and reliability from data acquisition systems.

PCIS-DASK kernel drivers currently support Windows 7/8.1 OS.

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1.5 PCB Layout

NOTE:

All dimensions shown are in mm

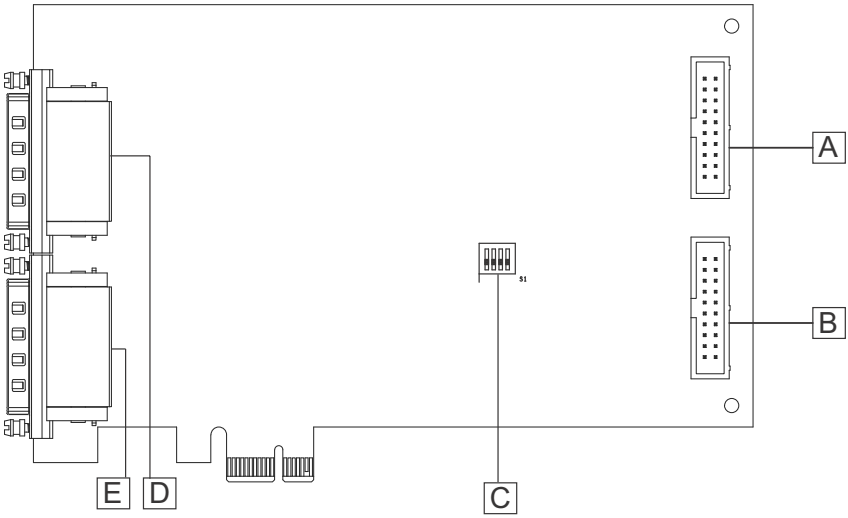


Figure 1-1: PCIe-7442 Board Layout

A	JP4	16CH (TTL15 to 31) TTL I/O connector
B	JP3	16CH (TTL 0 to 15) TTL I/O connector
C	S1	Board ID DIP switch
D	CN2	64CH isolated digital output connector
E	CN1	64CH isolated digital input connector

Table 1-1: PCIe-7442 Board Layout Legend

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1.6 Connectors

The PCIe-7442 is equipped with a 68-pin Dual port VHDCI connector, via CN1A, CN1B, CN2A, and CN2B.

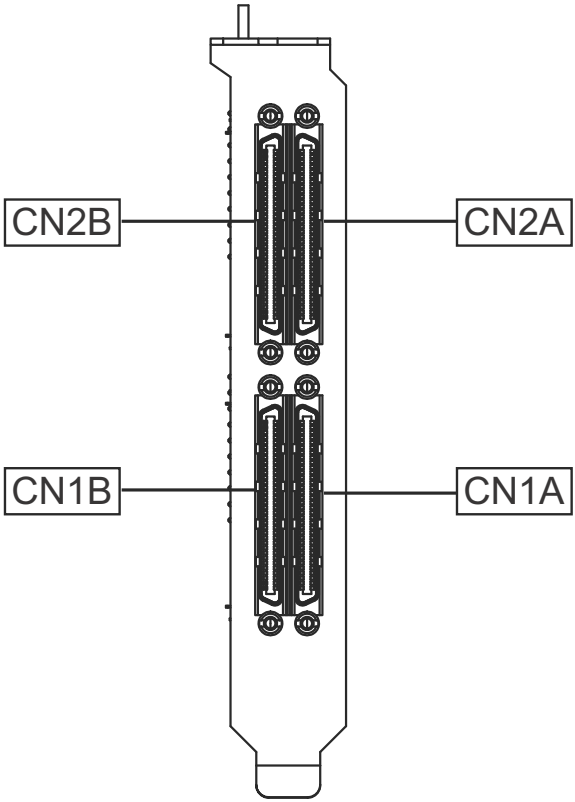


Figure 1-2: CN1/CN2 Connector

IDI_0	**A01**	**A35**	IDI_8
IDI_1	**A02**	**A36**	IDI_9
IDI_2	**A03**	**A37**	IDI_10
IDI_3	**A04**	**A38**	IDI_11

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IDI_4	**A05**	**A39**	IDI_12
IDI_5	**A06**	**A40**	IDI_13
IDI_6	**A07**	**A41**	IDI_14
IDI_7	**A08**	**A42**	IDI_15
COM1	**A09**	**A43**	COM2
COM1	**A10**	**A44**	COM2
COM1	**A11**	**A45**	COM2
COM1	**A12**	**A46**	COM2
COM1	**A13**	**A47**	COM2
COM1	**A14**	**A48**	COM2
COM1	**A15**	**A49**	COM2
COM1	**A16**	**A50**	COM2
N/C	**A17**	**A51**	N/C
IDI_16	**A18**	**A52**	IDI_24
IDI_17	**A19**	**A53**	IDI_25
IDI_18	**A20**	**A54**	IDI_26
IDI_19	**A21**	**A55**	IDI_27
IDI_20	**A22**	**A56**	IDI_28
IDI_21	**A23**	**A57**	IDI_29
IDI_22	**A24**	**A58**	IDI_30
IDI_23	**A25**	**A59**	IDI_31
COM3	**A26**	**A60**	COM4
COM3	**A27**	**A61**	COM4
COM3	**A28**	**A62**	COM4
COM3	**A29**	**A63**	COM4
COM3	**A30**	**A64**	COM4
COM3	**A31**	**A65**	COM4
COM3	**A32**	**A66**	COM4
COM3	**A33**	**A67**	COM4
N/C	**A34**	**A68**	N/C

Figure 1-3: CN1A Connector ID

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N/C	**B68**	**B34**	N/C
COM8	**B67**	**B33**	COM7

COM8	**B66**	**B32**	COM7
COM8	**B65**	**B31**	COM7
COM8	**B64**	**B30**	COM7
COM8	**B63**	**B29**	COM7
COM8	**B62**	**B28**	COM7
COM8	**B61**	**B27**	COM7
COM8	**B60**	**B26**	COM7
IDI_63	**B59**	**B25**	IDI_55
IDI_62	**B58**	**B24**	IDI_54
IDI_61	**B57**	**B23**	IDI_53
IDI_60	**B56**	**B22**	IDI_52
IDI_59	**B55**	**B21**	IDI_51
IDI_58	**B54**	**B20**	IDI_50
IDI_57	**B53**	**B19**	IDI_49
IDI_56	**B52**	**B18**	IDI_48
N/C	**B51**	**B17**	N/C
COM6	**B50**	**B16**	COM5
COM6	**B49**	**B15**	COM5
COM6	**B48**	**B14**	COM5
COM6	**B47**	**B13**	COM5
COM6	**B46**	**B12**	COM5
COM6	**B45**	**B11**	COM5
COM6	**B44**	**B10**	COM5
COM6	**B43**	**B09**	COM5
IDI_47	**B42**	**B08**	IDI_39
IDI_46	**B41**	**B07**	IDI_38
IDI_45	**B40**	**B06**	IDI_37
IDI_44	**B39**	**B05**	IDI_36
IDI_43	**B38**	**B04**	IDI_35
IDI_42	**B37**	**B03**	IDI_34
IDI_41	**B36**	**B02**	IDI_33
IDI_40	**B35**	**B01**	IDI_32

Figure 1-4: CN1B Connector ID

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Pin	Definition
IDI_n	Isolated digital input channel n
COM1	Common VDD junction for input channels 0-7
COM2	Common VDD junction for input channels 8-15
COM3	Common VDD junction for input channels 16-23
COM4	Common VDD junction for input channels 24-31
COM5	Common VDD junction for input channels 32-39
COM6	Common VDD junction for input channels 40-47
COM7	Common VDD junction for input channels 48-55
COM8	Common VDD junction for input channels 56-63
N/C	No connection

Table 1-2: CN1 Connector Pin Assignment

IDO_0	**A01**	**A35**	IDO_8
IDO_1	**A02**	**A36**	IDO_9
IDO_2	**A03**	**A37**	IDO_10
IDO_3	**A04**	**A38**	IDO_11
IDO_4	**A05**	**A39**	IDO_12
IDO_5	**A06**	**A40**	IDO_13
IDO_6	**A07**	**A41**	IDO_14
IDO_7	**A08**	**A42**	IDO_15
VDD1	**A09**	**A43**	VDD2
IGND	**A10**	**A44**	IGND
IGND	**A11**	**A45**	IGND
IGND	**A12**	**A46**	IGND
IGND	**A13**	**A47**	IGND
IGND	**A14**	**A48**	IGND
IGND	**A15**	**A49**	IGND
IGND	**A16**	**A50**	IGND
N/C	**A17**	**A51**	N/C
IDO_16	**A18**	**A52**	IDO_24

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IDO_17	**A19**	**A53**	IDO_25
IDO_18	**A20**	**A54**	IDO_26
IDO_19	**A21**	**A55**	IDO_27
IDO_20	**A22**	**A56**	IDO_28
IDO_21	**A23**	**A57**	IDO_29
IDO_22	**A24**	**A58**	IDO_30
IDO_23	**A25**	**A59**	IDO_31
VDD3	**A26**	**A60**	VDD4
IGND	**A27**	**A61**	IGND
IGND	**A28**	**A62**	IGND
IGND	**A29**	**A63**	IGND
IGND	**A30**	**A64**	IGND
IGND	**A31**	**A65**	IGND
IGND	**A32**	**A66**	IGND
IGND	**A33**	**A67**	IGND
N/C	**A34**	**A68**	N/C

Figure 1-5: CN2A Connector ID

V5V	**B68**	**B34**	V5V
IGND	**B67**	**B33**	IGND
IGND	**B66**	**B32**	IGND
IGND	**B65**	**B31**	IGND
IGND	**B64**	**B30**	IGND
IGND	**B63**	**B29**	IGND
IGND	**B62**	**B28**	IGND
IGND	**B61**	**B27**	IGND
VDD8	**B60**	**B26**	VDD7
IDO_63	**B59**	**B25**	IDO_55
IDO_62	**B58**	**B24**	IDO_54
IDO_61	**B57**	**B23**	IDO_53
IDO_60	**B56**	**B22**	IDO_52
IDO_59	**B55**	**B21**	IDO_51
IDO_58	**B54**	**B20**	IDO_50

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IDO_57	**B53**	**B19**	IDO_49
IDO_56	**B52**	**B18**	IDO_48
N/C	**B51**	**B17**	N/C
IGND	**B50**	**B16**	IGND
IGND	**B49**	**B15**	IGND
IGND	**B48**	**B14**	IGND
IGND	**B47**	**B13**	IGND
IGND	**B46**	**B12**	IGND
IGND	**B45**	**B11**	IGND
IGND	**B44**	**B10**	IGND
VDD6	**B43**	**B09**	VDD5
IDO_47	**B42**	**B08**	IDO_39
IDO_46	**B41**	**B07**	IDO_38
IDO_45	**B40**	**B06**	IDO_37
IDO_44	**B39**	**B05**	IDO_36
IDO_43	**B38**	**B04**	IDO_35
IDO_42	**B37**	**B03**	IDO_34
IDO_41	**B36**	**B02**	IDO_33
IDO_40	**B35**	**B01**	IDO_32

Figure 1-6: CN2B Connector ID

Pin	Definition
IDO_n	Isolated digital output channel n
VDD1	Common VDD junction for output channels 0-7
VDD2	Common VDD junction for output channels 8-15
VDD3	Common VDD junction for output channels 16-23
VDD4	Common VDD junction for output channels 24-31
VDD5	Common VDD junction for output channels 32-39
VDD6	Common VDD junction for output channels 40-47
VDD7	Common VDD junction for output channels 48-55
VDD8	Common VDD junction for output channels 56-63
IGND	Ground return path for isolated output channels

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Pin	Definition
V5V	Onboard unregulated 5V power supply output
N/C	No connection

Table 1-3: CN2 Connector Pin Assignment

1.7 DI/O Connections

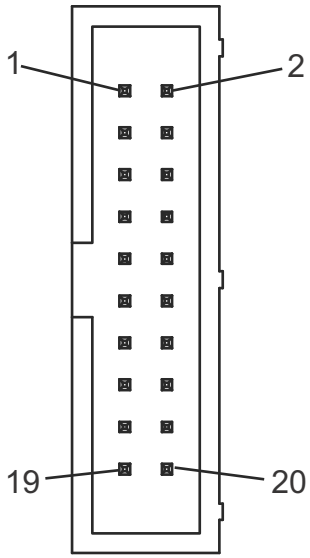


Figure 1-7: I/O Connector

TTLIO_n	TTL I/O channel n
SGND	System ground for PCIe-7442 card

Pin	Function	Pin	Function
1	TTLIO_0	2	TTLIO_8
3	TTLIO_1	4	TTLIO_9

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Pin	Function	Pin	Function
5	TTLIO_2	6	TTLIO_10
7	TTLIO_3	8	TTLIO_11
9	SGND	10	SGND
11	TTLIO_4	12	TTLIO_12
13	TTLIO_5	14	TTLIO_13
15	TTLIO_6	16	TTLIO_14
17	TTLIO_7	18	TTLIO_15
19	SGND	20	SGND

Table 1-4: JP3 I/O Connector Pin Assignment

Pin	Function	Pin	Function
1	TTLIO_16	2	TTLIO_24
3	TTLIO_17	4	TTLIO_25
5	TTLIO_18	6	TTLIO_26
7	TTLIO_19	8	TTLIO_27
9	SGND	10	SGND
11	TTLIO_20	12	TTLIO_28
13	TTLIO_21	14	TTLIO_29
15	TTLIO_22	16	TTLIO_30
17	TTLIO_23	18	TTLIO_31
19	SGND	20	SGND

Table 1-5: JP4 I/O Connector Pin Assignment

1.8 Digital Channels

1.8.1 Isolated Digital Input Channels

The isolated digital input, with open collector transistor structure, supports voltage range of 0 to 28V with input resistance 4.7K. Connection between external signals and the PCIe-7442 is as shown. Since the input common junction can be common ground

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with the existing environment, digital input can be current source or current sink.

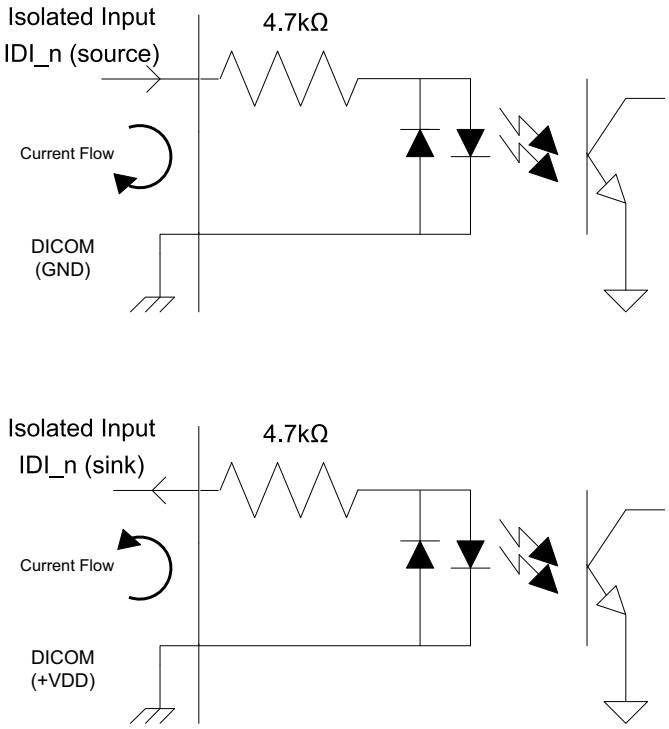


Figure 1-8: Isolated Input Connection

1.8.2 Isolated Digital Output Channels

In the common ground connection of isolated digital output, as shown, when isolated digital output goes ON, sink current passes through the transistors until output is OFF. When the load is of an inductance nature, such as a relay, coil, or motor, the VDD pin must be connected to an external power source, allowing the fly-wheel diode to form a current-release closed loop, whereby transistors are protected from high reverse voltage from inductance loading when the output is switched to OFF.

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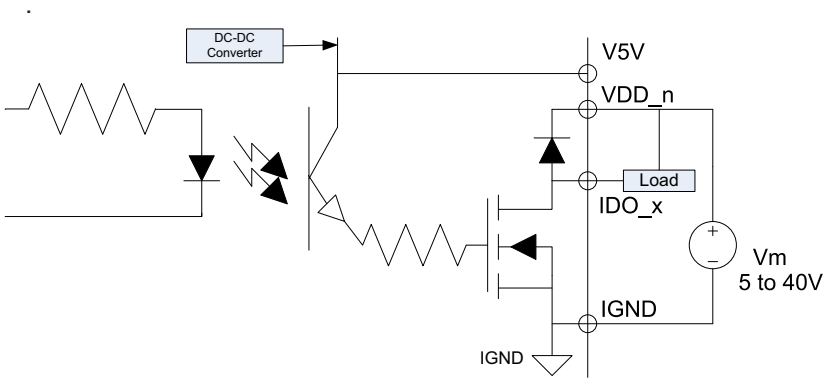


Figure 1-9: Common Ground Connection

1.9 Change of State (COS) Interrupt

The COS designation refers to either the input state (logic level) changing from low to high, or vice versa, with the COS detection circuit ascertaining the edge of the level change. In the PCIe-7442, COS detection is applied to all input channels, wherein when any channel changes logic level, an interrupt request is issued to the PCI controller.

1.9.1 COS Detection

All enabled DI channel signal level changes are detected to generate the interrupt request, during which time corresponding DI data is further latched into the COS latch register. DI data are here sampled by a 33 MHz clock, such that pulse width of the digital input must exceed 31ns, or input data cannot be latched accurately. The COS latch register is erased after the interrupt request is cleared.

1.9.2 COS Detection Architecture

The COS interrupt system generates an interrupt request signal which is serviced request with ISR. The PCIe-7442 has bank 0 from DI0 to DI31 and bank 1 from DI32 to 63, cascaded together toward the same IRQ line via CPLD. Notification can be configured to show which bank or DI line carries the COS when it

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occurs, and to enable/disable the COS function of specific DI lines. COS function for each is disabled as default.

1.10 Programmable Power Up DO Status

The PCIe-7442 provides programmable configuration of all 64CH DO initial status when powering up. As well, the system can be configured to hold DO status and avoid power-up initial configuration after a hot system reset.

1.11 Watchdog Timer (WDT)

In safety-critical applications, enabling watchdog timer (WDT) function automatically generates an interrupt signal for when the OS or card crashes. To enable, the watchdog timer overflow counter must be configured by Windows API. Generally, trigger source is acquired from the onboard 32-bit watchdog timer.

The WDT overflow interval can be programmed via API, and WDT counter value must be reloaded before enabling the WDT, and periodical reload of the timer value enabled by configuration. If the timer is not reloaded within the specified interval, the WDT module generates an overflow interruption signal. When the SafetyOut_Enable bit is enabled, 64CH DO safety statuses are automatically configured. This WDT function is disabled by default.

1.12 Programmable TTL I/O

32CH programmable TTL input/output is provided, with the channels divided between JP3 and JP4 connectors. The direction of each TTL channel can be reconfigured at any time. I/O voltage level is compatible with 5V TTL level and 3.3V TTL level, with driving strength of each channel 4mA. Current consumption of the TTL channel should be regularly monitored.

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2 Getting Started

2.1 Unpacking Checklist

Before unpacking, check the shipping carton for any damage. If the shipping carton and/or contents are damaged, inform your dealer immediately. Retain the shipping carton and packing materials for inspection. Obtain authorization from your dealer before returning any product to ADLINK. Ensure that the following items are included in the package.

- PCIe-7442 high-speed DI/O card
- Quick Start Guide

If any of the items is damaged or missing, contact your dealer immediately.



The card must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the card. Wear a grounded wrist strap when servicing.

2.2 Installing the Card

Install the card driver before you install the card into your computer system. See “Software Support” on page 3. for driver support information.

To install the card:

1. Turn off the system/chassis and disconnect the power plug from the power source.
2. Remove the system/chassis cover.
3. Select the PCIE Express slot that you intend to use, then remove the bracket opposite the slot, if any.
4. Align the card connectors (golden fingers) with the slot, then press the card firmly until the card is completely seated on the slot.
5. Secure the card to the chassis with a screw.

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6. Replace the system/chassis cover.
7. Connect the power plug to a power source, then turn on the system.

Configuration

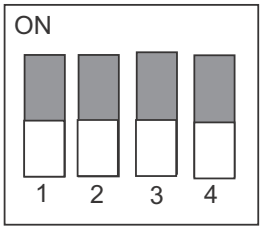
All PCI/PCIE Express cards on your system are configured individually. Because configuration is controlled by the system and the software, no jumper setting is required for base address, DMA, and interrupt IRQ. Configuration is subject to change with every boot of the system as new PCI/PCIE Express® cards are added or removed.

Troubleshooting

If your system fails to boot or if you experience erratic operation with your PCI/PCIE Express card in place, an interrupt conflict may have been generated (such as when the BIOS Setup is incorrectly configured). Refer to the system's BIOS documentation for details.

2.3 Setting Board ID

When more than one data acquisition card is installed in the system, identification of specific cards can be a problem. The PCIe-7442 provides Board ID function, in which, according to settings of a DIP switch located in S1, ID is directly assigned to specific cards, providing error-free access to the card. Switch setting conditions are as shown, wherein 1= ON and 0 = OFF.



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Board ID	Switch			
	1	2	3	4
0	1	1	1	1
1	0	1	1	1
2	1	0	1	1
3	0	0	1	1
4	1	1	0	1
5	0	1	0	1
6	1	0	0	1
7	0	0	0	1
8	1	1	1	0
9	0	1	1	0
10	1	0	1	0
11	0	0	1	0
12	1	1	0	0
13	0	1	0	0
14	1	0	0	0
15	0	0	0	0

Table 2-1: Board ID Setting Conditions

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3 I/O Registers

3.1 About PCIe Controller Registers

The PCIe-7442 function library provides simple and easy-to-use functions to mange interrupt procedures. The functions eliminate the need to manipulate the interrupt register in the PCIe controller. It is recommended to use these functions to avoid the effort in developing all-new interrupt functions.

3.2 Isolated Digital Input Register

Status of the 64 isolated inputs is supplied by the four isolated input registers, with each bit corresponding to a channel. Bit value 1 indicates the input is ON and 0 OFF.

Address/W	R	Value Mapping [MSB (bit15)----LSB (bit0)]
BASE+0x02h	R	IDI [15…0]
BASE+0x04h	R	IDI [31...16]
BASE+0x42h	R	IDI [47...32]
BASE+0x44h	R	IDI [63...48]

3.3 COS Interrupt Control Registers

The two supported interrupt modes, disabled by default, enable interrupt when registers as listed are written. In the first mode, COS (Change of State) interrupt function monitors the status of enabled input channels and status changes from 0 to 1 or 1 to 0. In the second mode, the Watchdog Timer (WDT) counter is enabled. The interrupt asserts when the WDT Counter reaches zero. After processing the interrupt request event, interrupt request must be cleared to handle subsequent requests. Since an interval is required in which to clear the interrupt, COS or WDT interrupts preceding the previous interrupt that have not cleared will be ignored. To clear the interrupt request, write 1 to the corresponding bit (CLRn). The WDT INT control registers are as shown.

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The COS interrupt is enabled by two registers. Because the 64 digital inputs are divided into two 32-bit onboard buses, every 32 inputs are connected to a CPLD. When COS interrupt EA0 (BASE+0x06h) is enabled, the first CPLD (CPLD0) generates an interrupt signal when the first 32 inputs IDI [31..0] experience state change. When COS interrupt EA1 (BASE+0x46h) is enabled, the second CPLD (CPLD1) generates an interrupt signal when the second 32 inputs IDI[63..32] experience state change.

For COS interrupt EA1 (BASE+0x46h), Bits 15–9 and Bits 7–1 are unused, Bit0 CLR0: COS 0 interrupt clear is 1: Clear and 0: No effect, and Bit8 EA0: COS 0 interrupt enable/disable is 1: Enabled and 0: Disabled.

Address: BASE+0x06h
Reset Value: 0x0000h
Read/Write: W

--	--	--	--	--	--	--	CLR0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
--	--	--	--	--	--	--	EA0
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8

For COS interrupt EA1 (BASE+0x46h), Bits 15–9 and Bits 7–1 are unused, Bit0 CLR0: COS 0 interrupt clear is 1: Clear; 0: No effect, and Bit8 EA0: COS 0 interrupt enable/disable is 1: Enabled; 0: Disabled.

Address: BASE+0x46h
Reset Value: 0x0000h
Read/Write: W

--	--	--	--	--	--	--	CLR1
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
--	--	--	--	--	--	--	EA1
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8

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3.4 COS Setup/Latch Registers

Change of State (COS) interrupt is provided on any digital input channel, allowing status of digital input channels to be monitored by setting registers as follows.

Enabling COS Setup registers generates an interrupt when the corresponding channel changes its state.

For IDI_COS_EN [n]: Change-of-State function enable of IDI on channel n, n = 0 – 63, bit value 0 disables COS function and 1 enables.

Address	R/W	Value Mapping (MSB----LSB)
BASE+0x08h	W	IDI_COS_EN[15…0]
BASE+0x0Ah	W	IDI_COS_EN[31...16]
BASE+0x48h	W	IDI_COS_EN[47...32]
BASE+0x4Ah	W	IDI_COS_EN[63...48]

When COS occurs, the COS latch registers also latch the IDI[31..0], IDI[63..32] data, respectively. Once the interrupt request is cleared, the COS latch register automatically clears. Since these registers can be checked for post=interrupt status, the CPU is freed from the workload presented by constant polling of all inputs, enabling it to handle other tasks. With bit value 1, input is ON, and with 0, OFF (initial value).

Address	R/W	Value Mapping (MSB----LSB)
BASE+0x08h	R	IDI_COS_LATCH_DATA[15…0]
BASE+0x0Ah	R	IDI_COS_LATCH_DATA[31...16]
BASE+0x48h	R	IDI_COS_LATCH_DATA[47...32]
BASE+0x4Ah	R	IDI_COS_LATCH_DATA[63...48]

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Address: BASE+0x06h Reset Value: 0x0000h Read/Write: W							
--	--	--	--	--	--	--	CLR0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
--	--	--	--	--	--	--	EA0
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8

3.5 TTL I/O Setup, Status, DO, and DI Registers

An extra 32CH TTL I/O function is provided for optional applications. Divided between two 16-bit banks and between JP3 and JP4 connectors, they accommodate selection of direction for each TTL channel at any time via the two-bank TTL I/O setup register.

Address	R/W	Value Mapping (MSB----LSB)
BASE+0x0Ch	W	TTL_IO_SETUP[15…0]
BASE+0x4Ch	W	TTL_IO_SETUP[31..16]

When TTL I/O channel direction is set, status can be read back through TTL I/O Status Read Back Register to determine whether correct.

Address	R/W	Value Mapping (MSB----LSB)
BASE+0x0Ch	R	TTL_IO_STATUS[15…0]
BASE+0x4Ch	R	TTL_IO_STATUS[31...16]

When the I/O direction setting is output, data can be transmitted via TTL I/O output channel, with bit value 0 setting output low (default), and 1 high.

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Address	R/W	Value Mapping (MSB----LSB)
BASE+0x0Eh	W	TTL_IO_DO[15…0]
BASE+0x4Eh	W	TTL_IO_DO[31...16]

When the I/O direction setting is input, data can be read through the TTL I/O input channel, with bit value 0 setting input low and 1 high (initial value).

Address	R/W	Value Mapping (MSB----LSB)
BASE+0x0Eh	R	TTL_IO_DI[15…0]
BASE+0x4Eh	R	TTL_IO_DI[31...16]

Address	R/W	Value Mapping (MSB----LSB)
BASE+0x08h	W	IDI_COS_EN[15…0]
BASE+0x0Ah	W	IDI_COS_EN[31...16]
BASE+0x48h	W	IDI_COS_EN[47...32]
BASE+0x4Ah	W	IDI_COS_EN[63...48]

3.6 Isolated Digital Output and Read Back Registers

The 64 isolated digital outputs are divided between output connectors CN2A and CN2B, controlled by four 16-bit registers in bank2. Each digital output line is controlled by each bit of the four control registers. To complete the process, corresponding DO output data must be issued, followed by the start command to bank2. 64-bit DO data is transmitted at the same time. Output device type is Open Drain Power MOSFET driver. DO Send Out Start requires no register value, ony the transmission of the address (BASE + 0x88h) in Write mode after setup of all 64-bit channel output data. When back2 receives the Start command, 64-bit DO data is sent at the same time, and progress can be checked via nDO_SendReady flag status. Bit value 0 sets output Power MOSFET OFF (Initial value), and 1 ON.

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Address	R/W	Value Mapping (MSB----LSB)
BASE+0x80h	R	DO Read Back Start
BASE+0x82h	R	IDO[15…0]
BASE+0x84h	R	IDO[31...16]
BASE+0x86h	R	IDO[47...32]
BASE+0x88h	R	IDO[63...48]

3.7 Power-up DO Setup/Read Register

When the system powers up, the PCIe-7442 can initiate transmission of default initial value to 64CH digital outputs. The power-up default DO values can be configured and stored in flash memory, such that DO assumes a specified status at power up. Default 64CH power-up default DO values can be programmed via the Power-up DO Setup Register in turn. After access to the previous Power-up DO Setup Register (BASE+0x92h), it can take up to 0.5s to finish writing the procedure to the flash memory. It can be determined whether the procedure is complete via the nAction_Ready flag. Bit value: 0 sets Output Power MOSFET to OFF (Initial value), and 1 to ON.

Address	R/W	Value Mapping (MSB----LSB)
BASE+0x8Ch	W	IDO[15...0]
BASE+0x8Eh	W	IDO[31...16]
BASE+0x90h	W	IDO[47...32]
BASE+0x92h	W	IDO[63...48]

Configured initial power-up DO values stored in the flash memory can be reviewed by sending out the Read Start command (BASE+0x8Ch), after which read procedure starts in 50 ms. When the Read Back procedure is ready (nAction_Ready flag), the 64-bit Power-up DO Read Back Register can be read back in turn. Bit value: 0 sets Output Power MOSFET to OFF (Initial value), and 1 to ON.

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Address	R/W	Value Mapping (MSB----LSB)
BASE+0x8Ch	R	Read Back Start
BASE+0x8Eh	R	IDO[15…0]
BASE+0x90h	R	IDO[31...16]
BASE+0x92h	R	IDO[47...32]
BASE+0x94h	R	IDO[63...48]

3.8 Watchdog Timer Load, Safety DO Setup/Read Back Registers

In the 32-bit watch dog timer (WDT) with 10 MHz clock, the WDT counter loads the 32-bit value of two 16-bit WDT_LOAD_CONFIG registers in turn, where the corresponding user-defined hexadecimal value determines the overflow time of the WDT counter. Overflow time is calculated by the set value multiplied by 100 ns. Timer interval is from 0 to 429.496 seconds.

Address	R/W	Value Mapping (MSB----LSB)
BASE+0x94h	W	WDT_LOAD_CONFIG[15…0]
BASE+0x96h	W	WDT_LOAD_CONFIG[31...16]

When the WDT interrupt asserts, the system can be set to send out the Safety DO value via the SafetyOut_Enable bit. When WDT INT asserts, the system process may halt or be offline, in the event of which this function prevents untoward damage. Default 64CH safety DO values are stored in the flash memory. When WDT interrupt asserts and the SafetyOut_Enable bit is enabled, the PCIe-7442 enters the safety DO procedure which sends out the default safety value to 64CH digital outputs.

64CH safety default DO values can be programmed by accessing the previous WDTSafety DO Setup register in turn. After accessing the previous WDTSafety DO Setup register (BASE+0x9Eh), it takes 500 ms to finish writing the procedure to the flash memory. It can be determined whether the procedure is complete via

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nAction_Ready flag. Bit value: 0 sets Output Power MOSFET to OFF(Initial value), and 1 to ON.

Address	R/W	Value Mapping (MSB----LSB)
BASE+0x98h	W	IDO[15…0]
BASE+0x9Ah	W	IDO[31...16]
BASE+0x9Ch	W	IDO[47...32]
BASE+0x9Eh	W	IDO[63...56]

Configured Safety DO values stored in flash memory can be reviewed by sending out the WDTSafety DO ReadBack command (BASE+0x96h). The flash memory read procedure starts in 50 ms. The finished flag can be checked by nAction_Ready flag. After Read Back, the 64-bit WDTSafety DO Read Back registers can be reviewed in turn. Bit value: 0 sets Output Power MOSFET to OFF(Initial value) and 1 to ON.

Address	R/W	Value Mapping (MSB----LSB)
BASE+0x96h	R	Read Back Start
BASE+0x98h	R	IDO[15...0]
BASE+0x9Ah	R	IDO[31...16]
BASE+0x9Ch	R	IDO[47...32]
BASE+0x9Ch	R	IDO[63...56]

3.9 WDT INT Control, Hot-Reset, and Hold Control Register

The PCIe-7442 supports COS INT and watch dog timer (WDT) interrupt modes. When enabled, the WDT counts down as a mode of intrrupt, and is asserted when the counter reaches zero. WDT enable and clear WDT INT can be operated by setting two bits (WDTE and WIC) in Bank2 WDT INT Control/Hot-Reset Hold Control Register.

The PCIe-7442 also enhances industrial safety by, when the WDT interrupt asserts, issuing the Safety DO value to set the SOE bit

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and prevent possible system damage. According to user settings, when the system experiences unexpected or normal hot system reset without proper power down, the board can retain the original pre-rest DO values, or enter the power-up initial procedure to issue the previously configured default initial DO values. Setting the HRHE bit enables Hot_Reset_Hold function anytime, especially useful in unstable environments.

Bit functionality is as shown.

Address: BASE+0x8Ah **Reset Value: 0x0000h** **Read/Write: W**							
--	--	--	--	WSOE	WIC	WDTE	HRHE
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
--	--	--	--	--	--	--	--
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8

Bit	Function	1	0
0	HRHE: Hot Reset Hold Enable, enables hot-system-reset DO hold	Enabled	Disabled
1	WDTE: WDT interrupt enable/ disable	Enabled	Disabled
2	WIC: WDT interrupt clear	Clear WDT interrupt	No effect
3	WSOE: WDT Safety DO Send Out enable	Enabled	Disabled
4 to 15	Not Used	N/A	N/A

Address: BASE+0x8Ah **Reset Value: 0x0000h** **Read/Write: R**							
--	ARDYS	SRDYS	RBRDYS	SOES	WIS	WDTES	HRHES

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Address: BASE+0x8Ah **Reset Value: 0x0000h** **Read/Write: R**							
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
--	--	--	--	--	--	--	--
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8

Bit	Function	1	0
0	HRHES: Hot Reset Hold Enable Status	Enabled	Disabled
1	WDTES: WDT Interrupt Enable Status	Enabled	Disabled
2	WIS: WDT Interrupt Status	WDT interrupt does not assert	WDT interrupt asserts
3	SOES: Safety Out Enable Status	Enabled	Disabled
4	RBRDYS: DO Read Back Data Ready Status	Not ready	Ready
5	SRDYS: DO Data Sending Finished Status	Not finished	Finished
6	ARDYS: Flash Data Read/ Write Finished Status	Not finished	Finished
7 to 15	Not Used	N/A	N/A

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Important Safety Instructions

For user safety, please read and follow all instructions, Warnings, Cautions, and Notes marked in this manual and on the associated device before handling/operating the device, to avoid injury or damage.

S'il vous plaît prêter attention stricte à tous les avertissements et mises en garde figurant sur l'appareil , pour éviter des blessures ou des dommages.

- Read these safety instructions carefully
- Keep the User's Manual for future reference
- Read the Specifications section of this manual for detailed information on the recommended operating environment
- The device can be operated at an ambient temperature of 50ºC
- When installing/mounting or uninstalling/removing device; or when removal of a chassis cover is required for user servicing (See "Getting Started" on page 17.):
  - Turn off power and unplug any power cords/cables
  - Reinstall all chassis covers before restoring power
- To avoid electrical shock and/or damage to device:
  - Keep device away from water or liquid sources
  - Keep device away from high heat or humidity
  - Keep device properly ventilated (do not block or cover ventilation openings)
  - Always use recommended voltage and power source settings
  - Always install and operate device near an easily accessible electrical outlet
  - Secure the power cord (do not place any object on/over the power cord)
  - Only install/attach and operate device on stable surfaces and/or recommended mountings
- If the device will not be used for long periods of time, turn off and unplug from its power source

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- Never attempt to repair the device, which should only be serviced by qualified technical personnel using suitable tools
- A Lithium-type battery may be provided for uninterrupted backup or emergency power.



Risk of explosion if battery is replaced with one of an incorrect type; please dispose of used batteries appropriately.
Risque d'explosion si la pile est remplacée par une autre de type incorrect. Veuillez jeter les piles usagées de façon appropriée.

- The device must be serviced by authorized technicians when:
  - The power cord or plug is damaged
  - Liquid has entered the device interior
  - The device has been exposed to high humidity and/or moisture
  - The device is not functioning or does not function according to the User's Manual
  - The device has been dropped and/or damaged and/or shows obvious signs of breakage
- Disconnect the power supply cord before loosening the thumbscrews and always fasten the thumbscrews with a screwdriver before starting the system up
- It is recommended that the device be installed only in a server room or computer room where access is:
  - Restricted to qualified service personnel or users familiar with restrictions applied to the location, reasons therefor, and any precautions required
  - Only afforded by the use of a tool or lock and key, or other means of security, and controlled by the authority responsible for the location

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	**BURN HAZARD** Touching this surface could result in bodily injury. To reduce risk, allow the surface to cool before touching. ***RISQUE DE BRÛLURES*** *Ne touchez pas cette surface, cela pourrait entraîner des blessures.* *Pour éviter tout danger, laissez la surface refroidir avant de la toucher.*

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Getting Service

Ask an Expert: http://askanexpert.adlinktech.com

ADLINK Technology, Inc.
Address: 9F, No.166 Jian Yi Road, Zhonghe District
New Taipei City 235, Taiwan
新北市中和區建一路 166 號 9 樓
Tel: +886-2-8226-5877
Fax: +886-2-8226-5717
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
Address: 5215 Hellyer Avenue, #110
San Jose, CA 95138, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-360-0222
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203)
300 Fang Chun Rd., Zhangjiang Hi-Tech Park
Pudong New Area, Shanghai, 201203 China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1 Shang Di East Rd.
Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8626
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园
A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

LiPPERT ADLINK Technology GmbH
Address: Hans-Thoma-Strasse 11
D-68163 Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

PENTA ADLINK Technology GmbH
Ulrichsbergerstrasse 17
94469 Deggendorf, Germany
Tel: +49 (0) 991 290 94 – 10
Fax: +49 (0) 991 290 94 - 29
Email: emea@adlinktech.com

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

ADLINK Technology, Inc. (French Liaison Office)
Address: 6 allée de Londres, Immeuble Ceylan
91940 Les Ulis, France
Tel: +33 (0) 1 60 12 35 66
Fax: +33 (0) 1 60 12 35 66
Email: france@adlinktech.com

ADLINK Technology Japan Corporation
Address: 〒101-0045 東京都千代田区神田鍛冶町 3-7-4
神田 374 ビル 4F
KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
Chiyoda-ku, Tokyo 101-0045, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5209-6013
Email: japan@adlinktech.com

ADLINK Technology, Inc. (Korean Liaison Office)
Address: 경기도 성남시 분당구 수내로 46 번길 4 경동빌딩 2 층
(수내동 4-4 번지) (우) 463-825
2F, Kyungdong B/D, 4 Sunae-ro 46 beon-gil
Bundang-gu, Seongnam-si, Gyeonggi-do, Korea, 463-825
Toll Free +82-80-800-0585
Tel +82-31-786-0585
Fax +82-31-786-0583
Email: korea@adlinktech.com

ADLINK Technology Singapore Pte. Ltd.
Address: 84 Genting Lane #07-02A, Cityneon Design Centre
Singapore 349584
Tel: +65-6844-2261
Fax: +65-6844-2263
Email: singapore@adlinktech.com

ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)
Address: #50-56, First Floor, Spearhead Towers
Margosa Main Road (between 16th/17th Cross)
Malleswaram, Bangalore - 560 055, India
Tel: +91-80-65605817, +91-80-42246107
Fax: +91-80-23464606
Email: india@adlinktech.com

ADLINK Technology, Inc. (Israeli Liaison Office)
Address: 27 Maskit St., Corex Building
PO Box 12777
Herzliya 4673300, Israel
Tel: +972-54-632-5251
Fax: +972-77-208-0230
Email: israel@adlinktech.com

ADLINK Technology, Inc. (UK Liaison Office)
Tel: +44 774 010 59 65
Email: UK@adlinktech.com

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