PCIe-9842

200 MS/s 14-Bit 1-CH High-Speed PCI Express Digitizer

User's Manual

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1 Introduction

The ADLINK PCIe-9842 is 200MS/s 14-bit 1-CH digitizer designed for applications such as LIDAR tests, optical fiber tests and radar signal acquisition. The 100MHz bandwidth analog input is designed to receive ±1V high speed signal with 50Ω impedance. With this simplified front-end design and high stable onboard reference, PCIe-9842 provides not only high accuracy measurement results but also delivers high dynamic performance.

For applications that require data to be acquired and transferred in real-time, PCIe-9842 is designed on the PCI Express x4 bus as the interface. When signal is converted from analog to digital data, data will be transferred to host system memory continuously due to PCI Express high bandwidth features.

The auto-calibration function of the PCIe-9842 is performed with onboard reference circuit that calibrates the offset and gain errors of analog input. Once the auto-calibration procedure is done, the calibration constant will be stored in EEPROM such that these values can be loaded and used as needed by the board. Because all the calibration is conducted automatically by software commands, users don't have to calibrate the module manually.



Figure 1-1: PCIe-9842 Product Image

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1.1 Features

- Up to 200MS/s sampling rate
- High resolution 14-Bit ADC
- ±1V Input range with 50Ω input impedance and DC couple
- Up to 100 MHz bandwidth for analog input
- High dynamic performance, up to 70 dB SNR with 10 MHz sine input
- High-speed PCI Express x4 bus interface
- Scatter-Gather DMA data transfer for high speed data streaming
- Supports one external digital trigger input
- Digital trigger output to stimulus external instrument
- Supports auto-calibration

1.2 Applications

- Radar signal acquisition
- IF signal spectrum monitoring
- Optical fiber test
- Physics experiment and science research
- Cable fault location and partial discharge monitoring for power applications

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1.3 Specifications

1.3.1 Analog Input

Specification	Value
Number of Channels	1 single-ended channel
Connector	SMA Screw Type
Input Impedance	50Ω ± 2%
Input Coupling	DC
Input Signal Range	±1.0 V
Overvoltage Protection	±5 V
ADC Resolution	14 bits, 1 in 16,384
Offset Error	±1 mV
Gain Error	±0.5% of input
-3 dB Bandwidth	100MHz

Table 1-1: Analog Input

1.3.2 Timebase

Specification	Value
Sample Clock Source	Internal: onboard clock (oscillator)
Time base Frequency	200 MHz
Sampling Rate Range	200 MS/s - 3051.75 S/s
Internal Timebase Accuracy	<±25 ppm

Table 1-2: Timebase

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1.3.3 Triggers

Specifications	Value
Trigger Source	Software trigger
	External digital trigger
Trigger Mode	Post-Trigger, delay-trigger
	Re-trigger for all trigger modes
External Digital Trigger Input	
Compatibility	3.3 V TTL, 5 V tolerant
Input High Threshold (V_{IH})	2.0 V
Input Low Threshold (V_{IL})	0.8 V
Maximum Input Overload	-0.5 V to+5.5 V
Input Impedance	50 Ω
Trigger Condition	Rising edge or Falling edge, software programmable
Minimum Pulse Width	20 ns
Digital Trigger Output	
Compatibility	5 V TTL
Output High Threshold (VOH)	2.4 V
Output Low Threshold (VOL)	0.2 V
Trigger Output Polarity	Positive or Negative
	Software programmable
Trigger Output Pulse Width	(50ns, 100ns, 150ns, 200ns, 500ns, 1us, 2us, 7.5us and 10us) ± 10ns, software select-able
Trigger Output driving Capacity	Capable of driving a 50 ohm load

Table 1-3: Triggers

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1.3.4 Aux Digital I/O

Specification	Value
Aux DIO Function	Static DIO interface
	Synchronized digital input interface
IO Compatibility	3.3V TTL
Input Level High (VIH)	2.0V minimum
Input Level Low (VIL)	0.8V maximum
Output Level High (VOH)	2.4V minimum
Output Level Low (VOL)	0.2V maximum
Output Driving Capability	±12 mA
Aux DIO Function as Static IO	
Number of Channel	8-bit
Direction selection	Each bit can be programmed as input or output channels
Data Transfer	Polling, access through specific registers
Aux DIO Function as Synchronized Digital Input (SDI)	
Number of Input Channels	2-bit
Data Transfer	DMA, 2 SDI bits and ADC data are combined into one register and transferred to host PC by DMA. Refer to Chapter 3 for detail data format.

Table 1-4: Aux Digital I/O

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1.3.5 Data Memory

Specification	Value
Onboard Memory	16K samples
Data Transfer Type	Scatter-gather DMA transfer

Table 1-5: Data Memory

1.3.6 Onboard Reference

Specification	Value
Recommend Warm-Up Time	15 minutes
Reference Voltage	+5.000 V
Reference Temp. Coeff. ppm/°C	<±5.0 ppm/°C

Table 1-6: Onboard Reference

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1.3.7 General Information

Specification	Value	
Environment		
Operating Environment	Ambient temperature: 0°C to +50°C	
	Relative humidity: 10% to 90% non-condensing	
Storage Temperature	Ambient temperature: -20°C to +80°C	
	Relative humidity: 10% to 90% non-condensing	
Physical		
PCB Dimension (not including connector)	PCI-E: Standard PCI Express short length card	
	106.7 mm (H) X 174.6 mm(W)	
Bus Interface		
Bus Type	PCI Express x4	
Certification		
FCC	FCC 47 CFR Part 15 Subpart B, ICES-003 Issue 4, ANSI C63.4-2003	
CE/EMC	EN55022, EN61000-3-2, EN61000-3-3	
	EN55024, IEC 61000-4-2, IEC 61000-4-3, IEC 61000-4-4, IEC 61000-4-5, IEC 61000-4-6, IEC 61000-4-8, IEC 61000-4-11	
Power Requirements		
Power rails	**Standby Current (A)**	**Full Load Current (A)**
+12 V	218 mA	222 mA
+3.3 V	1.18 A	1.21 A

Table 1-7: General Information

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1.4 Software Support

1.4.1 Driver Information

ADLINK provides comprehensive software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environment such as LabVIEW® and MATLAB®. ADLINK also provides ActiveX component ware for measurement, and breakthrough proprietary software applications.

All software options are included in the ADLINK All-in-One CD.

Supported Operating System

- Windows 7/Vista/XP
- Linux

Recommended Application Environments

- VB.NET/VC.NET/VB/VC++/BCB

Driver Support

- DAQPilot for Windows
- DAQPilot for LabVIEW
- WD-DASK for Windows
- WD-DASK/X for Linux
- Toolbox adapter for MATLAB

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1.4.2 WD-DASK

The WD-DASK includes device drivers and DLL for Windows 98/ NT/2000/XP/Vista/Win7. DLL is binary compatible across Windows 98/ NT/2000/XP/Vista/Win. This means all applications developed with WD-DASK are compatible with these Windows operating systems. The developing environment may be VB, VC++, Delphi, BC5, or any Windows programming language that allows calls to a DLL. The WD-DASK user's and function reference manuals are in the ADLINK All-in-One CD. (\\Manual\Software Package\WD-DASK).

1.4.3 DAQPilot

DAQPilot is a driver and SDK with a graphics-driven interface for various application development environments. DAQPilot comes as ADLINK's commitment to provide full support to its comprehensive line of data acquisition products and is designed for the novice to the most experienced programmer.

As a task-oriented DAQ driver, SDK and wizard for Windows systems, DAQPilot helps you shorten the development time while accelerating your learning curve for data acquisition programming.

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Figure 1-2: DAQPilot

You can download and install DAQPilot at:
http://www.adlinktech.com/TM/DAQPilot.html

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1.4.4 DAQMaster

ADLINK DAQMaster is a smart device manager that opens up access to ADLINK data acquisition and test and measurement products. DAQMaster delivers all-in-one configurations and provides you with a full support matrix to properly and conveniently configure ADLINK Test and Measurement products.

As a configuration-based device manager for ADLINK DAQ cards, DAQMaster enables you to manage ADLINK devices and interfaces, install and upgrade software applications, and manage ADLINK DAQPilot tasks.

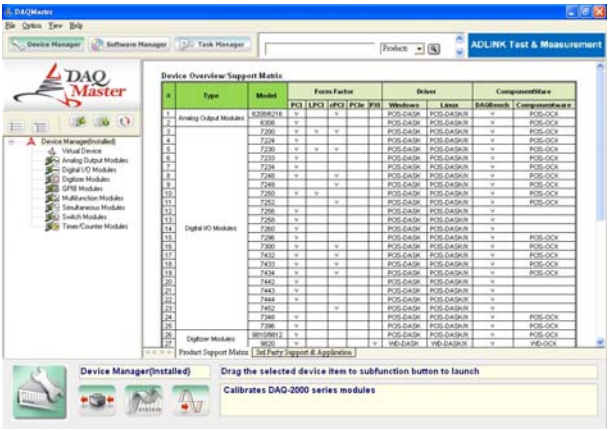


Figure 1-3: DAQMaster

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2 Getting Started

This chapter further describes the proper installation environment, installation procedures, its package contents and basic information users should be aware of.

Note: Diagrams and images of equipment illustrated are used for reference only. Actual system configuration and specs may vary.

2.1 Installation Environment

Whenever unpacking and preparing to install any equipment described in this manual, please refer to the Important Safety Instructions chapter of this manual.

Only install equipment in well lit areas on flat, sturdy surfaces with access to basic tools such as flat and cross head screwdrivers, preferably with magnetic heads as screws and standoffs are small and easily misplaced.

Recommended Installation Tools

- Phillips (cross-head) screwdriver
- Flat-head screwdriver
- Anti-static Wrist Strap
- Anti-static mat

The ADLINK PCIe-9842 digitizer cards are electro-static sensitive equipment that can be easily damaged by static electricity. The equipment must be handled on a grounded anti-static mat. The operator must wear an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the carton and packaging for damage. Shipping and handling could cause damage to the equipment inside. Make sure that the equipment and its associated components have no damage before installing.

Caution: The equipment must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the antistatic bag shipped with the product to handle the equipment and wear a grounded wrist strap when servicing.

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2.2 Package Contents

Before continuing, check the package contents for any damage and check if the following items are included in the packaging:

- PCIe-9842 Multi-function Data Acquisition Card
- ADLINK All-in-one Compact Disc
- Software Installation Guide
- PCIe-9842 User's Manual

If any of these items are missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

Warning:DO NOT install or apply power to equipment that is damaged or if there is missing/incomplete equipment. Retain the shipping carton and packing materials for inspection. Please contact your ADLINK dealer/vendor immediately for assistance. Obtain authorization from your dealer before returning any product to ADLINK.

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2.3 Device Layout and I/O Connectors

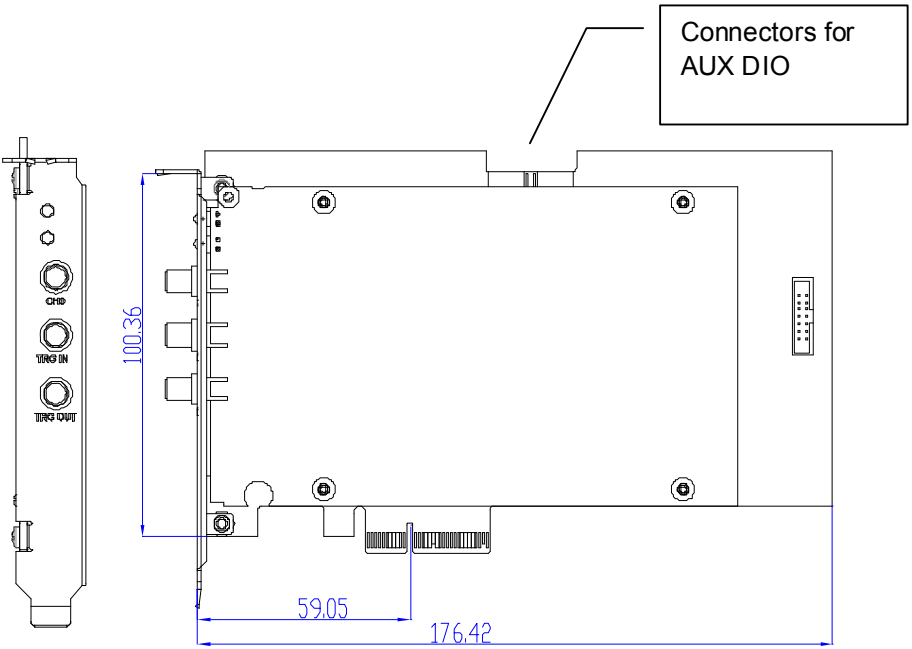


Figure 2-1: PCIe-9842 Mechanical Dimensions (units in mm)

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The connector types and functions are described as follows.

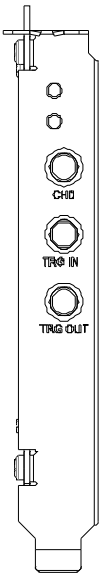
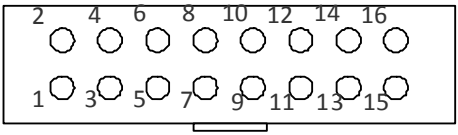
	Name	Mark on Faceplate	Type	Remark
	LED1	N/A	Green	ON status for card registered to system OFF Status for card released from system
	LED2	N/A	Blue	BLINK status for Acquisition on-going OFF status for Acquisition stop
	Analog Input channel	CH0	SMA Screw type	Analog input channel
	Ext. Digital Trigger Input	TRG IN		External digital trigger input. This channel receives trigger signal from external instrument and initial an acquisition procedure.
	Trigger Output	TRG OUT		Trigger output. Every time an acquisition begins, a pulse synchronized with timebase clock will assert and send output through this connector. The pulse width of the trigger output can be programmed from 50ns to 10us through software.

Table 2-1: Connector Types

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The PCIe-9842 includes a connector for auxiliary DIO functions. This digital IO port serves as two functions: general purpose DIO and synchronized DI. For more detail operation of AUX DIO function, please refer to Section 3. The following table depicts the pin define of this connector.



Legend	Pin	Pin	Legend
DIO0 / SDI0	1	2	GND
DIO1 / SDI1	3	4	GND
DIO2	5	6	GND
DIO3	7	8	GND
DIO4	9	10	GND
DIO5	11	12	GND
DIO6	13	14	GND
DIO7	15	16	GND

Table 2-2: Auxiliary Digital I/O

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2.4 Installing the Module

To install the card:

1. Turn off the system/chassis and disconnect the power plug from the power source.
2. Remove the system/chassis cover.
3. Select the PCI slot that you intend to use, then remove the bracket opposite the slot, if any.
4. Align the card connectors (golden fingers) with the slot, then press the card firmly until the card is completely seated on the slot.
5. Secure the card to the chassis with a screw.
6. Replace the system/chassis cover.
7. Connect the power plug to a power source, then turn on the system/chassis.

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3 Operation Theory

The operation theory of the PCIe-9842 is described in this chapter, including the control and setting of ADC sampling, trigger sources, trigger modes and data transfer.

3.1 Functional Block Diagram

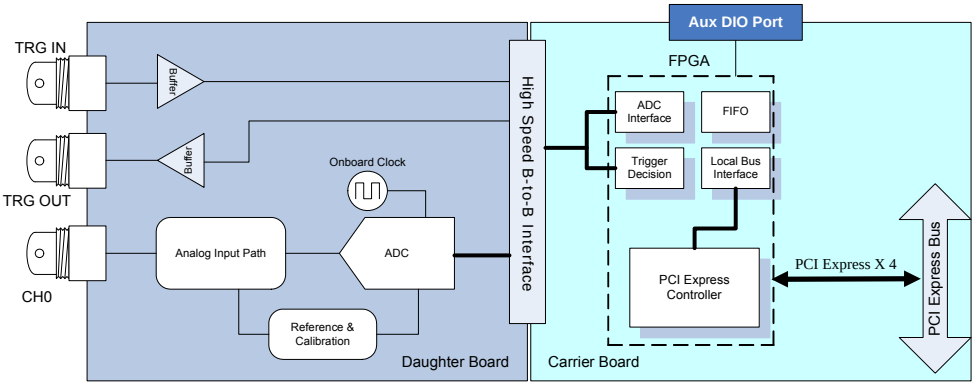


Figure 3-1: PCIe-9842 Block Diagram

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3.2 Basic AI Acquisition

In this section, we are going to explain the basic acquisition timing.

3.2.1 Analog Input Path

The following figure shows the block diagram of the analog input path of a digitizer. The input channel is terminated with 50 Ω input impedance. An anti-aliasing filter is adopted to eliminate high frequency noise which is higher than 100 MHz. The 14-bit ADC provides not only accurate DC performance but also high signal-to-noise ratio, high spurious-free dynamic range in AC performance. At last, the ADC data transfer to system memory via the high speed PCI Express x4 interface.

When perform auto-calibration, an internal calibration provide stable and accurate reference voltage to AI for calibration.

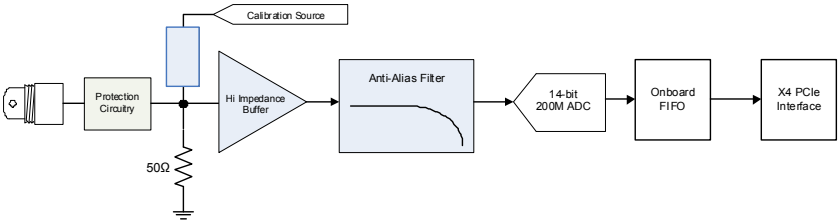


Figure 3-2: Analog Input Signal Path

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3.2.2 Basic Acquisition Timing

The PCIe-9842 begins acquisition process when it receives a trigger event. The trigger event comes from software command or external digital trigger. The Timebase is a clock that sent to the ADC and the acquisition engine for essential timing functionality. The Timebase is from onboard 200MHz oscillator. To achieve different sampling rate, a can interval counter is used.

Refer to Figure 3-3 and use post-trigger mode as an example. When a trigger is accepted by digitizer, the acquisition engine of the digitizer will begin to acquire data that coming from ADC and store these sampled data to onboard FIFO. When FIFO is not empty, data will be transferred to system memory immediately through the DMA engine. The sampled data is generated continuously at the rising edge of Timebase according to the scan interval counter setting. While sampled data reaches customer specified number, in this example is 256, the acquisition ends.

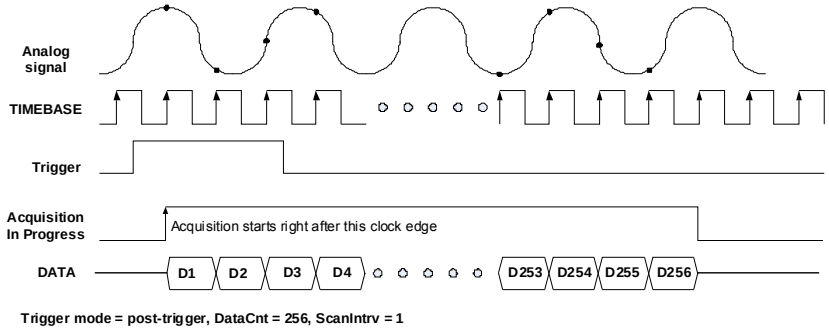


Figure 3-3: Basic Acquisition Timing of Digitizer

To achieve different sampling rate other than 200MS/s, user can specify a number for scan interval counter. For example, if you set the scan interval counter as 2, the equivalent sampling rate is 200MS/s / 2 = 100MS/s. If you set the scan interval counter as 3, the equivalent sampling rate is 200MS/s / 3 = 66.66MS/s, vice versa. Refer to Figure 3-4 for detail timing. The scan interval counter is 16-bit in width, therefore the lowest sampling rate is 3.051KS/s (200MS/s / 65535).

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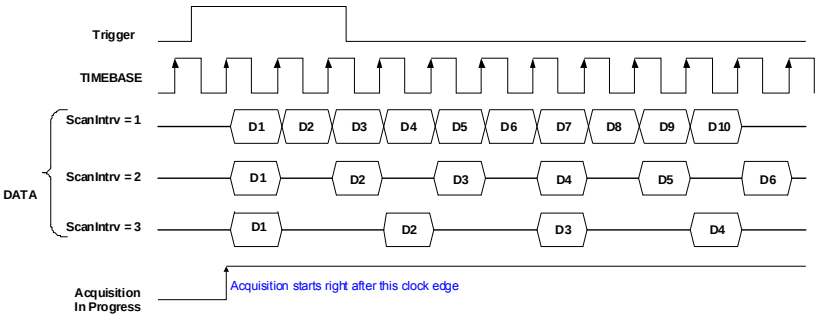


Figure 3-4: Different Sampling Rate by Setting Different Scan Interval Counters

Counter Name	Length	Valid Value	Description
ScanIntrv	16-bit	1 - 65535	**Scan Interval Counter** This counter is a Timebase divider to achieve equivalent sampling rate of digitizer. Sampling rate = Timebase / ScanIntrv
DataCnt	32-bit	1 - 536870911	**Data Counter** You can specify the amount of data to be acquired.
trigDelayTicks	16-bit	1 - 65536	**Delay Trigger Counter** The delay trigger counter is used to indicate the time between a trigger event and the start of an acquisition. The unit of a delay count is the period of the Timebase.
ReTrgCnt	31-bit	1 - 2147483648	**Re-Trigger Counter** The digitizer can enable re-trigger to accept multiple triggers. Refer to section 3.5.3 for more detail.

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3.2.3 AI Data Format

The ADC data of the PCIe-9842 is on the 14 MSB of the 16-bit A/D data. The 2 LSB of the 16-bit A/D data should be truncated by software when SDI function does not enable. When SDI function enabled, the 2 LSB, bit 0 and bit 1, represent the SDI0 and SDI1, respectively. Refer to following table for the A/D data structure with SDI enabled or disabled.

A/D data format with SDI Enabled								
D15	D14	D13	D12	……	D3	D2	D1	D0
D15 ~ D2 bits represent the data from ADC (2's complement) D1,D0 bits represent the status of SDI0 & SDI1, respectively								
A/D data format with SDI Disabled								
D15	D14	D13	D12	……	D3	D2	D1	D0
D15 ~ D2 bits represent the data form ADC (2's complement) D1, D0 bits should be truncated.								

Description	Analog Input Range	Digital Code (HEX)
Full-Scale Range	±1 V	
Least Significant Bit	122 µV	
FSR – 1 LSB	1.000 V	7FFC
Midscale + 1 LSB	0.000122 V	0001
Midscale	0 V	0000
Midscale – 1 LSB	-0.000122 V	FFFC
-FSR	-1.000 V	8004

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3.2.4 Synchronous Digital Input

The PCIe-9842 has two synchronous digital input channels, SDI0 an SDI1. These two digital input lines can be sampled synchronously with Timebase clock for mixed signal applications. Thus the data transfer can up to 200 Mbit/s when using internal 200 MS/s Timebase clock. These two digital input lines are combined with ADC data and located in 2 LSB when SDI function is enabled. Please refer to Figure 3-5 for more details.

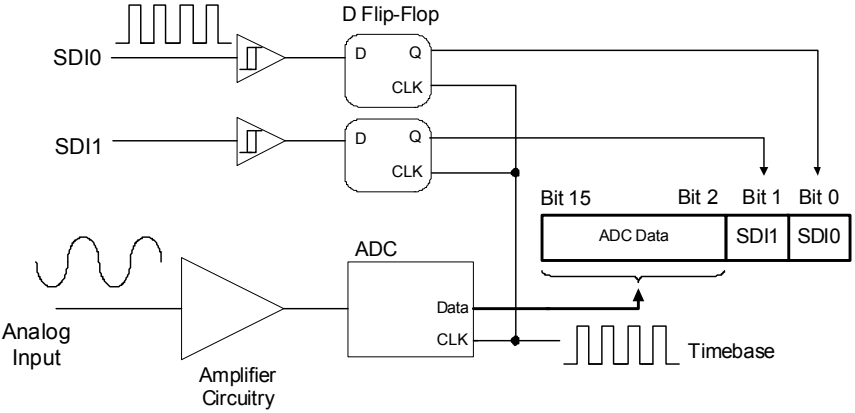


Figure 3-5: Synchronous Digital Input Operations

Note: When, the SDI function is enabled, the remaining DIO ports (DIO2-7) are invalid.

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3.3 Trigger Sources

The PCIe-9842 supports trigger signal from software command and external digital signal. When the PCIe-9842 receives a trigger, a sequence of acquisition operation begins.

A software trigger is generated by a software command through API. The trigger asserts right after executing the specific API function. Please refer to WD-DASK function reference manual for more detail operation.

An external digital trigger occurs when a TTL rising edge or a falling edge is detected at the SMA connector TRG IN on the front panel. As illustrated in following figure, the trigger polarity can be selected by software. Note that the signal level of the external digital trigger signal should be TTL-compatible, and the minimum pulse width is 20 ns.

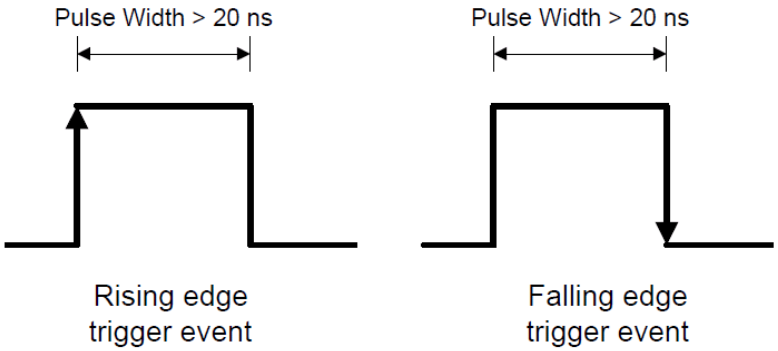


Figure 3-6: External Digital Trigger Polarity and Pulse Width Requirement

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3.4 Trigger Modes

There are two trigger modes working with trigger sources to initiate different data acquisition timing when a trigger event occurs: Post-Trigger and Delay-Trigger. The following sections describe these trigger modes in detail.

3.4.1 Post-Trigger Acquisition

Use post-trigger acquisition when you want to collect data after the trigger event, as illustrated in Figure 3-7. When the operation starts, PCIe-9842 waits for a trigger event. Once it receives the trigger signal, the acquisition begins. Data generates from ADC and being transferred to system memory continuously. The acquisition stops once when the total data amount reaches pre-defined number.

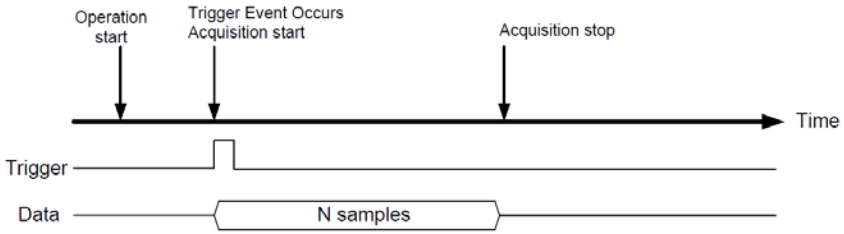


Figure 3-7: Post-Trigger Mode Operation

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3.4.2 Delay Trigger Acquisition

Use delay-trigger acquisition to delay the data collection after the trigger event, as illustrated in Figure 3-8. When PCIe-9842 receives trigger event, it waits a certain delay time and then begins acquisition. The delay time is specified by a 16-bit counter value so that the maximum delay time is the period of TIMEBASE X (2^{16} - 1), while the minimum delay is the period of Timebase.

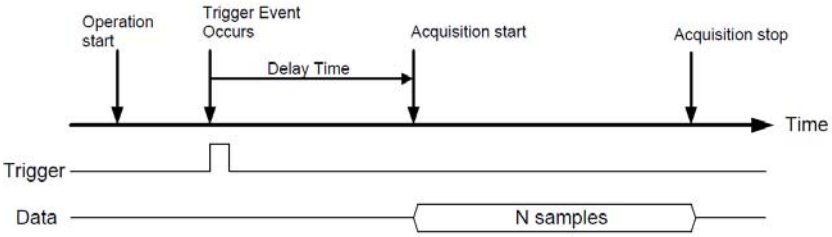


Figure 3-8: Delay-Trigger Mode Operation

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3.4.3 Post-Trigger or Delay-Trigger Acquisition with Re-Trigger

Use post-trigger or delay trigger acquisition with re-trigger function to collect data after several trigger events, as illustrated in Figure 3-9. You can program the number of triggers then the digitizer will acquire a specific sample data each time a trigger is accepted. Thus the time between last sampled data and next trigger event can be only one clock period of Timebase. After the initial setup, the process does not require software intervention.

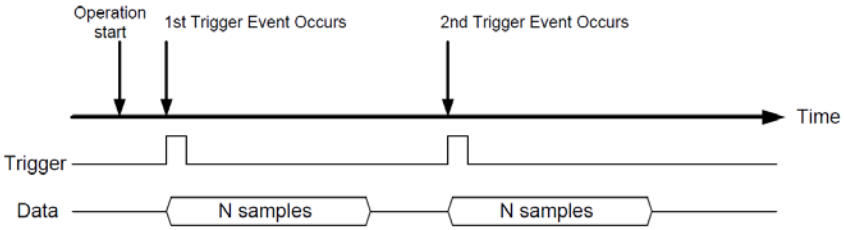


Figure 3-9: Re-Trigger Mode Operation

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3.5 Data Transfers

The PCI Express bus offers dedicated bandwidth of up to 250 MB/s. Unlike the PCI bus, which is a parallel bus architecture and divides bandwidth all devices on the bus, PCI Express is a peer-to-peer architecture and provides dedicated data pipeline. The data transfer can occur at 2.5 Gb/s, which enables theoretical 250 MB/s bandwidth per lane. With PCI Express, the data bandwidth is dramatically improved when compare to PCI bus. Data can be streamed to system faster and the amount of onboard memory can be reduced to minimum number.

One of the most important features of the PCIe-9842 is its PCI Express x4 interface. PCIe-9842 equips a 200MS/s high sampling rate ADC, it generates 400MByte data rate per second. Therefore it is very useful to have high bandwidth bus interface when streaming data from ADC to system memory.

The actual data throughput for a PC system will depend on the system topology, data transfers between other devices in the system and other components in the system. For example, data transfer between digitizers and host memory usually travel through a PCIe switch before transferring to host system. All digitizers share the bandwidth available on the link between PCIe switch and the host system.

To provide efficient data transfer, a PCI bus-mastering DMA is essential for continuous data streaming, as it helps to achieve full potential PCI Express bus bandwidth. The bus-mastering controller releases the burden of the host CPU since data are directly transferred to the host memory without intervention. Once analog input operation begins, the DMA returns control of the program. During DMA transfer, the hardware temporarily stores acquired data in the onboard AD Data FIFO, and then transfers the data to a user-defined DMA buffer in the computer.

By using a high-level programming library for high speed DMA data acquisition, users simply need to assign the sampling period and the number of conversions into their specified counters. After the AD trigger condition is met, the data will be transferred to the system memory by the bus-mastering DMA.

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In a multi-user or multi-tasking OS, such as Microsoft Windows, Linux, and so on, it is difficult to allocate a large continuous memory block. Therefore, the bus controller provides DMA transfer with scatter-gather function to link non-continuous memory blocks into a linked list so users can transfer large amounts of data without being limited by memory limitations. In non-scatter-gather mode, the maximum DMA data transfer size is 2 MB double words (8 MB bytes); in scatter-gather mode, there is no limitation on DMA data transfer size except the physical storage capacity of your system.

Users can also link descriptor nodes circularly to achieve a multi-buffered DMA. Figure 3-10 illustrates a linked list that is comprised of three DMA descriptors. Each descriptor contains a PCI address, PCI dual address, a transfer size, and the pointer to the next descriptor. PCI address and PCI dual address support 64-bit addresses which can be mapped into more than 4 GB of address space.

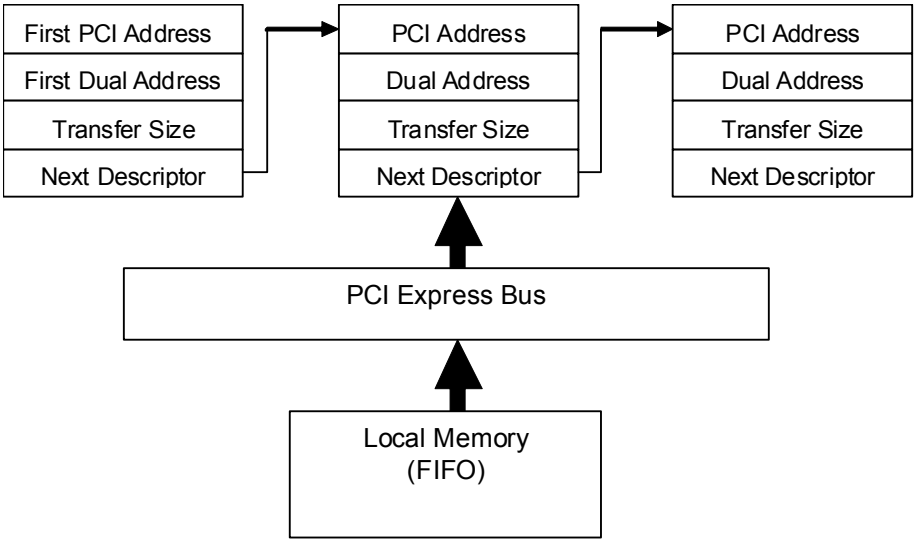


Figure 3-10: Data Transfers

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3.6 AUX DIO

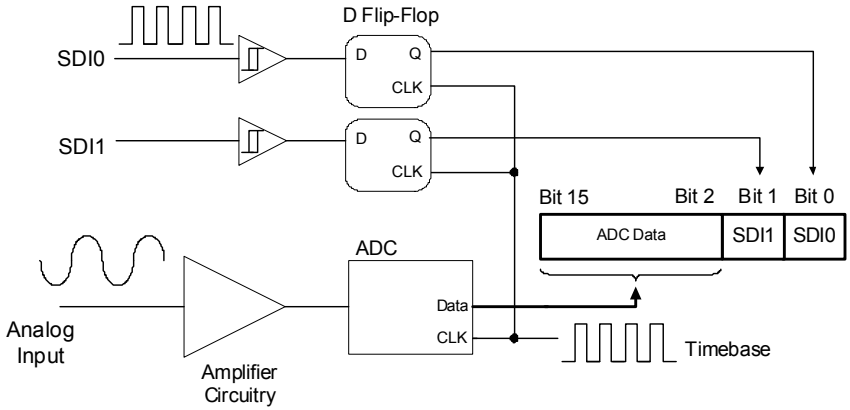
The PCIe-9842 features an auxiliary digital IO port. The auxiliary digital IO is software configurable for two functions:

General purpose digital IO

When configured as general purpose digital IO port, there are 8 digital lines for digital IO. Each line can be configured its direction as input or output by software. The data transfer of the general purpose digital IO is polling.

Synchronous digital input (SDI)

When configured as synchronous digital input, there are only two digital input lines available. These two digital input lines can be sampled synchronously with Timebase clock for mixed signal applications. Thus the data transfer can up to 200Mbit/s when using maximum sampling rate. These two digital input lines are combined with analog input channel. Please refer to following figure for more detail.



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4 Calibrations

This chapter introduces the calibration process to minimize analog input measurement errors and analog output errors.

4.1 Calibration Constant

The PCIe-9842 is factory calibrated before shipment by writing the associated calibration constants to the onboard EEPROM. Every time the system boot up, the PCIe-9842 driver will load these calibration constants that minimize the error in analog input path and analog output circuit. ADLINK provides a software API for calibrating the PCIe-9842 whenever users want to calibrate the module.

The onboard EEPROM provides four banks for calibration constant storage in PCIe-9842. The bank 0, which is the default bank, records the factory calibrated constants. Bank 0 is written protection that prevents any abnormal auto-calibration process occurred in user's environment. The banks 1, 2, and 3, which are user-defined spaces, provided for user's self-calibration constants. When user executes the auto-calibration process, the calibration constants will be recorded to bank 1, 2, and 3 based on user assignment.

When the PCIe-9842 boots up, the driver will access the calibration constants and set to hardware automatically. Without user's assignment, the driver will load constants stored in bank 0. If user wants to load constants from bank 1, 2, and 3, user can assign the bank 1, 2, and 3 as the boot up bank through software. Once user re-assigns the bank, driver will load the constants when user re-boot the system. This setting will be recorded to EEPROM and maintains no change until user modifies it.

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4.2 Auto-Calibration

Because errors in measurement and outputs will vary with time and temperature, it is recommended to re-calibration when the card is installed in the user's environment. The auto-calibration can measure and minimize errors without external signal connections, reference voltages, or measurement devices.

The PCIe-9842 has an on-board calibration reference to ensure the accuracy of auto-calibration. The reference voltage is measured on the production line and recorded in the on-board EEPROM. Before user begins the auto-calibration procedure, it is recommended to warm up the PCIe-9842 for at least 15 minutes. Please remove cables before an auto-calibration procedure is initiated.

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

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- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



RISK OF EXPLOSION IF BATTERY IS REPLACED BY AN INCORECT TYPE. DISPOSE OF USED BATTERIES ACCORDING TO THEIR INSTRUCTIONS.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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