PXI-2020/2022

8/16-CH 16-Bit 250 KS/s
Simultaneous Sampling Card
User's Manual

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Getting Service from ADLINK

Contact us should you require any service or assistance.

ADLINK Technology, Inc.
Address: 9F, No.166 Jian Yi Road, Chungho City,
Taipei County 235, Taiwan
台北縣中和市建一路 166 號 9 樓
Tel: +886-2-8226-5877
Fax: +886-2-8226-5717
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-360-0222
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203)
300 Fang Chun Rd., Zhangjiang Hi-Tech Park,
Pudong New Area, Shanghai, 201203 China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1, B/D
Shang Di East Rd., Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8625
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园
A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7,
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

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ADLINK Technology (Europe) GmbH
Address: Nord Carree 3, 40477 Duesseldorf, Germany
Tel: +49-211-495-5552
Fax: +49-211-495-5557
Email: emea@adlinktech.com

ADLINK Technology, Inc. (French Liaison Office)
Address: 15 rue Emile Baudot, 91300 Massy CEDEX, France
Tel: +33 (0) 1 60 12 35 66
Fax: +33 (0) 1 60 12 35 66
Email: france@adlinktech.com

ADLINK Technology Japan Corporation
Address: 151-0072 東京都渋谷区幡ヶ谷
1-1-2 朝日生命幡ヶ谷ビル 8F
Asahiseimei Hatagaya Bldg. 8F
1-1-2 Hatagaya, Shibuya-ku, Tokyo 151-0072, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5333-6040
Email: japan@adlinktech.com

ADLINK Technology, Inc. (Korean Liaison Office)
Address: 서울시 서초구 서초동 1506-25 한도 B/D 2 층
2F, Hando B/D, 1506-25, Seocho-Dong, Seocho-Gu,
Seoul 137-070, Korea
Tel: +82-2-2057-0565
Fax: +82-2-2057-0563
Email: korea@adlinktech.com

ADLINK Technology Singapore Pte. Ltd.
Address: 84 Genting Lane #07-02A, Cityneon Design Centre,
Singapore 349584
Tel: +65-6844-2261
Fax: +65-6844-2263
Email: singapore@adlinktech.com

ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)
Address: No. 1357, "Anupama", Sri Aurobindo Marg, 9th Cross,
JP Nagar Phase I, Bangalore - 560078, India
Tel: +91-80-65605817
Fax: +91-80-22443548
Email: india@adlinktech.com

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1 Introduction

ADLINK's PXI-2020/2022 are simultaneous-sampling multi-function DAQ cards to meet a wide range of application requirements for PXI systems. The devices can simultaneously sample 8/16 AI channels with differential input configurations in order to achieve maximum noise elimination. If more analog input channels are required, multiple cards can be synchronized through the PXI Trigger bus. The PXI-2020/2022 feature digital triggering, 4-CH programmable digital I/O lines, and 2-CH 32-bit general-purpose timer/counter. The auto-calibration functions adjust the gain and offset to be within specified accuracies such that you do not have to adjust trim pots to calibrate the cards.

Flexible Triggering

The PXI-2020/2022 feature flexible triggering options such as a software trigger, external digital trigger and triggers from the PXI Star trigger and trigger bus. These versatile trigger sources allow you to configure the PXI-2020/2022 to fit your application needs. Post-trigger, delay-trigger, pre-trigger and middle-trigger modes are also available to acquire data around the trigger event. The PXI-2020/2022 also feature repeated trigger acquisition, so you can acquire data in multiple segments with successive trigger events at extremely short rearming intervals.

Multiple-Module Synchronization

The versatile trigger options provided by the PXI backplane allow the PXI-2020/2022 to achieve multi-module synchronization in a simplified way. Utilizing the PXI Trigger bus, the PXI-2020/2022 can output trigger signals and the timebase to the PXI trigger bus when configured as a master, or receive trigger signals and the timebase from the PXI trigger bus when configured as a slave. Moreover, when the PXI-2020/2022 are plugged into a peripheral slot of a PXI system, they can also receive triggers or the timebase from the PXI Star trigger controller slot. The precision 10 MHz clock that comes from the PXI backplane can also be used as one of the timebase sources. Combining these PXI trigger features with the interface of the PXI-2020/2022 makes it very easy to synchronize multiple modules.

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Calibration

The PXI-2020/2022 includes a precision on-board reference with very low temperature drift. This feature not only provides a stable calibration source for auto-calibration but also maintains stable acquisition accuracy over a wide temperature range. The automated calibration process can be done through software without need for any manually adjustments. Once the calibration process has completed, the calibration information will be stored in the on-board EEPROM so that the values can be loaded and used as needed by the board.

1.1 Features

The PXI-2020/2022 Simultaneous Data Acquisition Card provides the following advanced features:

- Supports 3.3V and 5V PCI signal
- PXI specification Rev 2.2 compliant
- 8/16-CH differential analog inputs
- Bipolar analog input
- Programmable gains of x1, x4
- Scatter gather DMA transfer for AI continuously data acquisition
- 4-CH TTL digital input/output
- 2-CH 32-bit general purpose timer/counters
- Digital triggering
- Fully auto calibration
- Multiple cards synchronization through PXI trigger bus
- Onboard 16 K sample memory for data storage

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1.2 Applications

- Automotive Testing
- Cable Testing
- Transient signal measurement
- ATE
- Laboratory Automation
- Biotech measurement

1.3 Specifications

Basic Specifications

Analog Input[1]		
Model Number	PXI-2020	PXI-2022
Number of channels: (pro-grammable)	8 differential	16 differential
A/D converter :	AD7685 or equivalent	
Maximum sampling rate:	250 kS/s (each channel)	
Resolution:	16 bits	
Input coupling:	DC	
Programmable input range:	±10V, ±2.5V	
Operational common mode voltage range:	±8V	
Overvoltage protection:	Power on: Continuous ±30V	
	Power off: Continuous ±30V	
FIFO buffer size:	16 K samples (8192 x 32 bits)	
Data transfers:	Polling Mode, Bus-mastering DMA with scatter/gather	
Input impedance	1 GΩ	
Trigger mode:	Pre-Trigger, Post-Trigger, Middle-Trigger, Delay-Trigger	
Time-base source	Internal 80Mhz	

Table 1-1: Basic Specifications

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Triggers

Trigger Specifications	
Model Name	PXI-2020/2022
Trigger Sources (refer to section 4.4 for details)	(1)Software (2)AFI [0..7] (3)PXI Star Trigger (4)PXI Trigger Bus[5] (SSI) (5)SMB Trigger I/O (please refer to chapter 2.3 for details) *GA 3-8 can use (1), (2), (4), (5) as output signals. GA2 can use all options.
Trigger Mode	Pre-Trigger, Post-Trigger, Middle-Trigger, Delay-Trigger
AFI (Auxiliary Function Interface)	
Number of Channel	8 input/output (refer to pin legend definition)
Compatibility	Output 3.3 V TTL
Input Logic Levels	Input low voltage: 0.8 V (max) Input high voltage: 2.0 V(min)
Output Logic Levels	Output low voltage: 0.4 V (max) Output high voltage: 2.8 V (min)
Output Driving Capacity	±24 mA
Maximum Input Overload	-0.5 V to +5.5 V
Trigger Condition	Rising or Falling, software selectable
Minimum Pulse Width	12.5 ns
Power-on State	Input, pull-low with 10KΩ resistor
Data Transfer	Polling mode
PXI Star Trigger	
Receive Trigger from	PXI Star Trigger
Compatibility	Output 3.3 V TTL
Pulse Duration	12.5 ns
Pulse Logic	Rising or Falling edge, software selectable
PXI Trigger Bus[0..7]	
Receive Trigger from	PXI Trigger Bus line 5
Compatibility	Input 3.3 V or 5 V TTL Output 3.3 V TTL
Pulse Duration	12.5 ns
Pulse Logic	Rising or Falling edge, software selectable

Table 1-2: Triggers

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Digital I/O

Digital I/O Specifications	
Model Name	PXI-2020/2022
Number of Channel	4 input/output
Compatibility	Input 3.3 V or 5 V TTL Output 3.3 V TTL
Input Logic Levels	Input low voltage: 0.8 V (max) Input high voltage: 2.0 V(min)
Output Logic Levels	Output low voltage: 0.4 V (max) Output high voltage: 2.8 V (min)
Output Driving Capacity	±24 mA
Power-on State	Input, pull-low with 10KΩ resistor
Data Transfer	Polling mode

Table 1-3: Digital I/O

General Purpose Timer/Counter (GPTC)

General Purpose Specifications	
Model Name	PXI-2020/2022
Number of Channels	2 up/down counter/timers (by AFI)
Resolution	32-bit
Compatibility	Input 3.3 V or 5V TTL Output 3.3 V TTL
Base clock available	20 MHz
Data Transfer	Polling mode

Table 1-4: General Purpose Timer/Counter

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Timebase System

Timebase Specifications	
Model Name	PXI-2020/2022
Timebase Source	(1) Internal: onboard 80MHz oscillator (2) External from hardware IO
Sampling Rate Range	Timebase divided by 32-bit counter. TIMEBASE(80MHz) divider to the achieve equivalent sampling rate of DAQ. The equation is: Sampling rate = TIMEBASE / ScanIntrv The value of TIMEBASE depends on the card type. Take PXI-2022 (250KS/s) as an example, the ScanIntrv = 320 results in 250KS/s and ScanIntrv = 640 results in 125KS/s, and so on.
Internal Timebase Accuracy	<±25ppm (typical)
External Timebase Clock	
Sources (External from hardware IO) (refer to section 4.3 for details)	(1) PXI_10M (2) AFI [0..7] (3) PXI Trigger BUS[0] (4) PXI Star Trigger (5) SMB_CLK
Dedicate External Clock Input From IO Connector	
Clock Type	Digital TTL
Input Frequency Range	1MHz ~ 20MHz
Input Coupling	DC
Input Compatibility	Input 3.3V or 5V TTL

Table 1-5: Timebase System

Auto Calibration

Auto Calibration Specifications	
Model Name	PXI-2020/2022
Onboard reference	+5.000 V
Recommended warm-up time:	15 minutes
Temperature drift	±3 ppm°C (ADR02 5V Reference Chip)
Stability	50 ppm/1000hrs (ADR02 5V Reference Chip)

Table 1-6: Auto Calibration

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General

General Specifications	
Model Name	PXI-2020/2022
Dimensions	Single 3U PXI module, 100mm by 160mm (not including connector)
Connector	68-pin VHDCI-type female
Operating Environment	Ambient temperature: 0 to 55°C Relative humidity: 10% to 90% non-condensing
Storage Environment	Ambient temperature: -20 to 80°C Relative humidity: 5% to 95% non-condensing

Table 1-7: General

Power Requirements

Power Specifications	
Model Name	PXI-2020/2022
+3.3 V	1.5 A (typical)
+5 V	1.3 A (typical)
+12 V	0.35 A (typical)

Table 1-8: Power Requirements

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1.4 Performance

Analog Input Measurement[1]	
Model Number	PXI-2020/2022
Function	Result under 25°C ± 5°C
Offset Error (gain = 1)	±0.6 mV (Typical)
Gain Error (gain = 1)	±0.02% (Typical)
–3dB small signal bandwidth	gain = 1 : 1 MHz gain = 4 : 700 KHz
System Noise	gain = 1 : 0.5 mVrms gain = 4 : 0.2 mVrms
CMRR*(2) (DC)	gain = 1 : 80 dB gain = 4 : 80 dB
Spurious-free dynamic range (SFDR)	87 dB
Signal-to-noise and distortion ratio (SINAD)	82 dB
Total harmonic distortion (THD)	–85 dB
Signal-to-noise ration (SNR)	84 dB
Effective number of bits (ENOB)	13.3 bits

Table 1-9: Performance

Notes for Table 1-9:

SFDR, SINDA, THD, SNR, ENOB Data are based on below condition

- ▷ Gain = 1
- ▷ 0.9803771 KHz input tone, 18 Vpp input amplitude, 257 Sine waves, 65536 points
- ▷ 9.99832 KHz input tone, 18 Vpp input amplitude, 2621 Sine waves, 65536 points

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2 Getting Started

This chapter describes the proper installation environment, installation procedures, its package contents and basic information user should be aware of. The PXI-2020/2022 performs an automatic configuration of the IRQ, and port address. The PCI_SCAN software utility can be used to read the system configuration.

NOTE: Diagrams and images of equipment mentioned are used for reference only. Actual system configuration and specs may vary.

2.1 Installation Environment

Whenever unpacking and preparing to install any equipment described in this manual, please refer to the Important Safety Instructions chapter of this manual. Only install equipment in well lit areas on flat, sturdy surfaces with access to basic tools such as flat and cross head screwdrivers, preferably with magnetic heads as screws and standoffs are small and easily misplaced.

Recommended Installation Tools

- Philips (cross-head screwdriver)
- Flat-head screwdriver
- Anti-static wrist strap
- Anti-static mat

The PXI-2020/2022 contains several electro-static sensitive components that can be easily be damaged by static electricity. The equipment should be handled on a grounded anti-static mat and the operator should wear an anti-static wristband during the unpacking and installation procedure. Please also inspect the components for apparent damage. Improper shipping and handling may cause damage to the components. Be sure this is no shipping and handling damage on the components before continuing. CAUTION The equipment must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the equipment and wear a grounded wrist strap when servicing.

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2.2 Package Contents

Before continuing, check the package contents for any damage and check if the following items are included in the packaging:

- PXI-2020/2022 Simultaneous Data Acquisition Card
- ADLINK All-in-one DVD
- Software Installation Guide
- PXI-2020/2022 User's Manual.

Caution Do not install or apply power to equipment that is damaged or if there is missing/incomplete equipment. Retain the shipping carton and packing materials for inspection. Please contact your ADLINK dealer/vendor immediately for assistance. Obtain authorization from your dealer before returning any product to ADLINK.

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2.3 Mechanical Drawing and I/O Connectors

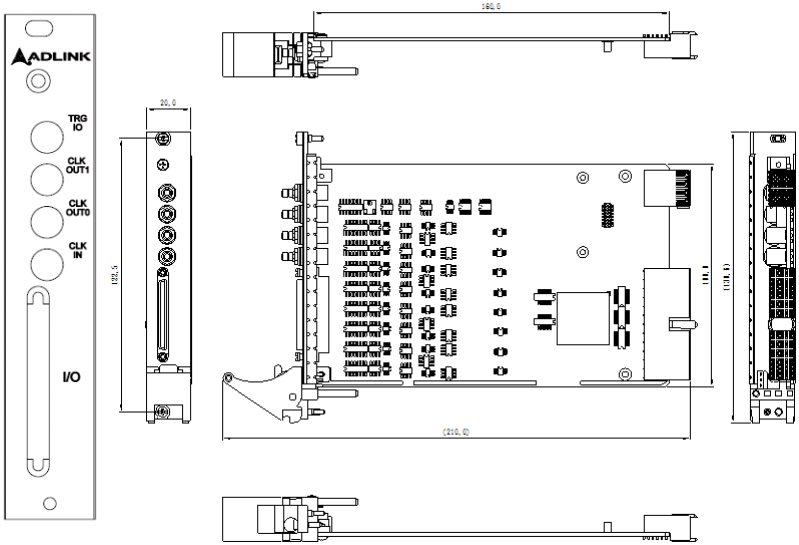


Figure 2-1: PXI-2020/2022 PCB Layout

The ADLINK PXI-2020/2022 is packaged in a Euro-card form factor compliant with PXI specifications measuring 160 mm in length and 100 mm in height (not including connectors). The connector types and functions are described as follows.

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SMB Connector

- SMB Connector 1: TRG IO
- SMB Connector 2: Sync CLK_OUT1
- SMB Connector 3: Sync CLK_OUT0
- SMB Connector 4: CLK IN

Connector	Direction	Type	Description/Function
TRG IO	Input Output	SMB	The TRG IO is a bidirectional port for external digital trigger input or output.
CLK OUT1	Output	SMB	The CLK OUTOUT 1 is a 50Ω, DC-coupled output; CLK_OUT0 and CLK_OUT1 is from the same source.
CLK OUT0	Output	SMB	The CLK OUTPUT 0 is a 50Ω, DC-coupled output; CLK_OUT0 and CLK_OUT1 is from the same source.
CLK IN	Input	SMB	The CLK IN is a 50Ω, AC-coupled external time-base input.

Table 2-1: SMB Connector

TRG IO, as an Input Port	
Connector type	SMB
Compatibility	3.3 V LVTTL(Low Voltage), 5 V tolerant
Input Logic Level	Input Low voltage: 0.8V (max) Input high voltage: 2.0 (min)
Maximum Input Overload	-0.5 V to +5.5 V
Trigger Polarity	Rising edge or falling edge (Software programmable)
Minimum Pulse Width	12.5 ns

Table 2-2: TRG IO, as an Input Port

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TRG IO, as an Output Port	
Connector type	SMB
Compatibility	3.3 V TTL
Output Logic Level	Output low voltage: 0.2 V (max)
	Output high voltage: 2.4 V (min)
Driving Capability	8 mA
Minimum Output Pulse Width	12.5 ns

Table 2-3: TRG IO, as an Output Port

CLK IN (External Clock from Front Panel)	
Connector Type	SMB
Clock Type	Sine wave or square wave
Input Impedance	50 Ω
Input Coupling	AC
Input Range	1 VP-P to 2 VP-P
Overvoltage Protection	2.5 VP-P

Table 2-4: CLK IN

CLK OUT0/OUT1, as an Output Port	
Connector Type	SMB
Clock Type	square wave
Compatibility	3.3 V TTL
Output Logic Level	Output low voltage: 0.2 V (max)
	Output high voltage: 2.4 V (min)
Driving Capability	24 mA
Output Impedance (for minimum load)	50 Ω

Table 2-5: CLK OUT0/OUT1, as an Output Port

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2.4 Installing the module

To install the PXI-2020/2022 module:

1. Turn off the PXI system/chassis and disconnect the power plug from the power source.
2. Align the module's edge with the card guide in the PXI chassis.
3. Slide the module into the chassis, until resistance is felt from the PXI connector.
4. Push the ejector upwards and fully insert the module into the chassis.
5. Once inserted, a "click" can be heard from the ejector latch.
6. Tighten the screw on the front panel.
7. Power on the PXI system/chassis.

To remove the module, reverse step 2 through 6 above.

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2.5 Software Support

ADLINK provides comprehensive software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environment such as LabVIEW® and MATLAB®. ADLINK also provides ActiveX component ware for measurement and SCADA/HMI, and breakthrough proprietary software applications. All software options are included in the ADLINK All-in-One DVD.

Programming Library

For customers who are writing their own programs, we provide function libraries for many different operating systems, including:

D2K-DASK:

Include device drivers and DLL for Windows 98/NT/2000/XP/Vista/7. DLL is binary compatible across Windows 98/NT/2000/XP/Vista/7. This means all applications developed with D2K-DASK are compatible across Windows 98/NT/2000/XP/Vista/7. The developing environment can be VB, VC++, Delphi, BCB6, or any Windows programming language that allows calls to a DLL. The user's guide and function reference manual of D2K-DASK are in the CD.

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2.6 PCI Configuration

1. Plug and Play:
   As a plug and play component, the card requests an interrupt number via its PCI controller. The system BIOS responds with an interrupt assignment based on the card information and on known system parameters. These system parameters are determined by the installed drivers and the hardware load seen by the system.

2. Configuration:
   The board configuration is done on a board-by-board basis for all PCI boards on your system. Because configuration is controlled by the system and software, there is no jumper setting required for base-address, DMA, and interrupt IRQ.
   The configuration is subject to change with every boot of the system as new boards are added or removed.

3. Trouble shooting:
   If your system doesn't boot or if you experience erratic operation with your PCI board in place, it's likely caused by an interrupt conflict (perhaps the BIOS Setup is incorrectly configured). In general, the solution, once you determine it is not a simple oversight, is to consult the BIOS documentation that comes with your system.

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3 Signal Connections

This chapter describes the connectors of the PXI-2020/2022, and the signal connection between the PXI-2020/2022 and external devices.

3.1 Connectors Pin Assignment

The PXI-2020/2022 is equipped with one 68-pin VHDCI-type connector (ACL-10568-1). It is used for digital input/output, analog input, and ti-mer/counter signals, etc. The pin assignments of the connectors are de-fined in Table 3-1 and Figure 3-2.

Connector Pin Assignment

	Pin #	Pin #	
DGND	34	68	DGND
DIO1	33	67	DIO0
DIO3	32	66	DIO2
DGND	31	65	AFI0/AD TRIG Out
AFI1/AD TIMER OUT	30	64	AFI2/GPTC_CLK0
DGND	29	63	AFI3/GPTC_GATE0
AFI4/GPTC_CLK1	28	62	AFI5/GPTC_GATE1
AFI6/GPTC_Out1	27	61	AFI7/GPTC_Out0
NC	26	60	NC
NC	25	59	NC
AIL0	24	58	AIH0
AIL8	23	57	AIH8
AGND	22	56	AGND
AIL1	21	55	AIH1
AIL9	20	54	AIH9
AGND	19	53	AGND
AIL2	18	52	AIH2
AIL10	17	51	AIH10
AGND	16	50	AGND
AIL3	15	49	AIH3

Table 3-1: PXI-2020/2022 68-pin VHDCI-type Pin Assignment

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AIL11	14	48	AIH11
AGND	13	47	AGND
AIL4	12	46	AIH4
AIL12	11	45	AIH12
AGND	10	44	AGND
AIL5	9	43	AIH5
AIL13	8	42	AIH13
AGND	7	41	AGND
AIL6	6	40	AIH6
AIL14	5	39	AIH14
AGND	4	38	AGND
AIL7	3	37	AIH7
AIL15	2	36	AIH15
AGND	1	35	AGND

Table 3-1: PXI-2020/2022 68-pin VHDCI-type Pin Assignment

Legend:

Pin #	Signal Name	Reference	Direction	Description
58, 55, 52, 49, 46, 43, 40,37, 57, 54, 51, 48, 45, 42, 39, 36	AIH <0..15>	AIL <0..15>	Input	Differential positive input for AI channel <0..15>
29, 31, 34, 68,	DGND	--------	--------	Digital ground
24, 21, 18, 15, 13, 9, 6, 3, 23, 20, 17, 14, 11, 8, 5, 2	AIL <0..15>	--------	Input	Differential negative input for AIL channels <0..15>
1, 4, 7, 10, 13, 16, 19, 22, 35, 38, 41, 44, 47, 50, 53, 56	AGND	--------	--------	Analog ground for AI
65	AFI0	DGND	In-put/Output	Auxiliary Function Input 0 (AD_TRIG_SRC0, AD TIMER_SRC0, AD_CONV_SRC0)/AD TRIG Out
30	AFI1	DGND	In-put/Output	Auxiliary Function Input 1 (AD_TRIG_SRC1, AD_ TIMER_SRC1, AD_CONV_SRC1)/(AD SAMPLE CLK Out)

Table 3-2: 68-pin VHDCI-type Connector Legend

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Pin #	Signal Name	Reference	Direction	Description
64	AFI2	DGND	Input	Auxiliary Function Input 2 (AD_TRIG_SRC2,AD_TIMER_SRC2,AD_CONV_SRC2)/(GPTC_CLK0)
63	AFI3	DGND	Input	Auxiliary Function Input 3 (AD_TRIG_SRC3,AD_TIMER_SRC3,AD_CONV_SRC3)/(GPTC_GATE0)
28	AFI4	DGND	Input	Auxiliary Function Input 4 (AD_TRIG_SRC4,AD_TIMER_SRC4,AD_CLK_SRC4)/(GPTC_CLK1)
62	AFI5	DGND	Input	Auxiliary Function Input 5 (AD_TRIG_SRC5,AD_TIMER_SRC5,AD_CONV_SRC5)/(GPTC_GATE1)
27	AFI6	DGND	In-put/Output	Auxiliary Function Input 6 (AD_TRIG_SRC6,AD_TIMER_SRC6,AD_CLK_SRC6)/(GPTC_OUT1)
61	AFI7	DGND	In-put/Output	Auxiliary Function Input 7 (AD_TRIG_SRC7,AD_TIMER_SRC7,AD_CLK_SRC7)/(GPTC_OUT0)
67, 33, 66, 32	DIO<0..3>	DGND	In-put/Output	Programmable DIO pins
25, 26, 59, 60	NC	DGND	--------	--------

Table 3-2: 68-pin VHDCI-type Connector Legend

Note: Pins 2, 5, 8, 11, 14, 17, 20, 23, 36, 39, 42, 45, 48, 51, 54, and 57 are NC for the PXI-2020.

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3.2 Analog Input Signal Connection

The PXI-2020/2022 provides 8/16 differential analog input channels. The analog signal can be converted to digital values by the A/D converter. To avoid ground loops and obtain more accurate measurements from the A/D conversion, it is quite important to understand the signal source type and how to connect the analog input signals.

3.2.1 Types of Signal Sources

Ground-Referenced Signal Sources

A ground-referenced signal means it is connected in some way to the building system. That is, the signal source is already connected to a common ground point with respect to the PXI-2020/2022, assuming that the computer is plugged into the same power system. Non- isolated outputs of instruments and devices that plug into the buildings power system are ground-referenced signal sources.

Floating Signal Sources

A floating signal source means it is not connected in any way to the buildings ground system. A device with an isolated output is a floating signal source, such as optical isolator outputs, transformer outputs, and thermocouples.

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3.2.2 Input Connect Configurations - Differential Input Mode

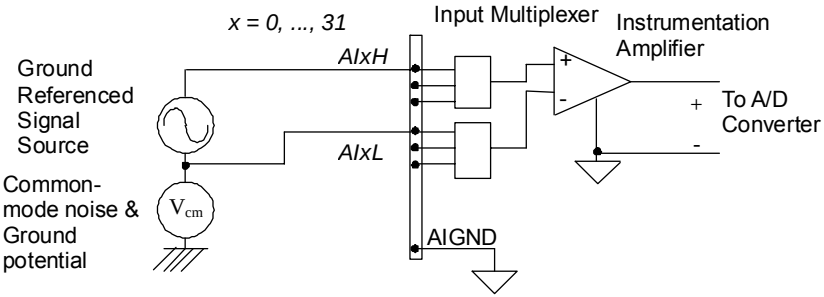


Figure 3-1: Ground-referenced Source and Differential Input

The differential input mode provides two inputs that respond to signal voltage difference between them. If the signal source is ground-referenced, the differential mode can be used for the common-mode noise rejection. Figure 3-1 shows the connection of ground-referenced signal sources under differential input mode.

Figure 3-2 shows how to connect a floating signal source to the PXI-2020/2022 card in differential input mode. For floating signal sources, you need to add a resistor at each channel to provide a bias return path. The resistor value should be about 100 times the equivalent source impedance. If the source impedance is less than 100ohms, you can simply connect the negative side of the signal to AIGND as well as the negative input of the Instru-mentation Amplifier without any resistors. In differential input mode, less noise couples into the signal connections than in single-ended mode.

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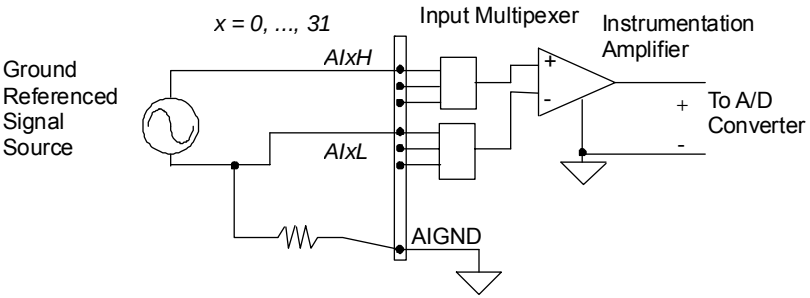


Figure 3-2: Floating Source and Differential Input

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4 Function Block and Operation Theory

The operation theory of the functions on the PXI-2020/2022 is described in this chapter. The functions include the A/D conversion, Digital I/O and General Purpose Counter/Timer. The operation theory can help you understand how to configure and program the PXI-2020/2022.

The entire PXI-2020 series of cards includs the PXI-2020/2022. In the PXI-2022 cards, all the A/D related timings are for simultaneously A/D sampling based on scanning, so that PXI-2022 also adopts the same concept, except there is only one conversion signal in a scan which could generate up to 16 samples from the different 16 channels at the same time. In the following description, to conform to the original timing design, we still use “scan” as the unit of A/D data acquisition.

4.1 Overall Function Block Diagram

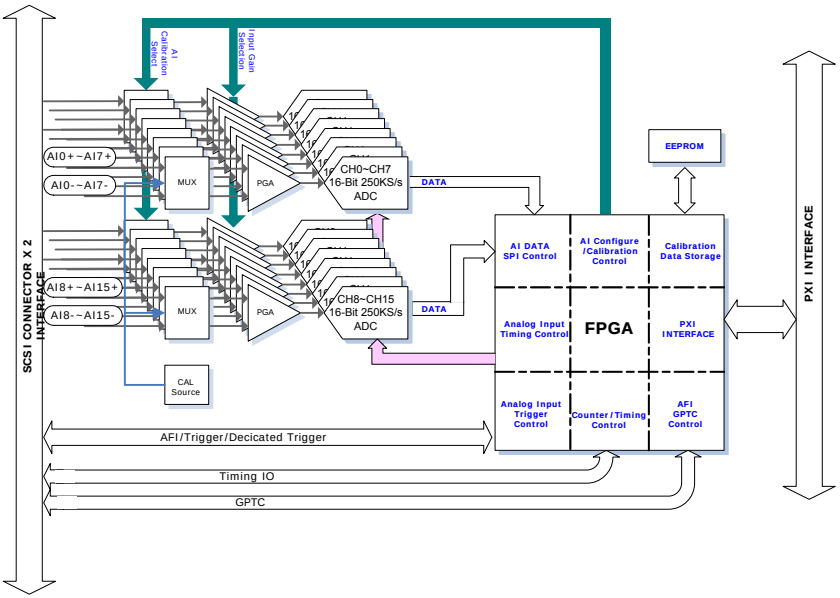


Figure 4-1: PXI-2022 Functional Block Diagram

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4.2 Basic AI Acquisition

In this section, the basic acquisition timing is explained.

4.2.1 Analog Input Path

The following figure shows the block diagram of the single analog input path of a PXI-2020/2022. Each path provides a choice of 1G Ω input impedance or high impedance. The gain amplifier is optimized for ±10 V and ±2.5 V input range with low noise and high dynamic range. An anti-aliasing filter is also adopted to eliminate high frequency noise. The 16-bit ADC provides not only accurate DC performance but also high signal-to-noise ratio, high spurious-free dynamic range in AC performance.

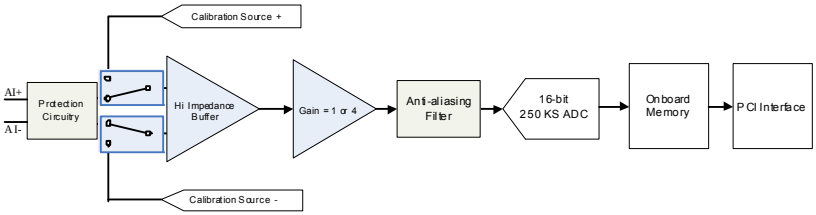


Figure 4-2: PXI-2020/2022 Analog Input Path

4.2.2 Basic Acquisition Timing

The trigger is a signal that starts or stops the acquisition. In post-trigger mode and delay trigger mode, the trigger is used to initiate acquisition. In pre-trigger mode, the trigger is used to stop acquisition. In middle-trigger mode, the trigger is used to inform the acquisition engine to acquire the specific number of data and then stop.

Timebase is a clock that sent to the ADC of each channel and the acquisition engine for essential timing functionality. The source of timebase can be either internal oscillator or external clock generator. Usually the maximum sampling rate of a Data Acquisition Module is determined by the speed of timebase. However, other sampling rate can be achieved by specifying a scan interval coun-

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ter. Please refer to Table 4-1 below and Section “4.3.4” on page 30 for more details.

Counter Name	Length	Valid value	Description
ScanIntrv	32-bit	4 to 4294967296	Scan Interval Counter. This counter is a TIMEBASE(80MHz) divider to the achieve equivalent sam-pling rate of DAQ. The equation is: Sampling rate = TIMEBASE / ScanIntrv The value of TIMEBASE de-pends on the card type. Take PXI-2022 (250KS/s) as an example, the ScanIntrv = 320 results in 250KS/s and Sca-nIntrv = 640 results in 125KS/s, and so on.
DataCnt	31-bit	1 to 2147483648	Data Counter. The amount of data to be acquired can be specified. The PXI-2022 includes 8 K sample space to store acquired data.
trigDelayTicks	32-bit	1 to 536870911	Delay Trigger Counter. The delay trigger counter is used to indicate the time be-tween a trigger event and the start of an acquisition. The unit of a delay count is the period of the TIMEBASE. For PXI-2022, the unit is 100ns. Refer to sec-tion 3.5.4 for more detail.
ReTrgCnt	32-bit	1 to 4294967296	Re-Trigger Counter. The DAQ can enable re-trigger to accept multiple triggers. Refer to section 4.5.5 for more details.

Table 4-1: Basic Counters

Refer to Figure 4-3 and use the post trigger mode as an example. When a trigger is accepted by data acquisition module, the acquisition engine of the card will begin to acquire data that coming from ADC and store these sampled data to onboard memory. The sampled data is generated con-tinuously at the rising edge of timebase according to the scan interval counter setting. While sampled data reaches customer specified number, in the below example is 256, the acquisition ends. Once the acquisition ends, acquisition engine begins to send request to system and transfer data from onboard memory back to system by DMA.

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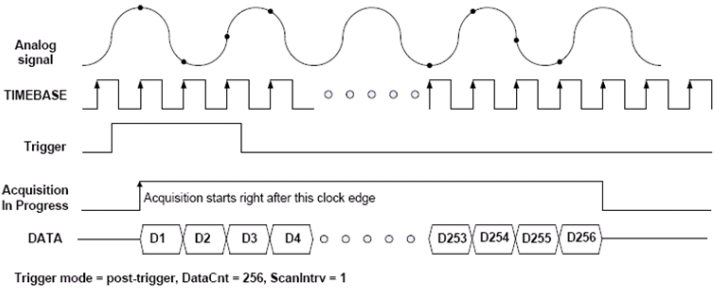


Figure 4-3: Basic Acquisition Timing of PXI-2020/2022

4.2.3 AI Data Format

When using an A/D converter, users should first know about the properties of the signal to be measured. Users can decide which channel to use and how to connect the signals to the card. Please refer to 4.2 for signal con-nections.

The A/D acquisition is initiated by a trigger source; users must decide how to trigger the A/D conversion. The data acquisition will start once a trigger condition is matched. After the end of an A/D conversion, the A/D data is buffered in a Data FIFO. The A/D data can now be transferred into the PC's memory for further process-ing.

Two acquisition modes, Software Polling and Scan acquisition are de-scribed below. Timing, trigger modes, trigger sources, and transfer me-thods are included in this section. The following table illustrates the idea transfer characteristics of various input ranges of the PXI-2020/2022. The data format of the PXI-2020/2022 is straight binary.

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Description	Bipolar Analog Input Range		Digital code
Full-scale Range	±10 V	±2.5 V	
Least significant bit	305.2 uV	76.3 uV	
FSR-1LSB	9.999695 V	2.499924 V	7FFF
Midscale +1LSB	305.2uV	76.3 uV	0001
Midscale	0 V	0 V	0000
Midscale –1LSB	-305.2 uV	-76.3 uV	FFFF
-FSR	-10 V	-2.5 V	8000

Table 4-2: Bipolar Analog Input Range and Output Digital Code

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4.3 ADC Sampling Rate and TIMEBASE Control

The PXI-2022 supports six timebase sources for analog input conversion:

1. On board Internal oscillator
2. External clock through front panel (AFI[0..7])
3. External clock through front panel SMB CLK IN
4. PXI Star Trigger
5. PXI Trigger Bus Line 0
6. PXI 10M

The following diagram shows the timebase architecture of the PXI-2022.

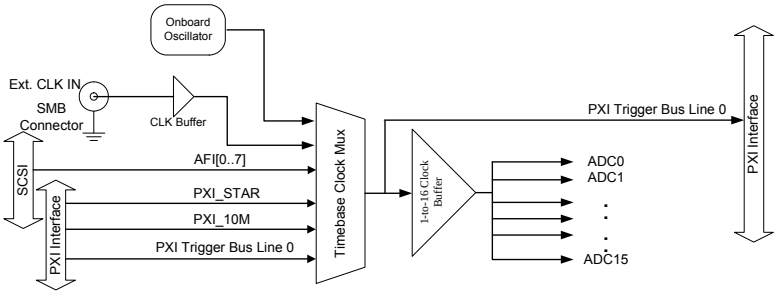


Figure 4-4: PXI-2022 Timebase Source and Architecture.

4.3.1 Internal Oscillator

The PXI-2020/2022 equips a high stability, low jitter oscillator for the ADCs. The oscillators are 80 MHz for the PXI-2020/2022.

4.3.2 External Clock through Front Panel

When you need a specific timebase in some applications that the onboard oscillator is not achievable, a clock from an external device can replace onboard oscillator. In addition, external timebase also provides a method to synchronize the DAQ module to other measurement modules by distribut-ing/receiving a common clock to/from multiple modules. The PXI-2020/2022 can receive

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an external timebase from the front panel connector AFI[0…7] or the SMB CLK IN.

As you supply the timebase from external SMB CLK IN, which should be a sine wave or square wave signal. This signal is AC coupled with 50Ω input impedance and the valid input level is from 1 to 2 volts peak-to-peak. Note that the external clock should be continuous for fix sampling rate ADC operation.

4.3.3 External Clock from PXI Interfaces

The PXI-2020/2022 can receive timebase via the PXI Trigger Bus line 0 by software setting. The eight PXI Trigger Bus lines (PXI_TRIG[0..7]) provide inter-module synchronization and communication. Note that this function is only available when the PXI-2020/2022 is in a PXI system. It's not supported when PXI-2020/2022 is in a CompactPCI system. When the PXI-2020/2022 is plugged into a generic peri-pheral slot in a PXI system, it can receive timebase from PXI_STAR. The PXI_STAR signal comes from star trigger controller is matched in propagation delay within 1 ns and the delay from star trigger slot to peripheral slot is less than 5 ns. According these hardware features, the PXI-2020/2022 can achieve very good synchronization performance when using PXI_STAR as timebase clock source. Note that the function is only available when the PXI-2020/2022 is in a PXI system. It's not supported when the PXI-2020/2022 is in a CompactPCI system.

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4.3.4 Sampling Rate Control

By specifying different scan interval counter (32-bit) value, different sam-pling rate can be achieved. The following formula determines the ADC sampling rate. Sampling Rate = TIMEBASE/ScanIntrv Where ScanIntrv is scan interval counter, value can be 4, 5, 6, 7, ... 2^{32-1}.

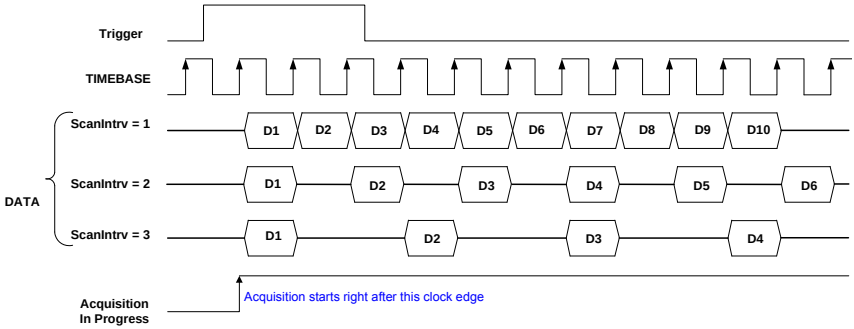


Figure 4-5: Configuring Different Sampling Rate of PXI-2022.

4.3.5 Timebase Exporting

The PXI-2020/2022 can export timebase to one of the PXI trigger bus line 0. By software programming, you can pick up a trigger line to transmit timebase clock. This feature is very useful when synchronize to multiple measurement modules.

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4.4 Trigger Sources

In addition to the internal software trigger, the PXI-2020/2022 supports external digital triggers from the front panel connector AFI[0…7], SMB TRIG I/O, PXI_STAR triggers, PXI Trigger Bus Line 5. You can configure the trigger source by software command. Please refer to Figure 4-6 for trigger architecture.

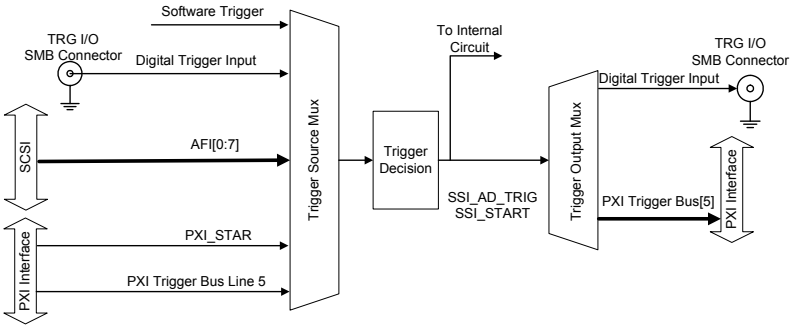


Figure 4-6: PXI-2020/2022 Trigger Sources

4.4.1 Software Trigger

Software trigger is generated by software command. The trigger asserts right after executing specified function calls to begin the operation. This is the easiest way to acquire a single A/D data. The A/D converter starts one con-version whenever the dedicated software command is executed. Then the software would poll the conversion status and read the A/D data back when it is available. This method is very suitable for applications that need to process A/D data in real time. Under this mode, the timing of the A/D conversion is fully controlled under software. However, it is difficult to control the A/D conversion rate.

4.4.2 External Digital Trigger

An external digital trigger occurs when a TTL rising edge or a falling edge is detected at the SMB connector TRG IO on the front panel. As illustrated in Figure 4-7, the trigger polarity can be selected by software. Note that the signal level of the external digital trigger signal should be TTL-compatible, and the minimum pulse width is 12.5 ns.

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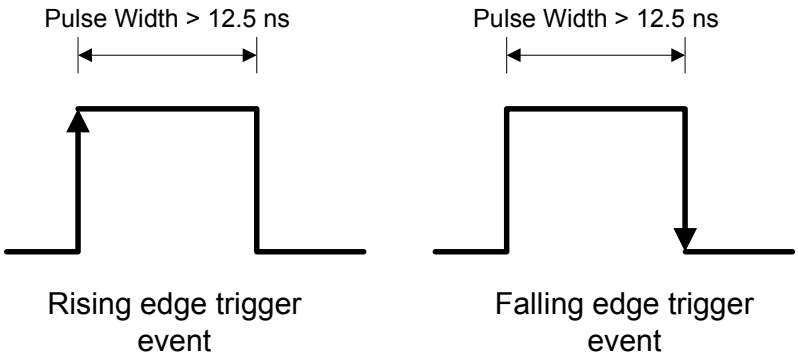


Figure 4-7: External Digital Trigger Polarity and Pulse Width Re-quirement.

4.4.3 PXI Star Trigger

When you select PXI Star Trigger as the trigger source, the PXI-2020/2022 can accept a TTL-compatible digital signal as a trigger signal. The trigger occurs when a rising edge or falling edge is detected at PXI Star Trigger. You can use software to configure the trigger polarity. The minimum pulse width requirement of this digital trigger signal is 12.5 ns.

4.4.4 PXI Trigger Bus

The PXI-2020/2022 utilizes PXI Trigger Bus[5] as System Synchronization In-terface (SSI). Using the interconnected bus provided by PXI Trigger Bus, you can easily synchronize multiple modules. When configured as input, the PXI-2020/2022 is served as a slave module and can accept three different SSI signals, SSI_TIMEBASE (PXI Trigger Bus[0]), PXI Trigger Bus[5] and PXI Star Trigger Bus[1]. When confi-gured as output, the PXI-2020/2022 is served as a master module and can output SSI_TIMEBASE, SSI_AD_TRIG or SSI_ADCONV to PXI Trigger Bus. Each signal is dedicated routed from the PXI Trigger Bus[5].

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4.4.5 Trigger Signal Exporting

The PXI-2020/2022 can export trigger signals to following connectors/bus: SMB TRG IO on front panel, AFI0 on front panel and PXI Trigger Bus Line 5. The TRG IO on the front panel can also be programmed to output the trigger signal when the trigger source is from software trigger, Auxiliary Function Interface, PXI Star Trigger, or PXI Trigger Bus Line 5. The timing characteristic is in Figure 4-8.

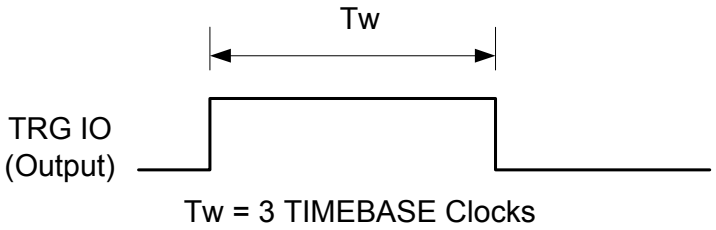


Figure 4-8: TRG IO Output Signal Timing

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4.5 User-controllable Timing Signals

In order to meet the requirements for user-specific timing and the re-quirements for synchronizing multiple cards, the PXI-2020/2022 series provides flexible user-controllable timing signals to connect to external circuitry or additional cards.

The entire DAQ timing of the PXI-2020/2022 series is composed of a bunch of counters and trigger signals in the FPGA. These timing signals are related to the A/D conversions and Timer/Counter applications. These timing signals can be inputs to or outputs from the I/O connectors, the SSI connector and the PXI bus. Therefore the internal timing signals can be used to control external devices or circuitry's. However, the SSI/PXI timing signals remain the same for every PXI-2020/2022 card.

We implemented signal multiplexers in the FPGA to individually choose the desired timing signals for the DAQ operations, as shown in the Figure 4-9.

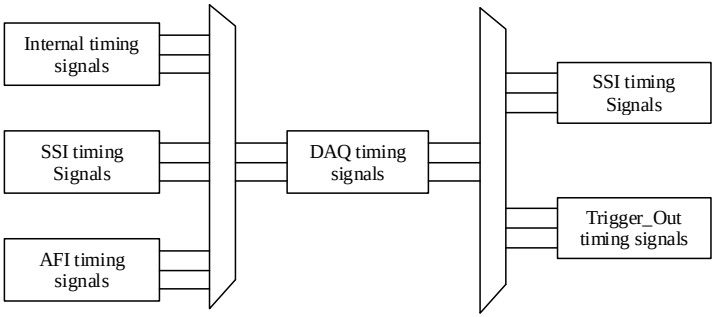


Figure 4-9: DAQ Signal Routing

You can utilize the flexible timing signals through our software drivers, and simply and correctly connect the signals with the PXI-2020/2022 series cards. Here is the summary of the DAQ timing signals and the corresponding functionalities for PXI-2020/2022 series.

To route an internal signal to the AFIn, PXI STAR Trigger, or the PXI Trigger Bus[5] line, or to enable clock sharing through the PXI trigger bus line or the PXI Star trigger line. please refer to D2K-DASK Function Reference, check the D2K-Route_Siganl Usage for details.

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Timing Signal Category	Corresponding Functionality
SSI/PXI signals	Multiple cards synchronization
AFI signals	Control PXI-2020/2022 by external timing signals
SMB CLK IN	Control PXI-2020/2022 by external timing signals
AI_Trig_Out	Control external circuitry or boards

Table 4-3: Summary of User-controllable Timing Signals and Corresponding Functionalities

4.5.1 DAQ timing signals

The user-controllable internal timing-signals contain: (Please refer to Section 4.1.4 for the internal timing signal definition)

1. TIMEBASE, providing TIMEBASE for all DAQ operations, which could be from internal 80MHz oscillator, EXTTIMEBASE from I/O connector or the SSI_TIMEBASE (PXI Trigger Bus [5]). Note that the frequency range of the EXTTIMEBASE is 1MHz to 80MHz, and the EXTTIMEBASE should be TTL-compatible.
2. AD_TRIG, the trigger signal for the A/D operation, which could come from external digital trigger, internal software trigger and SSI_AD_TRIG (PXI Trigger Bus [0]). Refer to Section 4.5 for detailed description.
3. SCAN_START, the signal to start a scan, which would bring the following ADCONV signals for AD conversion, and could come from the internal SI_counter, AFI[0] and SSI_AD_START. This signal is synchronous to the TIMEBASE. Note that the AFI[0] should be TTL-compatible and the minimum pulse width should be the pulse width of the TIMEBASE to guarantee correct functionalities.

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4. ADCONV, the conversion signal to initiate a single conversion, which could be derived from internal counter, AFI[0] or SSI_ADCONV. Note that this signal is edge-sensitive. When using AFI[0] as the external ADCONV source, each rising edge of AFI[0] would bring an effective conversion signal. Also note that the AFI[0] signal should be TTL-compatible and the minimum pulse width is 20ns.

4.5.2 Auxiliary Function Inputs (AFI)

You could use the AFI in applications that take advantage of external circuitry to directly control the PXI-2020/2022 series cards. The AFI includes 2 categories of timing signals: one group is the dedicated input, and the other is the multi-function input.

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4.6 Trigger Modes

There are four trigger modes working with trigger sources to initiate different data acquisition timing when a trigger event occurs. They are described in this section.

4.6.1 Post-trigger Acquisition

Use post-trigger acquisition when you want to collect data after the trigger event, as illustrated in Figure 4-10.

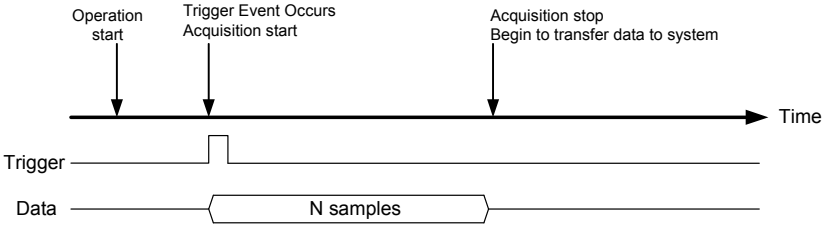


Figure 4-10: Post-trigger Acquisition

4.6.2 Pre-trigger Acquisition

Use pre-trigger acquisition to collect data before the trigger event. The acquisition starts once specified function calls are executed to begin the pre-trigger operation, and it stops when the trigger event occurs. If the trigger event occurs after the specified amount of data has been acquired, the system only stores the data before the trigger event with specified amount, as illustrated in Figure 4-11.

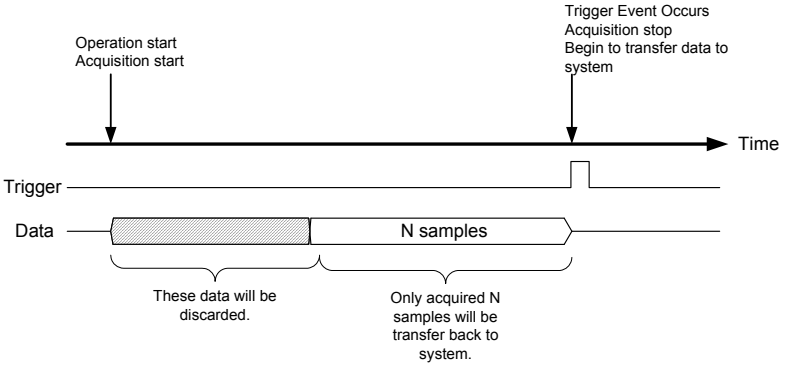


Figure 4-11: Pre-trigger Mode Operation

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The trigger event occurs after the specified amount of data has been acquired. However, if the trigger event occurs before the specified amount of data has been acquired, the acquisition engine will ignore the trigger signal until the specified amount of data has been acquired. Refer to Figure 4-12 for an example.

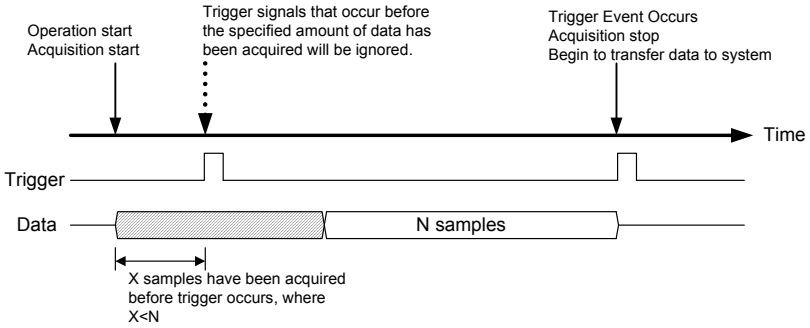


Figure 4-12: Pre-trigger Mode Operation

4.6.3 Middle-trigger Acquisition

Use middle-trigger acquisition when you want to collect data before and after the trigger event. The amount of stored data before and after trigger event can be set individually (M and N samples), as illustrated in Figure 4-13.

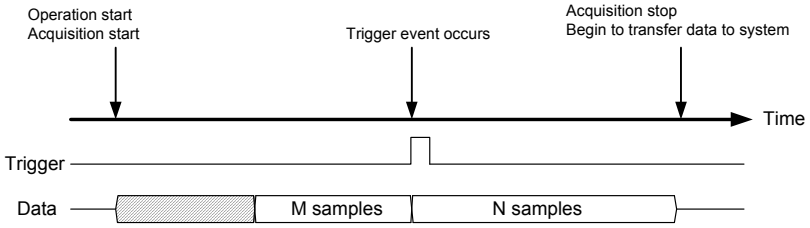


Figure 4-13: Middle-trigger Mode Operation

Please note that trigger event can only accepted when the specified amount of data has been acquired (M samples). If the sampled data is not enough, the trigger event will be ignored.

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4.6.4 Delay-trigger Acquisition

Use delay-trigger acquisition to delay the data collection after the trigger event, as illustrated in Figure 4-14. The delay time is specified by a 32-bit counter value so that the maximum delay time is the period of TIMEBASE X (232 - 1), while the minimum delay is the period of timebase.

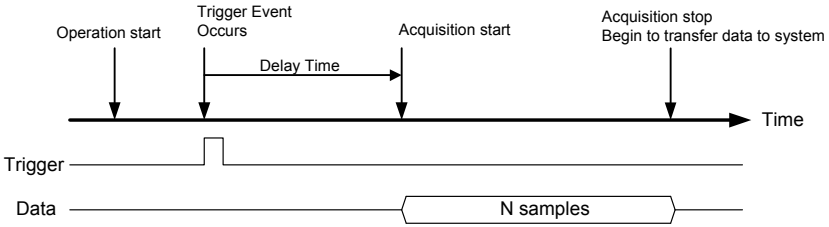


Figure 4-14: Delay-trigger Mode Operation

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4.7 Synchronizing Multiple Modules

SSI (System Synchronization Interface) provides the DAQ timing synchronization between multiple cards. In PXI-2020/2022 series, we designed a bi-directional SSI I/O to provide flexible connection between cards and allow one SSI master to output the signal and up to three slaves to receive the SSI signal. Note that the SSI signals are designed for card synchronization only, not for external devices.

In PXI form factor, we utilize the PXI trigger bus built on the PXI backplane to provide the necessary timing signal connections. All the SSI signals are routed to the P2 connector. No additional cable is needed. For detailed information of the PXI specifications, please refer to PXI specification Re-vision 2.0 from PXI System Alliance (www.pxisa.org).

The eight interconnected lines on PXI backplane named as PXI Trigger Bus[0:7] provide a flexible interface for multiple modules synchronization. The PXI-2020/2022 utilizes the PXI Trigger Bus[0:7] as the System Synchronization Interface (SSI). By providing flexible routing of timebase clock and trigger signals onto PXI Trigger Bus, the PXI-2020/2022 makes the synchronization be-tween multiple modules easy and simple. The bi-directional SSI I/Os provide a flexible connection between modules, which allows one SSI master PXI-2020/2022 to output the SSI signals to other slaves modules to receive the signals. Table 4-4 lists the summary of SSI timing signals and the functionalities. Figure 4-15 shows the architecture of SSI. Note that it's not allowed to route different signals onto the same trigger bus line.

SSI Timing Signal	Functionality
SSI_TIMEBASE	SSI master: send the TIMEBASE out SSI slave: accept the SSI_TIMEBASE to replace the internal TIMEBASE signal. Note: Affects A/D and operations
SSI_AD_TRIG	SSI master: send the internal AD_TRIG out SSI slave: accept the SSI_AD_TRIG as the digital trigger signal.
SSI_ADCONV	SSI master: send the ADCONV out SSI slave: accept the SSI_ADCONV to replace the internal ADCONV signal.

Table 4-4: SSI Timing

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The 3 internal timing signals could be routed to the PXI trigger bus through software drivers. Please refer to section 4.6.1 for detailed information of the 6 internal timing signals. Physically the signal routings are accomplished in the FPGA. Cards that are connected together through the PXI trigger bus, will still achieve synchronization on the 3 timing signals.

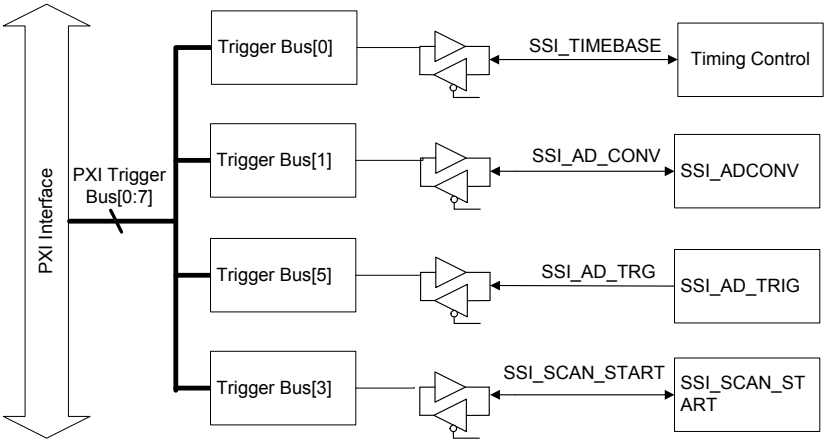


Figure 4-15: SSI Mode Operation

4.7.1 SSI_TIMEBASE

As an output, the SSI_TIMEBASE signal outputs the onboard LVTTL time-base through PXI trigger bus line 0. As an input, the PXI-2020/2022 accepts the SSI_TIMEBASE signal to be the source of timebase.

In PXI form factor, we utilize the PXI trigger bus built on the PXI backplane to provide the necessary timing signal connections. All the SSI signals are routed to the J2 connector. No additional cable is needed. For detailed information of the PXI specifications, please refer to PXI specification Revision 2.0 from PXI System Alliance (www.pxisa.org).

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The SSI/PXI mechanism

1. We adopt master-slave configuration for SSI/PXI. In a system, for each timing signal, there shall be only one master, and other cards are SSI slaves or with the SSI function disabled.
2. For each timing signal, the SSI master doesn't have to be in a single card.

   For example:

   We want to synchronize the A/D operation through the SSI_ADCONV signal for 4 PXI-2020/2022 cards. Card 1 is the master, and Card 2, 3, 4 are slaves. Card 1 receives an external digital trigger to start the post trigger mode acquisition. The SSI setting could be:

   a.Set the SSI_ADCONV signal of Card 1 to be the master.

   b.Set the SSI_ADCONV signals of Card 2, 3, 4 to be the slaves.

   c.Set external digital trigger for Card 1's A/D operation.

   d.Set the SI_counter and the post scan counter (PSC) of all other cards.

   e.Start DMA operations for all cards, thus all the cards are waiting for the trigger event.

When the digital trigger condition of Card 1 occurs, Card 1 will internally generate the ADCONV signal and output this ADCONV signal to SSI_ADCONV signal of Card 2, 3 and 4 through the SSI/PXI connectors. Thus we can achieve 8/16-channel acquisition simultaneously for PXI-2020 and PXI-2022, correspondingly..

You could arbitrarily choose each of the 4 timing signals as the SSI master from any one of the cards. The SSI master can output the internal timing signals to the SSI slaves. With the SSI, users could achieve better card-to-card synchronization.

Note that when power-up or reset, the DAQ timing signals are reset to use the internal generated timing signals.

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4.8 General Purpose Timer/Counter Operation

Two independent 16-bit up/down timer/counter are designed within FPGA for various applications. They have the following features:

- Count up/down controlled by hardware or software
- Programmable counter clock source (internal or external clock up to 10 MHz)
- Programmable gate selection (hardware or software control)
- Programmable input and output signal polarities (high active or low active)
- Initial Count can be loaded from software
- Current count value can be read-back by software without affecting circuit operation

4.8.1 Timer/Counter Functions Basics

Each timer/counter has three inputs that can be controlled via hardware or software. They are clock input (GPTC_CLK), gate input (GPTC_GATE), and up/down control input (GPTC_UPDOWN). The GPTC_CLK input provides a clock source input to the timer/counter. Active edges on the GPTC_CLK input make the counter increment or decrement. The GPTC_UPDOWN input controls whether the counter counts up or down. The GPTC_GATE input is a control signal which acts as a counter enable or a counter trigger signal under different applications.

The output of timer/counter is GPTC_OUT. After power-up, GPTC_OUT is pulled high by a pulled-up resister about 10K ohms. Then GPTC_OUT goes low after the PXI-2020/2022 is initialized.

All the polarities of input/output signals can be programmed by software. In this chapter, for easy explanation, all GPTC_CLK, GPTC_GATE, and GPTC_OUT are assumed to be active high or rising-edge triggered in the figures.

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4.8.2 General Purpose Timer/Counter Modes

Eight programmable timer/counter modes are provided. All modes start operating following a software-start signal that is set by the software. The GPTC software reset initializes the status of the counter and re-loads the initial value to the counter. The operation remains halted until the soft-ware-start is re-executed. The operating theories under different modes are described as below.

Mode 1: Simple Gated-Event Counting

In this mode, the counter counts the number of pulses on the GPTC_CLK after the software-start. Initial count can be loaded from software. Current count value can be read-back by software any time without affecting the counting. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-16 illustrates the operation with initial count = 5, count-down mode.

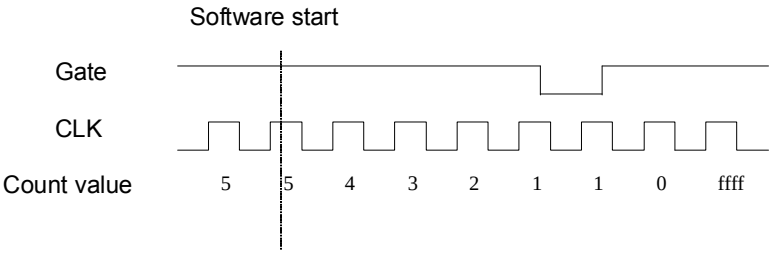


Figure 4-16: Mode 1 Operation

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Mode 2: Single Period Measurement

In this mode, the counter counts the period of the signal on GPTC_GATE in terms of GPTC_CLK. Initial count can be loaded from software. After the software-start, the counter counts the number of active edges on GPTC_CLK between two active edges of GPTC_GATE. After the com-pletion of the period interval on GPTC_GATE, GPTC_OUT outputs high and then current count value can be read-back by software. Figure 4-17 il-lustrates the operation where initial count = 0, count-up mode.

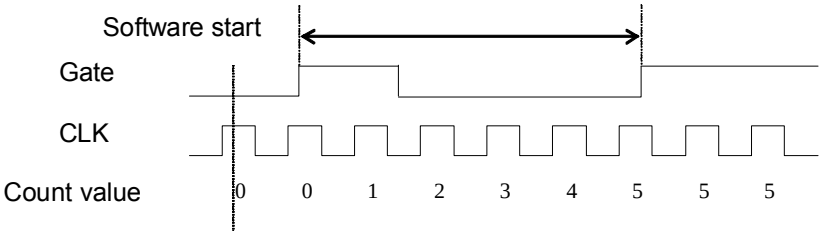


Figure 4-17: Mode 2 Operation

Mode 3: Single Pulse-width Measurement

In this mode the counter counts the pulse-width of the signal on GPTC_GATE in terms of GPTC_CLK. Initial count can be loaded from software. After the software-start, the counter counts the number of active edges on GPTC_CLK when GPTC_GATE is in its active state. After the completion of the pulse-width interval on GPTC_GATE, GPTC_OUT outputs high and then current count value can be read-back by software. Figure 4-18 illustrates the operation where initial count = 0, count-up mode.

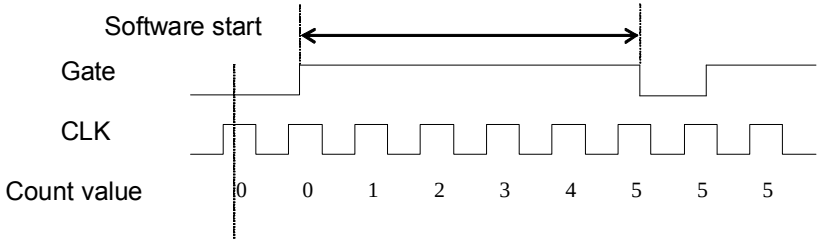


Figure 4-18: Mode 3 Operation

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Mode 4: Single Gated Pulse Generation

This mode generates a single pulse with programmable delay and pro-grammable pulse-width following the software-start. The two programmable parameters could be specified in terms of periods of the GPTC_CLK input by software. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-19 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.

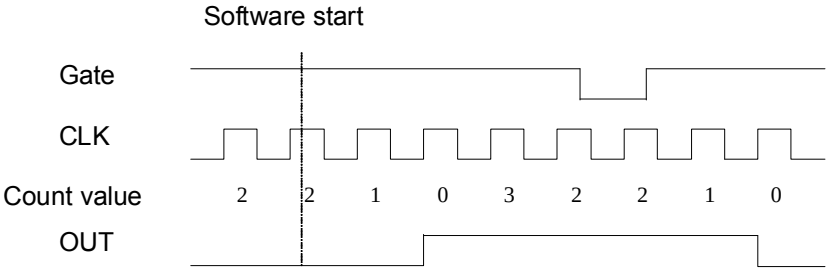


Figure 4-19: Mode 4 Operation

Mode 5: Single Triggered Pulse Generation

This function generates a single pulse with programmable delay and programmable pulse-width following an active GPTC_GATE edge. You could specify these programmable parameters in terms of periods of the GPTC_CLK input. Once the first GPTC_GATE edge triggers the single pulse, GPTC_GATE takes no effect until the software-start is re-executed. Figure 4-20 illustrates the generation of a single pulse with a pulse delay of two and a pulse-width of four.

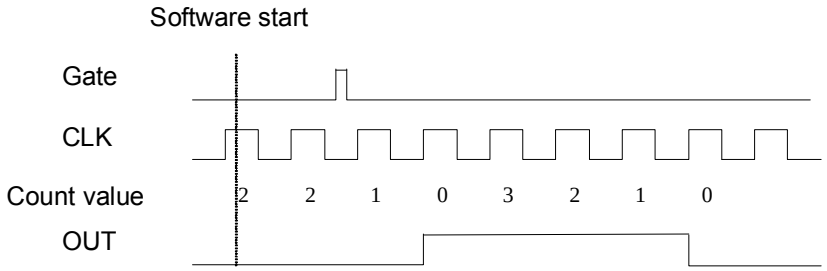


Figure 4-20: Mode 5 Operation

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Mode 6: Re-triggered Single Pulse Generation

This mode is similar to mode5 except that the counter generates a pulse following every active edge of GPTC_GATE. After the software-start, every active GPTC_GATE edge triggers a single pulse with programmable delay and pulse-width. Any GPTC_GATE triggers that occur when the prior pulse is not completed would be ignored. Figure 4-21 illustrates the generation of two pulses with a pulse delay of two and a pulse-width of four.

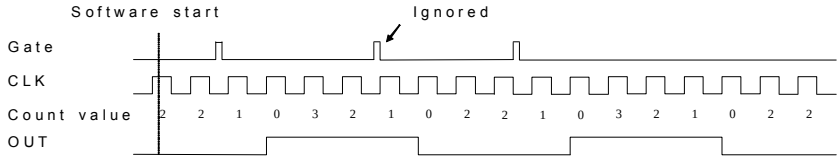


Figure 4-21: Mode 6 Operation

Mode 7: Single Triggered Continuous Pulse Generation

This mode is similar to mode5 except that the counter generates conti-nuous periodic pulses with programmable pulse interval and pulse-width following the first active edge of GPTC_GATE. Once the first GPTC_GATE edge triggers the counter, GPTC_GATE takes no effect until the soft-ware-start is re-executed. Figure 4-22 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.

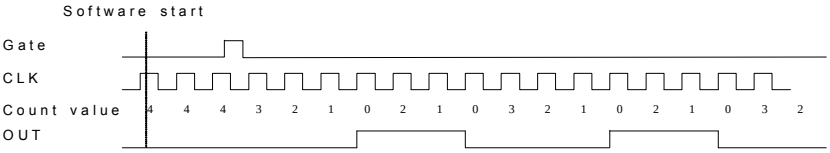


Figure 4-22: Mode 7 Operation

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Mode 8: Continuous Gated Pulse Generation

This mode generates periodic pulses with programmable pulse interval and pulse-width following the software-start. GPTC_GATE is used to enable/disable counting. When GPTC_GATE is inactive, the counter halts the current count value. Figure 4-23 illustrates the generation of two pulses with a pulse delay of four and a pulse-width of three.

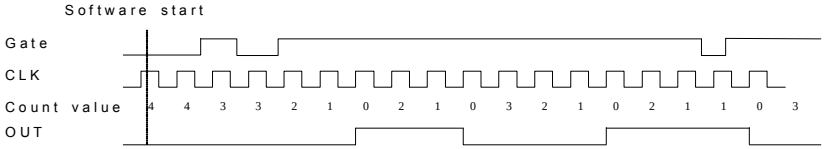


Figure 4-23: Mode 8 Operation

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5 Calibration

This chapter introduces the calibration process to minimize AD measurement errors and DA output errors.

5.1 Loading Calibration Constants

The PXI-2020/2022 is factory calibrated before shipment by writing the associated calibration constants of TrimDACs to the onboard EEPROM. TrimDACs are devices containing multiple DACs within a single package. TrimDACs do not have memory capability. That means the calibration constants do not retain their values after the system power is turned off. Loading calibration constants is the process of loading the values of TrimDACs stored in the onboard EEPROM. ADLINK provides software to make it easy to read the calibration constants automatically when necessary.

There is a dedicated space for calibration constants In the EEPROM. In addition to the default bank of factory calibration constants, there are three extra user-modifiable banks. This means users can load the TrimDACs values either from the original factory calibration or from a calibration that is subsequently performed.

Because of the fact that errors in measurements and outputs will vary with time and temperature, it is recommended recalibratation when the card is installed in the users environment. The auto-calibration function used to minimize errors will be introduced in the next sub-section.

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5.2 Auto-calibration

By using the auto-calibration feature of the PXI-2020/2022, the calibration software can measure and correct almost all the calibration errors without any external signal connections, reference voltages, or measurement devices.

The PXI-2020/2022 has an on-board calibration reference to ensure the accuracy of auto-calibration. The reference voltage is measured at the factory and adjusted through a digital potentiometer by using an ultra-precision calibrator. The impedance of the digital potentiometer is memorized after this adjustment. It is not recommended for users to adjust the on-board calibration reference except when an ultra-precision calibrator is available.

Note:

1. Before auto-calibration procedure starts, it is recommended to warn up the card for at least 15 minutes.
2. Please remove the cable before an auto-calibration procedure is initiated because the DA outputs would be changed in the process of calibration.

5.3 Saving Calibration Constants

After an auto-calibration is completed, users can save the new calibration constants into one of the three user-modifiable banks in the EEPROM. The date and the temperature when you ran the auto-calibration will be saved accompanied with the calibration constants. This means users can store three sets of calibration constants according to three different environments and reload the calibration constants later.

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Important Safety Instructions

Please read and follow all instructions marked on the product and in the documentation before operating the system. Retain all safety and operating instructions for future use.

- Please read these safety instructions carefully.
- Please keep this User's Manual for future reference.
- The equipment should be operated in an ambient temperature between 0 to 50°C.
- The equipment should be operated only from the type of power source indicated on the rating label. Make sure the voltage of the power source is correct when connecting the equipment to the power outlet.
- If the user's equipment has a voltage selector switch, make sure that the switch is set to the proper position for the area. The voltage selector switch is set at the factory to the correct voltage.
- For pluggable equipment, ensure they are installed near a socket-outlet that is easily accessible.
- Secure the power cord to prevent unnecessary accidents. Do not place anything over the power cord.
- If the equipment will not be in use for long periods of time, disconnect the equipment from mains to avoid being damaged by transient overvoltage.
- All cautions and warnings on the equipment should be noted.
- Please keep this equipment away from humidity.
- Do not use this equipment near water or a heat source.
- Place this equipment on a reliable surface when installing. A drop or fall could cause injury.
- Never pour any liquid into the opening, this could cause fire or electrical shock.

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- Openings in the case are provided for ventilation. Do not block or cover these openings. Make sure there is adequate space around the system for ventilation when setting up the work area. Never insert objects of any kind into the ventilation openings.
- To avoid electrical shock, always unplug all power and modem cables from the wall outlets before removing covers.
- Lithium Battery provided (real time clock battery)

  "CAUTION - Risk of explosion if battery is replaced by an incorrect type. Dispose used batteries as instructed in the instructions"
- The equipment should be checked by service personnel if one of the following situation arises:
  - The power cord or plug is damaged.
  - Liquid has penetrated the equipment.
  - The equipment has been exposed to moisture.
  - The equipment is not functioning or does not function according to the user's manual.
  - The equipment has been dropped and damaged.
  - If the equipment has obvious sign of breakage.
- Never open the equipment. For safety reasons, the equipment should only be opened by qualified service personnel.

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