# PXI-3800

3U PXI Pentium M

System Controller

**User's Manual**

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# 1 Introduction

The PXI-3800 System Controller is ADLINK's first Intel® Pentium® M solution in the PXI form factor. This product is designed to meet the highest performance requirements for embedded computing. It is based on the Intel® Pentium® M processor, 855GME and 6300ESB chipset that provides both long life and excellent driver support to meet the majority of industrial applications. The PXI-3800 System Controller complies with PXI specification Rev. 2.2 and features many practical interfaces, such as hot swappable CompactFlash card, USB 2.0 ports, and Gigabit Ethernet. The PXI-3800 can support a CPU frequency of up to 1.8GHz and a memory size up to 2GB RAM via two 200-pin DDR SO-DIMM sockets. With an embedded PXI trigger pin, the PXI-3800 provides synchronous trigger ability to meet the high-performance requirements of instrumentation. In addition, the PXI-3800's compact and rugged mechanism makes it ideal for test & measurement applications in harsh environments.

This chapter gives an overview of the PXI-3800 System Controller, and covers the following topics:

- Features
- Functional block diagram and overview
- Specifications
- Unpacking checklist

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## 1.1 Features

### PXI-3800 Features

- Standard 3U PXI form factor
- PICMG 2.0 CompactPCI Specification R3.0 compliant
- PICMG 2.8 PXI Specification Rev. 2.2 compliant
- PICMG 2.1 R1.0 CompactPCI Hot Swap Specification compliant
- Design for Pentium® M processor, FSB 400MHz, CPU frequency up to 1.8GHz
- Two 200-pin DDR SO-DIMM sockets supporting up to 2GB RAM
- One 44-pin EIDE (primary IDE) with built-in 2.5” low profile HDD (40 GB, standard)
- Two CompactFlash interfaces for HDD and FDD replacement; CF Type II supports hot-swappable CF card functionality
- Two USB 2.0 ports, two serial ports (RS-232) and one parallel port  provided on the front panel
- One AC ‘97  stereo audio output
- One TRIG I/O on the front panel for advanced PXI trigger function
- VGA output on the front panel supporting up to 2048 x 1536 resolution at 75Hz
- Intel® 82545EM controller providing one 10/100/1000 Mb Ethernet port
- Supports 7 bus-master PCI devices on PXI/CompactPCI bus
- Programmable watchdog timer

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## 1.2 Functional Block Diagram

The following sections give an overview the PXI-3800 System Controller's main features as outlined in the functional block diagram below:

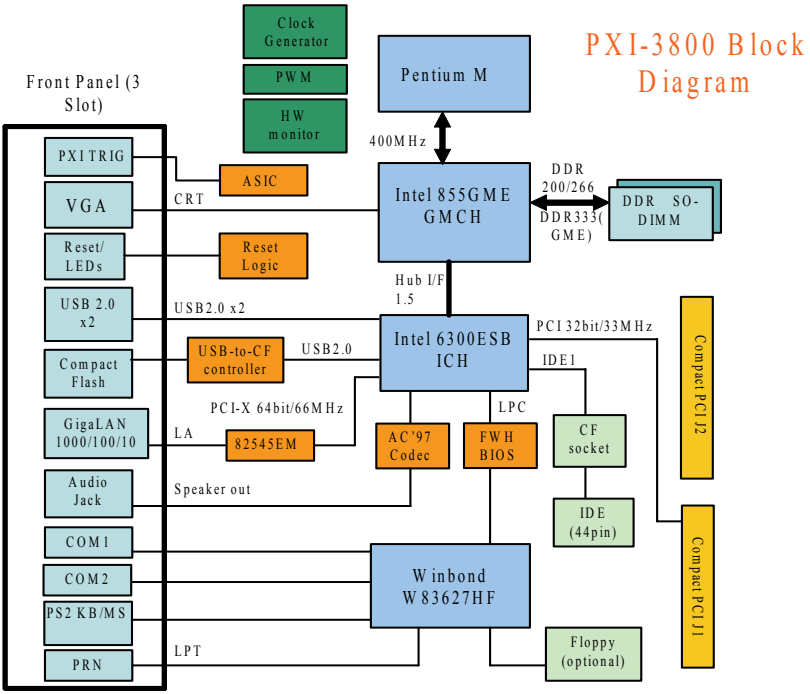



**Figure 1-1: PCI-3800 Functional Block Diagram**

### PXI Bus Interface

The PXI-3800 System Controller is built on the PICMG 2.8 Instrumentation Extensions to CompactPCI Specification. PXI specifications dedicate the leftmost slot of the PXI chassis to the System Controller. PXI is electrically compatible with the PCI local bus standard, and provides enhanced instrumentation signals for synchronization or communication between peripherals. Based on the mechanical design of CompactPCI systems, PXI systems provide

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the high levels of environmental performance required by the vibration, shock, temperature, and humidity extremes of industrial environments.

The PXI-3800 utilizes a 32-bit/33MHz PCI bus and can be used in the ADLINK PXI chassis listed below:

- PXIS-2506, 6-slot 3U PXI Instrument chassis
- PXIS-2556/T, 6-slot 3U Instrument chassis
- PXIS-2630, 8-slot 3U PXI Instrument chassis
- PXIS-2650/T, 8-slot 3U Instrument chassis
- PXIS-2700, 18-slot 3U PXI Instrument chassis
- PXIS-2680P, 8-slot 3U Integrated Portable Instrument chassis

When used in a Hot Swap compliant backplane and in accordance to the CompactPCI Hot Swap Specification, PICMG 2.1 R1.0, the PXI-3800 System Controller supports hot swappable peripherals in a powered system.

## CPU Support

The PXI-3800 supports a single Intel® Pentium® M Processor with 1MB L2 cache in 478-pin Micro-FCPGA or 479-ball Micro-FCBGA package. The standard PXI-3800 comes with a CPU socket which can be installed with a Micro-FC-PGA package CPU, including Pentium M 1.1GHz, 1.6GHz and 1.8GHz. The Pentium® M processor runs at a core speed up to 1.8GHz, with a Front Side Bus (FSB) speed of 400MHz. Micro-FCBGA package support is reserved for OEM programs only. ADLINK's factory can pre-mount the CPU for customers. Please contact an ADLINK sales representative for available CPU configurations.

The Intel® Pentium® M processor is a high performance, low power mobile processor with several micro-architectural enhance-

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ments over existing Intel mobile processors. The key features of the processor are listed as follows:

- Support Intel® Architecture with Dynamic Execution
- On-die, primary 32-KB instruction cache and 32-KB write-back data cache
- On-die, 1-MB second level cache with Advanced Transfer Cache Architecture
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2)
- 400-MHz, Source-Synchronous processor system bus
- Advanced Power Management features including Enhanced Intel® SpeedStep® technology

The Pentium® M processor runs at a core speed up to 1.8GHz, with a Front Side Bus (FSB) speed of 400MHz.

## Memory Support

The PXI-3800 is based on Intel® 855GME chipset, which consists of 855GME Graphics Memory Controller Hub (GMCH) and the 6300ESB I/O Controller Hub (ICH). The GMCH system memory interface supports the following features:

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- Single channel of x72, unbuffered, ECC DDR SDRAM (SO-DIMM)
- 200, 266MHz and 333MHz DDR device
- 64-bit data interface(72-bit with ECC)
- Up to two double-sided SO-DIMMs (four rows populated) with unbuffered PC2100/PC2700 DDR-SDRAM (with or without ECC)
- Up to 16 simultaneous open pages
- 64MB, 128MB, 256MB, and 512MB technologies for x8 and x16 width devices
- System memory supports up to 2GB
- SDRAM speed, type and size can be determined by the BIOS reading the SO-DIMM presence detect bits on the System Management Bus (SMBus)
- SDRAM timing register, which provides the DRAM speed control for the entire array, is programmed to use the timings of the slowest DRAMs installed.

## Ethernet Interfaces

The PXI-3800 supports an Intel® 82545EM Gigabit Ethernet controller. It integrates MAC and PHY functions into a single chip to provide a standard IEEE 802.3 Ethernet interface for 10/100/1000BASE-T applications. The controller provides a 64-bit wide interface compliant with PCI 2.3 and PCI-X 1.0a specifications. The Ethernet interface is routed to an RJ45 port with activity/speed LEDs. The controller supports Intel® Pre-Boot Execution Environment (PXE) for remote boot of Windows NT/2000. The board's Ethernet addresses are displayed on the label attached to the connector.

## Display Interfaces

The Intel® 855GME GMCH chip has dual independent display pipes which can support concurrent or simultaneous display on each display device. The 350MHz integrated 24bit RAMDAC supports analog display pixel resolution up to 1600x1200 at 85Hz and

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2048x1536 at 75Hz. One DVO port supports digital video output with 165MHz output clock on 12 bit interface with pixel resolution up to 1600x1200 at 85Hz. Tri-view is supported through the LFP interface, DVO and CRT. Up to 64MB of dynamic video memory allocation and is DDC2B compliant.

## IDE Interfaces

PXI-3800 supports one 44-pin EIDE connector and two Compact-Flash Type I/II sockets. The 44-pin EIDE connector supports a 2.5" HDD with Ultra ATA 66/100 support. CompactFlash support listed as below:

- One Compact Flash Type II interface through IDE interface
- One Compact Flash Type II drive using USB to CF adaptor

### Internal 44-pin IDE Interfaces

The 44-pin IDE connector is on the top-side of the PXI-3800. A 2.5-inch low profile 40GB HDD is mounted on the PXI-3800 as standard configuration. Contact an ADLINK sales representative for available 2.5-inch drive options. For some customers, a CompactFlash Disk may be used for harsh environment applications.

### Internal CompactFlash Socket

An internal CompactFlash socket is available on the PXI-3800. It is connected to the IDE interface, which is also bootable. With a solid state CF card, PXI-3800 can work in high-vibration environments.

## Universal Serial Bus (USB)

The PXI-3800 supports three USB 2.0 serial ports. Ports 1 and 2 are on front panel, port 3 is used as a USB-to-CF or USB-to-IDE adaptor to support a Compact Flash Type II socket on the front panel or a 2.5" IDE HDD. Additional ports can be added through the use of an external USB hub. USB allows for the easy addition of peripherals such as mouse, keyboard, speakers, etc. Transfer

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rates of up to 480Mb/s are supported. High-speed connections require shielded cables. The PXI-3800 provides each USB port 0.5A at 5V to power peripherals and each USB port is protected by a power distribution switch (0.5A rating allows for inrush currents).

### Hot-swappable CF Interface

An external CompactFlash socket is available on the PXI-3800 front panel. The external CompactFlash interface provides Plug and Play features and is also hot swappable. Therefore, a CompactFlash card can be used as a replacement for floppy disks and can also provide very large storage capability (up to 1GB). It is also possible to set this CF interface as a boot device by selecting boot from USB in the BIOS menu. Note that drivers are needed for the external CompactFlash interface. Refer to Chapter 3 for installation detail.

### Serial I/O

The PXI-3800 provides support for two 16C550 UART compatible COM ports. COM1 and COM2 are accessible from the front faceplate through DB-9 connectors. COM1 is jumper-selectable to support a RS-422/485 interface. The RS-485 mode supports auto direction control which can automatically sense the direction of data flow and switch the transmission direction accordingly. This feature will make half duplex RS-485 control under a multitasking OS (e.g. Windows) equivalent to full duplex RS-232.

### Floppy Disk Drive

The PXI-3800 does NOT come equipped with a Floppy Disk Drive in standard configuration. For most applications, the hot-swappable CF card can replace the functionality of a FDD. However, ADLINK will provide an FDD option on request, which will occupy 4 slots (16HP). Please contact an ADLINK sales representative for the Floppy Disk Drive option.

### IEEE-1284 Parallel Port/Printer Interface

The parallel I/O interface signals are routed to the DB-25 connector on the front faceplate. This port supports the full IEEE-1284

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specification and provides a basic printer interface. The BIOS will initialize the parallel port as LPT1 with an ISA I/O base address of 378h. This default configuration also assigns the parallel port to IRQ7. The printer interface mode (Normal, Extended, EPP, or ECP) is selectable through the BIOS menu.

## PXI Trigger I/O Port

The PXI-3800 System Controller provides one PXI trigger I/O port on the front panel for advanced PXI trigger functionality. The TRIG I/O is the software-controlled trigger connection for routing PXI triggers to or from the backplane trigger bus. All trigger lines are compatibility with TTL voltage levels and are edge sensitive. Please refer to Figure 2 for the detailed block diagram of PXI Trigger I/O.

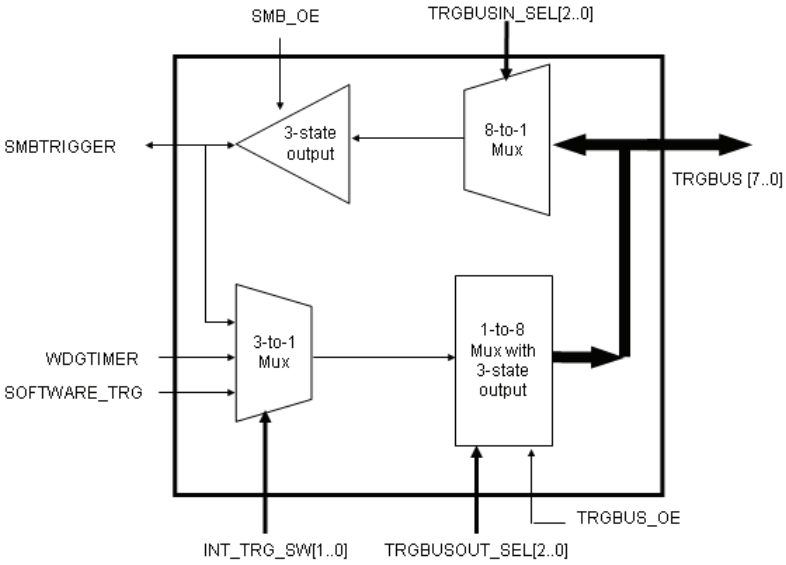



**Figure 1-2: PXI Trigger I/O Block diagram**

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## AC ’97 Multimedia Audio Output

The PXI-3800 System Controller supports an AC ‘97 2.2 compliant audio stereo output with amplifier. Supports multiple sample rates up to 48 kHz.

## Hardware Monitor Function

Two devices provide all the hardware monitor functions of a PXI-3800 system. The ADM1032 provides a CPU temperature monitor with programmable over/under temperature limits and over temperature alarm. The Winbond W83627HF provides system temperature and DC voltage monitoring.

| 83627HF Pin Name | Voltage/ Temperature | Function/Comments |
|---|---|---|
| -12VIN | -12V | +/- 5% |
| +12VIN | +12V | +/- 5% |
| +3.3VIN | +3.3V | +/- 5% |
| VSB | +5VSB | +/- 5% |
| VCOREB | +1.05V | +/- 5% |
| VCOREA | CPU_VCORE | Processor core voltage |
| VTIN1 | | System Temperature |
| VTIN2 | | External Temperature Sensor Input |
| OVT# | | CPU over temperature shutdown output |
| BEEP | | Beep function for hardware monitor |

**Table 1-1: W83627HF Hardware Monitor Inputs**

## Watchdog Timer

The PXI-3800 system implements two watchdog timers. The Intel® 6300ESB provides one 2-stage programmable watchdog timer (WDT) and the W83627HF provides one 1-stage programmable watchdog timer.

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### 6300ESB Watchdog Timer

- Supports selectable prescaler – approximately 1MHz (1us to 1s) and approximately 1KHz (1ms to 10min).
- The 2-stage WDT mode operates as follows: When the first programmed time expires before the counter is reloaded, the WDT generates an IRQ, SMI, or SCI interrupt and loads the second programmed value. If the host still fails to reload the WDT before the second timeout, the WDT drives WDT_TOUT# low and resets PXI-3800 system.

### W83627HF Watchdog Timer

- Watchdog timer is programmable from 1 to 255 seconds.
- Time out will generate interrupt to NMI or RESET, BIOS selectable.

## LED Setting

The PXI-3800 System Controller provides four LEDs on the front panel to display the following information:

- **System Active LED:** This Green LED will turn on after POST; turn off when system is powered off.
- **IDE LED:** This amber LED flashes when the IDE port is accessed.
- **WDT LED:** This Red LED should be off in normal situations. The LED flashes after the WDT is enabled by software. The LED turns on steady when the WDT times out.
- **General Purpose LED:** This Blue LED is a general purpose LED. Customers can define this LED through software.

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## 1.3 Specifications

### PXI/CompactPCI Compliancy

- PXI Specification Rev 2.2
- PICMG 2.0 CompactPCI Rev. 3.0
- PICMG 2.1 CompactPCI Hot-Swap Specification Rev. 1.0

### Form Factor

- Standard PXI 3U form factor (board size: 100mm x 160mm)
- 3-slot (12 HP) width

### CPU/Cache

- Supports Intel® Pentium® M processor, CPU frequency up to 1.8GHz
- Front Side Bus (FSB) frequency: 400MHz
- Cache size: 1MB on-die cache

### Chipset

- Intel® 855GME Graphic Memory Controller Hub (GMCH)
- Intel® 6300ESB I/O Controller Hub

### Host Memory

- Two 200-pin SO-DIMM sockets for DDR SDRAM, up to 2GB with or w/o ECC

### BIOS

- Award PnP BIOS with 4Mb LPC compatible Flash ROM
- BIOS write protection provides anti-virus capability
- DMI BIOS Support: Desktop Management Interface (DMI) allows users to download system hardware-level information such as CPU type, CPU speed, internal/external frequencies, and memory size
- Supports Intel® Pre-Boot Execution Environment (PXE) for remote boot
- Optional OEM BIOS features on request

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- Customized power-on screen
- Remote-console

### CompactPCI Bus Controller

- PLXtech PCI-6540 Univeral PCI-X to PCI-X bridge, supports transparent and non-transparent mode
- PCI-X Rev 1.0 compliant
- Supports 64-bit/66MHz, 64-bit/33MHz, 32-bit/33MHz

### Graphics

- Integrated into 855GME GMCH
- 350MHz integrated 24bit RAMDAC supports analog display pixel resolution up to 1600x1200 at 85Hz and 2048x1536 at 75Hz
- Up to 64MB of dynamic video memory allocation
- Dual independent display pipes support concurrent or simultaneous display on each display device
- Front panel analog VGA DB-15 connector is available
- One DVO port supports digital video output with 165MHz output clock on 12 bit interface with pixel resolution up to 1600x1200 at 85Hz

### Gigabit Ethernet

- Intel® 82545EM Gigabit Ethernet controller provides one 10/100/1000 Mbps Gigabit Ethernet port via a RJ-45 connector on the front panel.
- Standard IEEE 802.3 Ethernet interface
- 64-bit wide interface compliant with PCI 2.3 and PCI-X 1.0a Specifications
- Supports Intel® Pre-Boot Execution Environment (PXE) for remote boot in Windows NT/2000.

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## Onboard Peripherals

- Integrated into Intel® 6300ESB southbridge
- One EIDE connector supports a 2.5” HDD with Ultra ATA 66/100 support
- Four USB 2.0 ports
  - USB 1 and 2 are on the front panel
  - USB 3 is used for USB-to-CF or USB-to-IDE adaptor to support Compact Flash Type II socket on front panel or a 2.5” IDE HDD
- Two CompactFlash Type I/II sockets
  - Supports one CompactFlash Type II interface through IDE interface
  - Supports one CompactFlash Type II drive using USB to CF adaptor
- Supports up to three 16C550 UART compatible COM ports
  - COM1 and COM2 are on front faceplate, COM1 supports RS-232/422/485 (with RS-485+ Auto-Direction control)
- One PXI trigger input/output on front panel
- One AC ‘97  2.2 compliant audio stereo output with amplifier on the front panel. Supports multiple sample rates up to 48KHz.
- One high-speed bi-directional SPP/EPP/ECP parallel port
- One slim type FDD connector
- PS2 keyboard/mouse combo port on front panel

## Front Panel LED Indicators and Reset Button

- Four LEDs on the front panel including System Active LED (Green), IDE LED (Amber), Watchdog timer LED (Red), and General Purpose LED (Blue).
- Flush tact switch for system reset

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## Real-Time Clock and Nonvolatile Memory

The PXI-3800 system provides a century calendar as well as a time of day function. In addition, 256 bytes of battery backed-up RAM are available for use by the BIOS. A separate 3V coin cell battery provides battery backup.

## Environment

- Operating temperature: 0 to 55°C
- Storage temperature: -20 to 80°C
- Humidity: 5% to 95% non-condensed
- Shock: 15G peak-to-peak, 11ms duration, non-operation
- Vibration:
  - Non-operation: 1.88Grms, 5-500Hz, each axis
  - Operation: 0.5Grms, 5-500Hz, each axis, with 2.5” HDD

## Safety Certificate and Test

- CE; FCC Class A
- All plastic material, PCB and Battery used are all UL-94V0 certified

## Power Requirements

| Full loading Configurations | +5V | +3.3V | Total power |
|---|---|---|---|
| Pentium M 1.6G CPU 512MB RAM, 40GB HDD | 3.976A | 2.474A | 28.25W |
| Pentium M 1.1G CPU 512MB RAM, 40GB HDD | 2.468A | 2.215A | 19.65W |

**Table 1-2: Power Requirements**

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**Note:** The above power requirement values are measured on the PXI-3800 with a CPU, 512MB RAM, one mouse, and one internal 40GB slim-type HDD. The CPU is running under 100% loading. Power consumption will be decreased by 500mA for +5V and 300mA for +12V, if the external HDD is removed. Power consumption for all the other peripheral devices such as add-on cards is not included.

## 1.4 Unpacking Checklist

Check the shipping carton for any visible damage. If the shipping carton and contents are damaged, notify the dealer for a replacement. Retain the shipping carton and packing materials for inspection by the dealer. Remember to obtain authorization before returning any products to ADLINK.

Check for the following in the package. If there are any missing items, contact your dealer:

- PXI-3800 Controller (equipped with CPU, RAM and HDD)
- Y-Cable for PS/2 Keyboard and Mouse
- This User's Guide
- ADLINK All-In-One CD

**CAUTION:** This board must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the board. Wear a grounded wrist strap when servicing components.

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# 2 I/O Connectors and Pin Assignment

This chapter provides information about the board outline, connector definitions, and jumper settings to allow users to become familiar with the PXI-3800 before getting use. Included are the following topics:

- PXI-3800 Peripheral Connectivity
- PXI-3800 I/O Connectors
- PXI-3800 Connector Pin Assignments
- PXI-3800 Jumper Settings

## 2.1 Peripheral Connectivity

Table 2-1 lists the peripherals and their corresponding PXI-3800 connectors.

| Peripheral | External Connector | Onboard Connector |
|---|---|---|
| Video | VGA (DB-15) | --- |
| Serial Port | COM1 (DB-9) | --- |
| Serial Port | COM2 (DB-9) | --- |
| Parallel Port | PRN (DB-25) | --- |
| PXI trigger | TRIG (SMB) | --- |
| Keyboard/Mouse | PS/2 (Mini DIN-6) | --- |
| IDE | --- | IDE1 (44-pin) |
| IDE | | IDE2 (44-pin) |
| Supported by USB-to-IDE adapter | | |
| Floppy (optional) | --- | Slim type 26-pin |
| CompactFlash | --- | CF1 Socket |
| CompactFlash | CF2 Socket (Supported by USB-to-CF adaptor) | --- |
| USB 2.0 Port | USB 1,2 (USB 4-pin series) | --- |
| USB 3 | --- | Supports USB-to-CF or USB-to-IDE adaptation |
| Gigabit Ethernet | LAN (RJ-45) | --- |
| Audio speaker output | Y | --- |

**Table 2-1: Peripheral Connectivity Table**

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| Peripheral | External Connector | Onboard Connector |
|---|---|---|
| LEDs | Y | --- |
| Reset button | Y | --- |

**Table 2-1: Peripheral Connectivity Table**

## 2.2 PXI-3800 I/O Connectors

### PXI-3800 Front Panel I/O Connectors

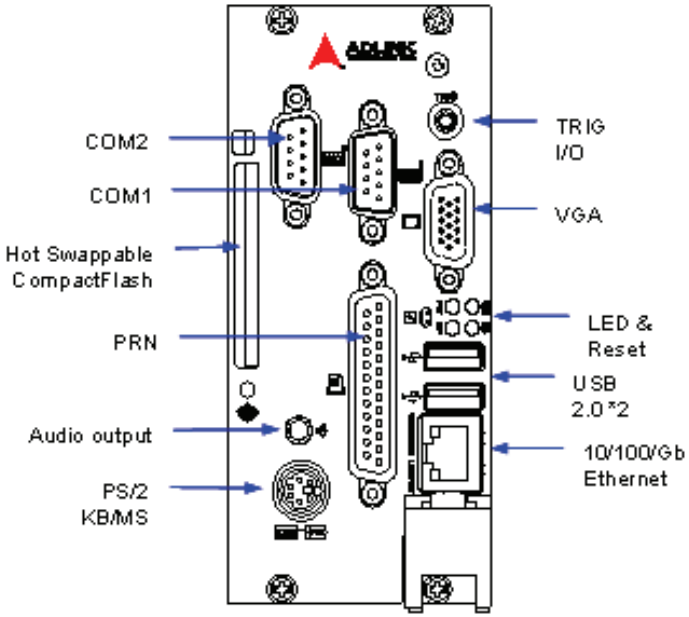



**Figure 2-1: PXI-3800 Front Panel I/O Connectors**

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## PXI-3800 Onboard I/O connectors

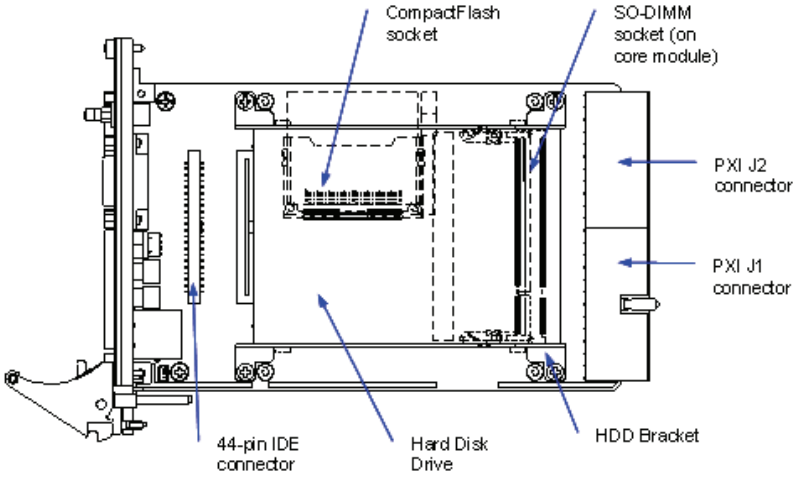



**Figure 2-2: PXI-3800 Onboard I/O Connectors**

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### PXI-3800DB Daughter Board I/O Connectors

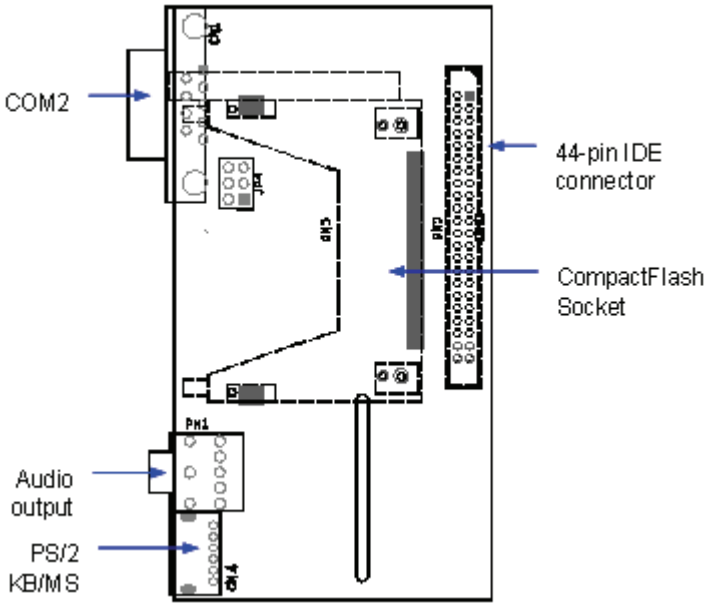
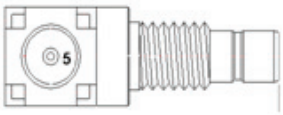



**Figure 2-3: PXI-3800DB Daughter Board I/O Connectors**

## 2.3 PXI-3800 Connector Pin Assignments

### PXI Trigger Connector

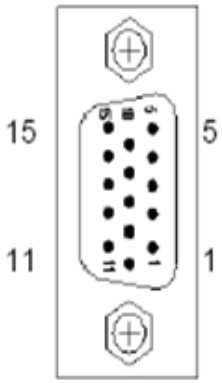


| Pin | Signal | Function |
|---|---|---|
| 1 | GND | Ground |
| 2 | GND | Ground |
| 3 | GND | Ground |
| 4 | GND | Ground |
| 5 | PXI_TRG | PXI trigger signal |

**Table 2-2: PXI Trigger Connector Pin Assignment**

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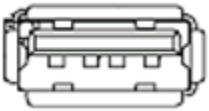
## VGA Connector




| Pin | Signal | Function |
|---|---|---|
| 1 | RED | Analog RED |
| 2 | GREEN | Analog GREEN |
| 3 | BLUE | Analog BLUE |
| 4 | NC | No Connect |
| 5 | GND | Ground |
| 6 | GND | Ground |
| 7 | GND | Ground |
| 8 | GND | Ground |
| 9 | +5V | Power In |
| 10 | GND | Ground |
| 11 | NC | No Connect |
| 12 | DDCDAT | DDC Data for CRT |
| 13 | HSYNC | Horizontal sync for Monitor |
| 14 | VSYNC | Vertical sync for Monitor |
| 15 | DDCCLK | DDC CLK for CRT |

**Table 2-3: VGA Connector Pin Assignment**

## USB port 1, 2 Connector

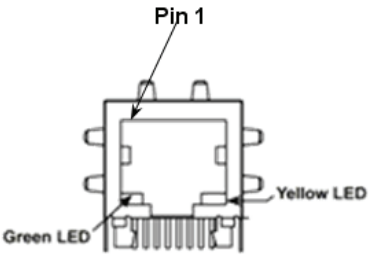


| Pin | Signal | Function |
|---|---|---|
| 1 | USBVCC | Power |
| 2 | USB- | Data (-) |
| 3 | USB+ | Data (+) |
| 4 | USBGND | Ground |

**Table 2-4: USB Connector Pin Assignment**

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## Ethernet (RJ-45) Connector




| Pin | Signal | Function |
|---|---|---|
| 1 | TDP | Transmit Data (+) |
| 2 | TDN | Transmit Data (-) |
| 3 | RDP | Receive Data (+) |
| 4 | LANCT1 | Termination |
| 5 | LANCT2 | Termination |
| 6 | RDN | Receive Data (-) |
| 7 | NC | No Connect |
| 8 | GND | Ground |
| 9 | TDP | Transmit Data (+) |

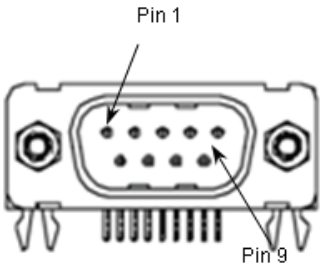
**Table 2-5: Ethernet Connector Pin Assignment**

| Status | | Yellow LED | Green LED |
|---|---|---|---|
| Network link is not established | | OFF | OFF |
| 10 Mbps(10 BaseT) | Link | ON | OFF |
| | Active | Flash | OFF |
| 100 Mbps (100 BaseT) | Link | ON | OFF |
| | Active | Flash | OFF |
| 1000 Mbps (1000 BaseT) | Link | ON | ON |
| | Active | Flash | ON |

**Table 2-6: Ethernet LED Status Definitions**

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## COM1, 2 Serial Port Connector DB-9




| Pin | Signal | Function |
|---|---|---|
| 1 | DCD# | Data Carrier Detect |
| 2 | RXD | Receive Data |
| 3 | TXD | Transmit Data |
| 4 | DTR# | Data Terminal Ready |
| 5 | GND | Ground |
| 6 | DSR# | Data Set Ready |
| 7 | RTS# | Request to Send |
| 8 | CTS# | Clear to Send |
| 9 | RI# | Ring Indicate |

**Table 2-7: COM Connector Pin Assignment**

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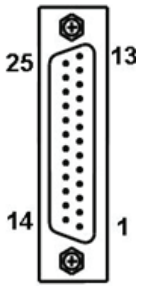
## 44-Pin IDE Connector

| Pin | Signal | Function | Pin | Signal | Function |
|---|---|---|---|---|---|
| 1 | BRSTDRVJ | Reset | 2 | GND | Ground |
| 3 | DD7 | Data 7 | 4 | DD8 | Data 8 |
| 5 | DD6 | Data 6 | 6 | DD9 | Data 9 |
| 7 | DD5 | Data 5 | 8 | DD10 | Data 10 |
| 9 | DD4 | Data 4 | 10 | DD11 | Data 11 |
| 11 | DD3 | Data 3 | 12 | DD12 | Data 12 |
| 13 | DD2 | Data 2 | 14 | DD13 | Data 13 |
| 15 | DD1 | Data 1 | 16 | DD14 | Data 14 |
| 17 | DD0 | Data 0 | 18 | DD15 | Data 15 |
| 19 | GND | Ground | 20 | KEY | - |
| 21 | DDREQ | Request | 22 | GND | Ground |
| 23 | DIOWJ | I/O Write | 24 | GND | Ground |
| 25 | DIORJ | I/O Read | 26 | GND | Ground |
| 27 | IORDY | I/O Ready | 28 | CSEL | Cable Select |
| 29 | DDACKJ | DMA Acknowledge | 30 | GND | Ground |
| 31 | IRQ14 | Interrupt Request | 32 | NC | No Connect |
| 33 | DA1 | Device Address 1 | 34 | 66DECT | ATA 66/100 detect |
| 35 | DA0 | Device Address 0 | 36 | DA2 | Device Address 2 |
| 37 | CS1PJ | Chip Select 1 | 38 | CS3PJ | Chip Select 3 |
| 39 | IDEACTPJ | Device Active | 40 | GND | Ground |
| 41 | +5V | +5V | 42 | +5V | +5V |
| 43 | GND | Ground | 44 | NC | No Connect |

**Table 2-8: IDE 44-pin Connector Pin Assignment**

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## LPT Printer Port Connector DB-25




| Signal Name | Pin | Pin | Signal Name |
|---|---|---|---|
| Line printer strobe | 1 | 14 | AutoFeed |
| PD0, parallel data 0 | 2 | 15 | Error |
| PD1, parallel data 1 | 3 | 16 | Initialize |
| PD2, parallel data 2 | 4 | 17 | Select In |
| PD3, parallel data 3 | 5 | 18 | Ground |
| PD4, parallel data 4 | 6 | 19 | Ground |
| PD5, parallel data 5 | 7 | 20 | Ground |
| PD6, parallel data 6 | 8 | 21 | Ground |
| PD7, parallel data 7 | 9 | 22 | Ground |
| ACK, acknowledge | 10 | 23 | Ground |
| Busy | 11 | 24 | Ground |
| Paper empty | 12 | 25 | Ground |
| Select | 13 | | |

**Table 2-9: LPT Connector Pin Assignment**

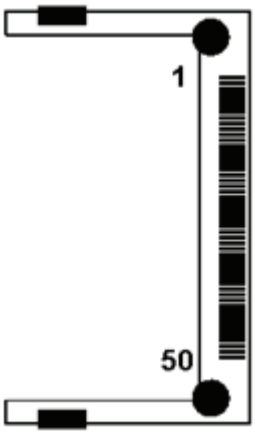
## General Purpose LED definitions

| LED | Color | Status | Description |
|---|---|---|---|
| System Active (PW) | Green | OFF | System power not on or power failure |
| | | ON | Power ON |
| IDE (HD) | Yellow | OFF | IDE idle |
| | | Flash | IDE access |
| WDT (WD) | Red | OFF | WDT not enabled |
| | | Flash | WDT enabled |
| | | ON | WDT timeout occur |
| General Purpose (GP) | Blue | OFF | Board inserted and power on |
| | | ON | Board inserted but not powered on |

**Table 2-10: General Purpose LED Definitions**

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## Compact Flash Type I/II Connector

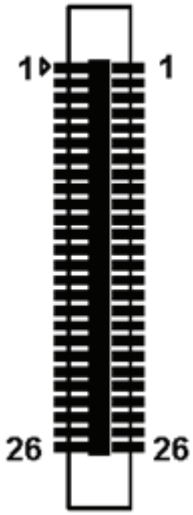



| Signal Name | Pin | Pin | Signal Name |
|---|---|---|---|
| GND | 1 | 26 | GND |
| SDD3 | 2 | 27 | SDD11 |
| SDD4 | 3 | 28 | SDD12 |
| SDD5 | 4 | 29 | SDD13 |
| SDD6 | 5 | 30 | SDD14 |
| SDD7 | 6 | 31 | SDD15 |
| SDCS#1 | 7 | 32 | SDCS#3 |
| GND | 8 | 33 | GND |
| GND | 9 | 34 | SDIOR# |
| GND | 10 | 35 | SDIOW# |
| GND | 11 | 36 | +5V |
| GND | 12 | 37 | IDEIRQ14 |
| +5V | 13 | 38 | +5V |
| GND | 14 | 39 | PCSEL |
| GND | 15 | 40 | NC |
| GND | 16 | 41 | SIDERST# |
| GND | 17 | 42 | SIORDY |
| SDA2 | 18 | 43 | NC |
| SDA1 | 19 | 44 | SDDACK# |
| SDA0 | 20 | 45 | IDEACT# |
| SDD0 | 21 | 46 | S66DECT |
| SDD1 | 22 | 47 | SDD8 |
| SDD2 | 23 | 48 | SDD9 |
| IOIS16# | 24 | 49 | SDD10 |
| GND | 25 | 50 | GND |

**Table 2-11: Compact Flash Connector Pin Assignment**

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## Slim Type FDD connector




| Pin | Signal | Function |
|---|---|---|
| 1 | VCC | Power |
| 2 | INDEX# | Index |
| 3 | VCC | Power |
| 4 | DS0# | Drive 0 Select |
| 5 | VCC | Power |
| 6 | DSKCHG# | Disk Change |
| 7 | NC | |
| 8 | DRATE0 | Data Rate |
| 9 | RPM | Drive Density Select 0 |
| 10 | MTR0# | Motor A On |
| 11 | NC | |
| 12 | FDIR# | Step Direction |
| 13 | NC | |
| 14 | STEP# | Step Pulse |
| 15 | GND | Ground |
| 16 | WDATA# | Write Data |
| 17 | GND | Ground |
| 18 | WGATE# | Write Gate |
| 19 | NC | |
| 20 | TRK0# | Track 0 |
| 21 | NC | |
| 22 | WRTPRT# | Write Protect |
| 23 | GND | Ground |
| 24 | RDATA# | Read Data |
| 25 | GND | Ground |
| 26 | HDSEL# | Head Select |

**Table 2-12: Slim Type Floppy Connector Pin Assignment**

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## PS/2 Keyboard/Mouse Combo Connector (Mini DIN-6)



| Pin | Signal | Function |
|---|---|---|
| 1 | KBDATA | Keyboard Data |
| 2 | MSDATA | Mouse Data |
| 3 | GND | Ground |
| 4 | VCC | Power |
| 5 | KBCLK | Keyboard Clock |
| 6 | MSCLK | Mouse Clock |

**Table 2-13: PS/2 Connector Pin Assignment**

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## J1 Connector Pin Assignment

| Pin | Z | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|
| **J1-25** | GND | +5V | REQ64# | ENUM# | +3.3V | +5V | GND |
| **J1-24** | GND | AD[1] | +5V | V(I/O) | AD[0] | ACK64# | GND |
| **J1-23** | GND | +3.3V | AD[4] | AD[3] | +5V | AD[2] | GND |
| **J1-22** | GND | AD[7] | GND | +3.3V | AD[6] | AD[5] | GND |
| **J1-21** | GND | +3.3V | AD[9] | AD[8] | M66EN | C/BE[0]# | GND |
| **J1-20** | GND | AD[12] | GND | V(I/O) | AD[11] | AD[10] | GND |
| **J1-19** | GND | +3.3V | AD[15] | AD[14] | GND | AD[13] | GND |
| **J1-18** | GND | SERR# | GND | +3.3V | PAR | C/BE[1]# | GND |
| **J1-17** | GND | +3.3V | NC | NC | GND | PERR# | GND |
| **J1-16** | GND | DEVSEL# | GND | V(I/O) | STOP# | LOCK# | GND |
| **J1-15** | GND | +3.3V | FRAME# | IRDY# | GND | TRDY# | GND |
| **J1-12~14** | Keying Area | | | | | | |
| **J1-11** | GND | AD[18] | AD[17] | AD[16] | GND | C/BE[2]# | GND |
| **J1-10** | GND | AD[21] | GND | +3.3V | AD[20] | AD[19] | GND |
| **J1-9** | GND | C/BE[3]# | GND | AD[23] | GND | AD[22] | GND |
| **J1-8** | GND | AD[26] | GND | V(I/O) | AD[25] | AD[24] | GND |
| **J1-7** | GND | AD[30] | AD[29] | AD[28] | GND | AD[27] | GND |
| **J1-6** | GND | REQ0# | GND | +3.3V | CLK0 | AD[31] | GND |
| **J1-5** | GND | NC | NC | RST# | GND | GNT0# | GND |
| **J1-4** | GND | NC | HEALTHY# | V(I/O) | INTP | INTS | GND |
| **J1-3** | GND | INTA# | INTB# | INTC# | +5V | INTD# | GND |
| **J1-2** | GND | TCK | +5V | TMS | TDO | TDI | GND |
| **J1-1** | GND | +5V | -12V | TRST# | +12V | +5V | GND |
| **Pin** | **Z** | **A** | **B** | **C** | **D** | **E** | **F** |

**Table 2-14: J1 Connector Pin Assignment**

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## J2 Connector Pin Assignment

| Pin | Z | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|
| J2-22 | GND | NC | NC | NC | NC | NC | GND |
| J2-21 | GND | CLK6 | GND | NC | RSV | RSV# | GND |
| J2-20 | GND | CLK5 | GND | RSV | GND | RSV | GND |
| J2-19 | GND | GND | GND | SMB_SDA | SMB_SCL | SMB_ALERT# | GND |
| J2-18 | GND | PXI_TRIG3 | PXI_TRIG4 | PXI_TRIG5 | GND | PXI_TRIG6 | GND |
| J2-17 | GND | PXI_TRIG2 | GND | REST# | REQ6# | GNT6# | GND |
| J2-16 | GND | PXI_TRIG1 | PXI_TRIG0 | DEG# | GND | PXI_TRIG7 | GND |
| J2-15 | GND | NC | GND | FAL# | REQ5# | GNT5# | GND |
| J2-14 | GND | AD[35] | AD[34] | AD[33] | GND | AD[32] | GND |
| J2-13 | GND | AD[38] | GND | V(I/O) | AD[37] | AD[36] | GND |
| J2-12 | GND | AD[42] | AD[41] | AD[40] | GND | AD[39] | GND |
| J2-11 | GND | AD[45] | GND | V(I/O) | AD[44] | AD[43] | GND |
| J2-10 | GND | AD[49] | AD[48] | AD[47] | GND | AD[46] | GND |
| J2-9 | GND | AD[52] | GND | V(I/O) | AD[51] | AD[50] | GND |
| J2-8 | GND | AD[56] | AD[55] | AD[54] | GND | AD[53] | GND |
| J2-7 | GND | AD[59] | GND | V(I/O) | AD[58] | AD[57] | GND |
| J2-6 | GND | AD[63] | AD[62] | AD[61] | GND | AD[60] | GND |
| J2-5 | GND | C/BE[5] | GND | V(I/O) | C/BE[4]# | PAR64 | GND |
| J2-4 | GND | V(I/O) | NC | C/BE[7]# | GND | C/BE[6]# | GND |
| J2-3 | GND | CLK4 | GND | GNT3# | REQ4# | GNT4# | GND |
| J2-2 | GND | CLK2 | CLK3 | SYSEN# | GNT2# | REQ3# | GND |
| J2-1 | GND | CLK1 | GND | REQ1# | GNT1# | REQ2# | GND |
| Pin | Z | A | B | C | D | E | F |

**Table 2-15: J2 Connector Pin Assignment**

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## 2.4 PXI-3800 Jumper Settings

The PXI-3800 is designed for maximum flexibility with a minimum number of jumpers. Most of the configuration options can be selected through the BIOS menu. However, some options require configuration by jumper.

**Note:** There is no jumper for Front Side Bus (FSB) or CPU frequency selection. The FSB and CPU frequency are set by auto-detection.

The PXI-3800 is assembled with three boards including one core module, one carrier board, and one daughter board. Table 17 lists the functions of the jumpers on the PXI-3800. Please refer to the figure below for the location of the jumpers on PXI-3800 carrier board and Figure 2-20 for the location of JP4 on the PXI-3800DB daughter board.

| Jumper | Location | Description |
|---|---|---|
| JP7 | PXI-3800 Carrier board | Clear CMOS |
| JP2 | PXI-3800 Carrier board | CF1 Master/Slave Selection |
| JP3~5 | PXI-3800 Carrier board | COM1 RS232/422/RS485 Selection |
| JP4 | PXI-3800DB Daughter board | USB-to-CF/USB-to-IDE selection |

**Table 2-16: Jumpers Definition on the PXI-3800**

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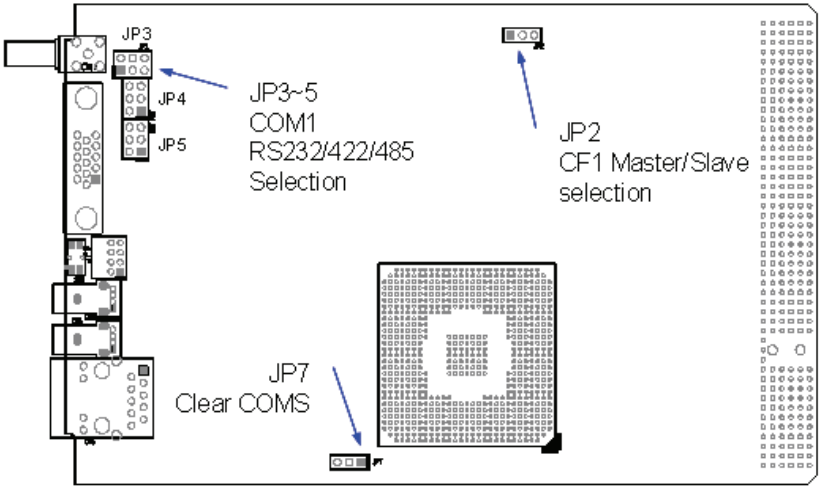



**Figure 2-4: PXI-3800 Carrier Board Jumper Locations**

## Clear CMOS (PXI-3800, JP7)

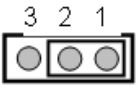
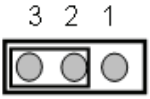
| Status | JP7 |
|---|---|
| Normal operation (Default) |   |
| Clear CMOS |   |

**Table 2-17: Clear CMOS Jumper Setting**

JP7 is a 3-pin jumper that can be used to clear the CMOS memory. The CMOS RAM stores the real time clock (RTC) information, BIOS configuration, and default BIOS settings. The CMOS is powered by a button cell battery when the system is powered off.

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Follow the steps below to clear the CMOS RAM data:

1. Remove the PXI-3800 CPU module from chassis.
2. Short pins 2 and 3 of JP7, then reinstall the jumper back to its normal location.
3. Insert the PXI-3800 back into the chassis. Turn the power on.

## CompactFlash Master/Slave Selection (PXI-3800, JP2)

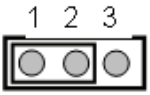
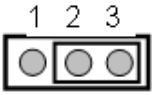
| Status | JP2 |
|---|---|
| CF1 Slave (Default) |  |
| CF1 Master |  |

**Table 2-18: CompactFlash Master/Slave Jumper Setting**

The CompactFlash Master/Slave jumper (JP2) allows the selection of the CF card to be configured as either a master or slave IDE device if there is more than one storage device installed in the system.

## COM port Operation Mode Selection (PXI-3800, JP3~JP5)

By setting the JP3~JP5 jumpers on the PXI-3800 carrier board, COM1 can be selected to operate under RS-232, RS-422, or RS-485 communications protocols. The default factory setting is RS-232 mode.

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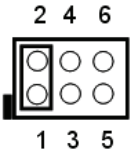
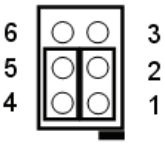
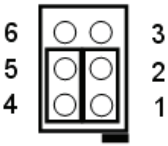
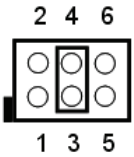
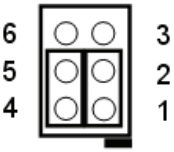
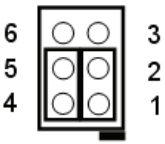
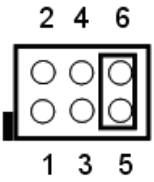
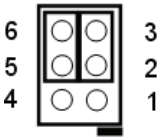
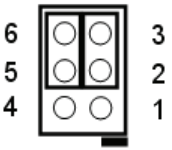
| Type | JP3 | JP4 | JP5 |
|---|---|---|---|
| RS-232 (Default) |  |  |  |
| RS-422 |  |  |  |
| RS-485 |  |  |  |

**Table 2-19: COM port Operation Mode Jumper Setting**

## USB-to-CF/USB-to-IDE Selection (PXI-3800DB, JP4)

By setting the JP4 jumper on the PXI-3800DB daughter board, the USB port can be set to either USB-to-CF or USB-to-IDE adaptation to support a CompactFlash socket on front panel or a 2.5” IDE HDD. The default factory setting is USB-to-CF mode.

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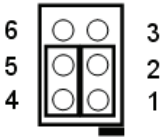
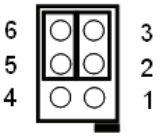
| Status | JP4 |
|---|---|
| Enable USB-to-CF (Default) |   |
| Enable USB-to-IDE |   |

**Table 2-20: USB-to-CF/USB-to-IDE Selection Jumper Setting**

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# 3 Getting Started

This chapter gives a summary of what is required to set up an operating system using the PXI-3800. Hardware installation and BIOS setup are also discussed. Note that the PXI-3800 is shipped with CPU, RAM and HDD preinstalled. The installations of the CPU, RAM, and HDD are done at the ADLINK factory and the procedures described in the following sections are for users' reference. If the default configuration does not suit your application needs, contact a local ADLINK dealer for special configurations or OEM versions.

## 3.1 Installing the PXI-3800

Use the following procedure to install the PXI-3800 controller into a PXI chassis. Consult your PXI chassis user guide for specific instructions and warnings.

**Step 1:**

Plug in your chassis before installing the PXI-3800. Make sure the system power is turned off.

**Step 2:**

Remove the blank face panel from the system slot.

**Step 3:**

Align the top and bottom edges of the board with the card guides on the chassis, then slide the board into the chassis until resistance is felt.

**Step 4:**

Move the locking handle in an inward direction until it is fully latched. Please note that slight resistance will be felt while inserting the board. If this resistance is more than under normal conditions, check to ensure that there are no bent pins on the backplane and that the board's connector pins are aligned properly with the connectors on the backplane.

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**Step 5:**

Verify that the board is seated properly. Secure the four screws at the top and bottom of the front panel; connect the appropriate cables to the board. The system can now be powered on.

Figure 3-1 shows a PXI-3800 being installed in the system slot of an ADLINK PXIS-2506 chassis.



**Figure 3-1: PXI-3800 System Controller being installed in a PXI Chassis**

## How to Remove the Controller from the PXI Chassis

**Step 1:**

Power off the chassis.

**Step 2:**

Loosen the four screws in the front panel.

**Step 3:**

Press down on the ejector handle.

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**Step 4:**

Slide the controller out of the chassis.

## 3.2 Memory Module Installation

The PXI-3800 controller has two 200-pin DDR SO-DIMM sockets and supports up to 2GB RAM. The memory module that comes with the standard PXI-3800 is a 512MB SDRAM module. You can upgrade the amount of installed RAM by changing the SO-DIMM module or adding a second SDRAM module. It is necessary to disassemble the PXI-3800 to install an SDRAM module in either the DM1 or DM2 socket on the PXI-3800 main board (one on each side), so we recommend that users have SDRAM installed professionally by ADLINK.

For applications requiring memory other than the standard 512MB, please contact a local ADLINK dealer for details.

### Installing the first memory module

Please refer to Figure 3-2 below to install the first memory module. After removing the heatsink, insert the module at a 30 degree angle and push the module firmly but gently into the slot until the security latches on the socket have locked into place on both sides of the module.

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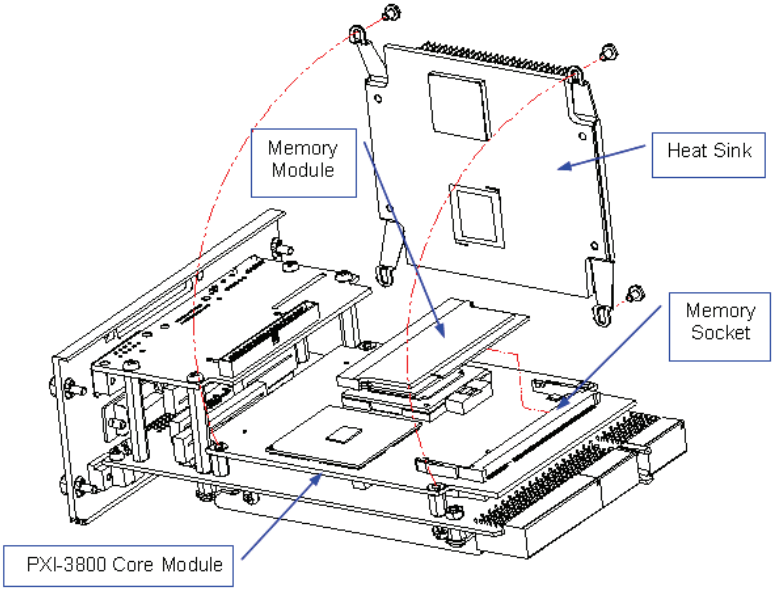



**Figure 3-2: First Memory Module Installation (preinstalled by ADLINK)**

## Installing the second memory module

After carefully removing the PXI-3800 Core Module from the Carrier Board, insert the second memory module into the slot on the underside of the Main Board as shown in Figure 3-3 below using the same procedure as described above for installation of the first memory module.

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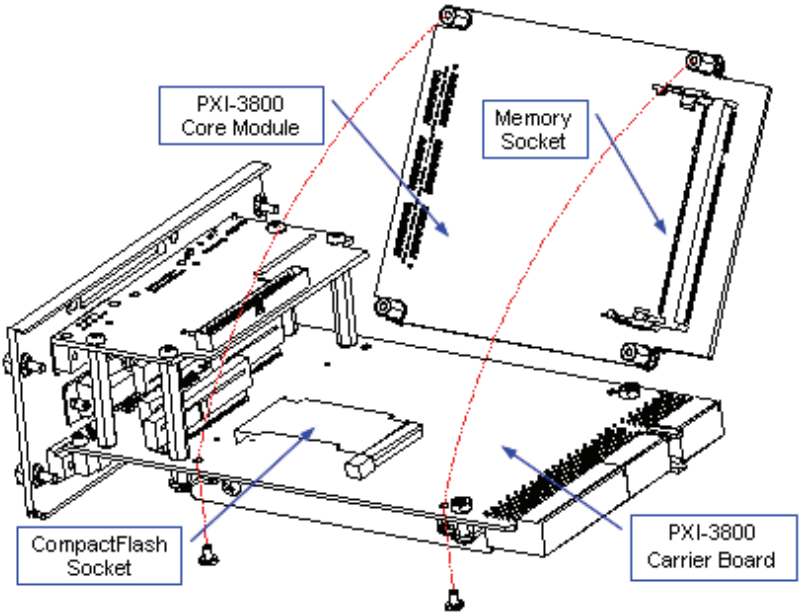



**Figure 3-3: Second Memory Module Installation**

## 3.3 HDD and CF Installation

The PXI-3800 is equipped with a set of slim-type HDD mounting brackets that accommodate a 2.5 inch IDE hard drive. A 40GB HDD is installed by default. For applications with different hard drive requirements, please contact a local ADLINK dealer for details.

You may purchase an off-the-shelf 2.5” HDD. However, due to space limitations and ventilation considerations, a low profile 2.5” HDD that is no thicker than 9.5mm is recommended.

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## HDD Installation

To change the HDD, follow these procedures carefully:

**Step 1:**

Check that the jumper setting of JP2 on the PXI-3800 is across pins 1 and 2.

**Step 2:**

Screw the HDD to the hard drive mounting bracket. Please note the orientation of the HDD. The HDD's pin #1 must match the location of IDE connector pin #1.

**Step 3:**

Install the HDD with mounting bracket plate on the Core Module of the PXI-3800

**Step 4:**

Use four copper stand-off screws to fasten the HDD to the Core Module

**Step 5:**

Connect a 44-pin HDD cable to the HDD. Ensure that pin #1 of the IDE connector, cable and the HDD are properly matched.

## CompactFlash Card Installation

The CompactFlash Card (or CF storage card) is widely used in digital consumer devices like PDAs, digital cameras, and MP3 players. The CF format features anti-shock and anti-vibration properties, improved environmental tolerance, low power consumption, a small form factor, and higher reliability. Plus, it has been widely accepted in the industrial and embedded application field.

The PXI-3800 has an internal as well as an external CompactFlash socket. Please see Figure 3-3 for the internal CF socket location. To install the internal CompactFlash socket which can be used as HDD replacement, simply insert the CF card into the socket. To remove it, push the ejector button on the side of the socket and extract the card. Please note that the internal CF inter-

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face is NOT hot swappable, and installation or removal should be done when the system power is off. The external CF interface is hot swappable so users can install or remove via the front panel while the system is running.

## 3.4 BIOS Configuration Overview

The Basic Input/Output System (BIOS) is a program that provides the basic level of communication between the processor and peripherals. In addition, the BIOS also contain code for various advanced features found in the system board. The BIOS setup program includes menus for configuring settings and enabling PXI-3800 controller features. Most users do not need to use the BIOS setup program, as the PXI-3800 controller ships with default settings that work well for most configurations. Please refer to the BIOS Manual in the ADLINK All-In-One CD for more detail information about the BIOS and other utilities. You can find the manual under the directory:

X:\Manual\PXI Platform\PXI Controller\PXI-3800

**CAUTION:** Changing BIOS settings may lead to incorrect controller behavior and possibly an unbootable controller. If this happens, follow the instructions in Section 2.4 to clear CMOS and restore the default settings. In general, do not change a BIOS setting unless you are absolutely certain of what it does.

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## 3.5 Operating System Installation

For more detailed information about the operating system, refer to the documentation provided by the operating system vendor.

PXI/CompactPCI devices are automatically configured by the BIOS during the boot sequence.

Most operating systems require initial installation on a hard drive from a floppy or a CD-ROM drive. These devices should be configured, installed, and tested with the supplied drivers before attempting to load the new operating system.

Read the release notes and installation documentation provided by the operating system vendor. Be sure to read all the README files or documents provided on the distribution disks, as these typically note documentation discrepancies or compatibility problems.

Select the appropriate boot device order in the SETUP/BIOS boot menu depending on the OS installation media used. For example, if the OS includes a bootable installation CD, select USB CD-ROM as the first boot device and reboot the system with the installation CD installed in the USB CD-ROM drive.

Proceed with the OS installation as directed and be sure to select appropriate device types if prompted. Refer to the appropriate hardware manuals for specific device types and compatibility modes of ADLINK PXI products.

When installation is complete, reboot the system and set the boot device order in the SETUP boot menu appropriately.

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## 3.6 Boot PXI-3800 via USB ports or CompactFlash sockets

This section describes how to boot PXI-3800 via USB ports or CompactFlash sockets (onboard or on the front panel). Please follow the instructions below:

### Boot from USB-CDROM Drive

**Step 1:**

Connect the USB CDROM Drive via a USB port on the front panel.

**Step 2:**

Put a boot CD in the USB CDROM Drive.

**Step 3:**

Power on the PXI-3800 and enter BIOS to modify the Boot Device setting as follows:

Advanced BIOS Features > First Boot Device [USB-CDROM]

**Step 4:**

Save the change

**Step 5:**

Reboot the system

### Boot from USB Floppy Drive

**Step 1:**

Connect USB Floppy Drive via a USB port on the front panel.

**Step 2:**

Put a boot disk in the USB Floppy Drive.

**Step 3:**

Power on the PXI-3800 and enter BIOS to modify the Boot Device setting as follows:

Advanced BIOS Features > First Boot Device [USB-FDD]

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**Step 4:**

Save the change

**Step 5:**

Reboot the system

### Boot from the front panel CompactFlash Drive

**Step 1:**

Put a boot CF disk in the CompactFlash socket on the front panel.

**Step 2:**

Power on the PXI-3800 and enter BIOS to modify the Boot Device setting as follows.

Advanced BIOS Features > First Boot Device [USB-HDD]

**Step 3:**

Save the change

**Step 4:**

Reboot the system

### Boot from the onboard CompactFlash Drive

**Step 1:**

Put a boot CF disk in the CompactFlash socket embedded inside the PXI-3800.

**Step 2:**

Power on the PXI-3800 and enter BIOS to modify the Boot Device setting as follows.

Advanced BIOS Features > First Boot Device [HDD-1]

**Step 3:**

Save the change

**Step 4:**

Reboot the system

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# 4 Driver Installation

The driver installation instructions for Windows 2000 and Windows XP are described below.

To install Windows drivers:

**Step 1:**

Fully install Windows properly before installing any drivers. Most of the standard I/O device drivers have been included in Windows.

**Step 2:**

Install the chipset driver.

**Step 3:**

Install the VGA driver.

**Step 4:**

Install the LAN driver.

**Step 5:**

Install the Audio driver.

**Step 6:**

Install the PXI Trigger driver.

To ensure compatibility, it is recommended that the chipset, VGA, LAN, Audio, and PXI Trigger drivers provided in the ADLINK All-In-One CD are used. For Linux drivers, please contact ADLINK.

To install the Windows drivers for the PXI-3800 system controller, refer to the installation information in this chapter. For installation information for non-Windows operating systems, please contact an ADLINK service center. The Windows drivers are located in the following directories of the ADLINK All-In-One CD:

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| | |
|---|---|
| Chipset driver | \Driver Installation\PXI Platform\PXI controller\PXI-3800\chipset\Win2KXP |
| VGA driver | \Driver Installation\PXI Platform\PXI controller\PXI-3800\VGA\ |
| LAN driver | \Driver Installation\PXI Platform\PXI controller\PXI-3800\LAN\ |
| Audio driver | \Driver Installation\PXI Platform\PXI controller\PXI-3800\Audio\ |
| PXI Trigger driver | \Driver Installation\PXI Platform\PXI controller\PXI-3800\PXI_Trigger\ |

The Bus-mastering IDE drivers are automatically installed by Windows.

For using USB 2.0, please update to the newest Windows Service Pack.

## 4.1 Chipset Driver Installation

This section describes the system requirements of Intel® 855GME chipset device drivers. The drivers are designed for and tested with Windows 2000/XP. The system must contain a supported Intel processor and chipset configuration. Ensure that a mouse is connected to the system. One of the following versions of Windows 2000/XP must be installed on the system prior to running the utility program.

- Windows XP Version 2002 (Original release)
- Windows 2000 5.00.2195 (Original release)

### Installing Hardware Configuration File

Follow the instructions below to install the hardware configuration file on a Windows 2000/XP system.

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**Note:** Record the location of the Windows 2000/XP directory before installing the drivers.

**Step 1:**

Check the System Requirements. Windows 2000/XP must be fully installed and running on the system prior to running this software.

**Step 2:**

Close any running applications.

**Step 3:**

The files are stored in an integrated Windows 2000/XP application setup program.

**Step 4:**

Insert the ADLINK All-In-One CD, run the infinst_enu.exe file at

**X:\Driver Installation\PXI Platform\PXI controller\PXI-3800\chipset\Win2kXP** (where X is the CD-ROM drive).

**Step 5:**

Click **Next** on the Welcome Screen to read and agree to the license agreement. Click **Yes** if you agree to continue. NOTE: If you click No, the program will terminate.

**Step 6:**

Click **Next** on the Readme Information screen to install INF files.

**Step 7:**

Click **Finish** to restart the system when prompted.

**Step 8:**

Follow the screen instructions and use default settings to complete setup when Windows 2000/XP restarts. Upon restart, Windows may display a dialog box announcing new hardware has been found and installs drivers for them. If a New Hardware Found dia-

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log box is displayed requesting the location of the drivers, click on the scrollbar and select the Windows directory.

**Step 9:**

Select **Yes**, when prompted to restart Windows.

## 4.2 VGA Driver Installation

This section describes the VGA driver installation for the onboard VGA controller Intel® 855E GMCH2. The relative drivers are located in **X:\Driver Installation\PXI Platform\PXI Controller\PXI-3800\VGA** of the ADLINK All-In-One CD, where X: is the drive letter of the CD-ROM drive. The VGA drivers for Windows 2000/XP and Linux are included.

Windows 2000 and Windows XP may try to install the standard VGA driver. To ensure compatibility, manually install the latest driver, which is included in the ADLINK All-In-One CD. To update to the new driver, follow the steps below:

**Step 1:**

Boot Windows and execute the win2k_xp149.exe file under this directory: X:\Driver Installation\PXI Platform\PXI controller\PXI-3800\VGA\Win2kXP

**Step 2:**

Follow the prompts. The VGA driver will automatically be installed onto the system.

**Step 3:**

Restart the system.

| | |
|---|---|
| **Note:** | After installing the VGA/AGP drivers in Windows, it is possible to find the drivers not working correctly. This may be caused by failing to install the Windows service pack beforehand. Ensure that the Windows service pack is installed to enable AGP capability. |

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## 4.3 LAN Driver Installation

This section describes the LAN driver installation for the onboard Intel® 82545EM Gigabit Ethernet controller. The drivers included in the ADLINK All-In-One CD support Windows 2000/XP and Linux.

Windows 2000/XP will attempt to install a LAN driver automatically. To ensure compatibility, manually install the latest LAN driver, which is stored on the ADLINK All-In-One CD. After installing Windows 2000/XP, update to the new driver by following these procedures:

**Step 1:**

Boot Windows and execute the pro2kxp.exe file under the directory: **X:\Driver Installation\PXI Platform\PXI controller\PXI-3800\LAN\Win2kXP**

**Step 2:**

Following prompt instructions, The LAN driver will automatically be installed on the system.

**Step 3:**

Restart the system.

## 4.4 Audio Codec Driver Installation

This section outlines the Audio Codec driver installation for the onboard AC97' Codec. The drivers included on the ADLINK All-In-One CD support Windows 2000/XP and Linux. Follow the instructions below to install the Audio driver for Windows 2000/XP.

**Step 1:**

Execute the wdm_a365.exe file in the following path location:

**X:\Driver Installation\PXI Platform\PXI controller\PXI-3800\Audio\Win2kXP**

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**Step 2:**

Click **Next** on the Welcome audio setup screen to install driver.

**Step 3:**

Finally, click **Finish** to restart.

## 4.5 PXI Trigger Driver Installation

This section outlines the PXI Trigger driver installation. The driver included on the ADLINK All-In-One CD supports Windows 2000. To install the driver for PXI Trigger, follow the instructions below:

**Step 1:**

Execute the setup.exe file in the following path location:

**X:\Driver Installation\PXI Platform\PXI controller\PXI-3800\PXI_Trigger\Win2k**

**Step 2:**

Click **Next** on the Welcome PXI Trigger setup screen to install the driver.

**Step 3:**

Finally, click **Finish** to restart.

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# 5 Utilities

This chapter explains extended functions of the PXI-3800 controller, including watchdog timer (WDT), Intel Pre-boot Execution Environment (PXE) and hot swappable function.

## 5.1 Watchdog Timer Overview

PXI-3800 has two different type watchdog timers (WDT), one is integrated into the south bridge 6300ESB and another is integrated into the super I/O W83627HF. The primary function of the WDT is to monitor the PXI-3800 operation and to generate IRQs and send a signal to PXI Trigger or reset the system if the software fails to function as programmed. The major features of the watchdog timer are:

1. Enabled and disabled through software control
2. Armed and strobed through software control

### Intel® 6300ESB ICH Watchdog Timer

The Intel® 6300ESB ICH includes a two-stage Watchdog Timer (WDT) that provides a resolution ranging from one micro second to ten minutes. The timer uses a 35-bit Down-Counter. The counter is loaded with the value from the first Preload register. The timer is then enabled and starts counting down. The time at which the WDT first starts counting down is called the first state. If the host fails to reload the WDT before the 35-bit down counter reaches zero the WDT generates an internal interrupt. After the interrupt is generated, the WDT loads the value from the second Preload register into the WDT's 35-bit Down-Counter and starts counting down. The WDT is now in the second stage. If the host still fails to reload the WDT before the second timeout, the WDT drives the WDT_TOUT# pin low. The WDT_TOUT# pin is held low until the system is reset. Users can choose to reset the system or send a PXI Trigger signal through BIOS WDT setting.

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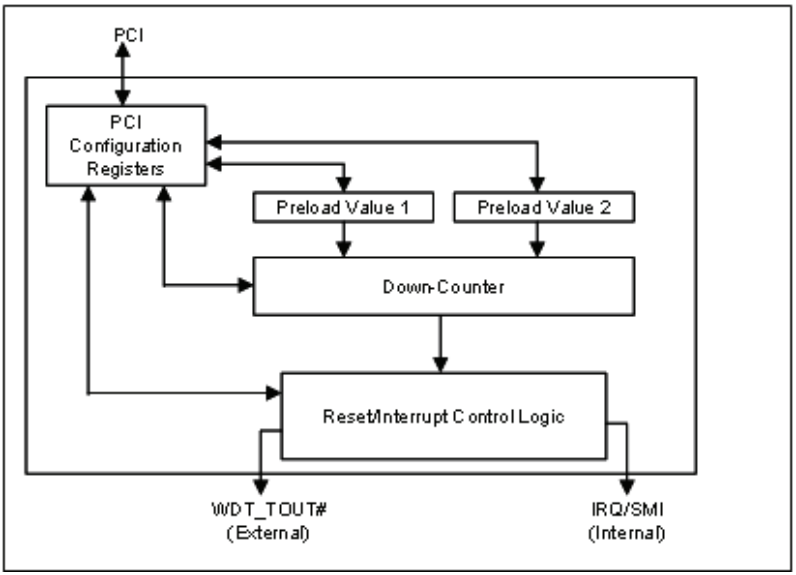



**Figure 5-1: Intel® 6300ESB Watchdog Timer Architecture**

## Configuration Registers

The Intel® 6300ESB WDT appears to BIOS as PCI Bus -0, Device 29, Function 4, and has the standard set of PCI Configuration register. The configuration registers are described below.

### Offset 10H: Base Address Register (BAR)

This register determines the memory base for WDT down-counter setting. It will be used to set Preload value 1 register, Preload value 2 register, General Interrupt Status register and Reload register.

### Preload Value 1& 2 registers

These two registers are used to hold the preload value for the WDT timer. Its value will be automatically transferred into the down-counter every time the WDT enters the first stage and

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second stage. Preload Value 1 register locates at Base + 00H and Preload Value 2 register locates at Base + 04H. Only bit [19:0] can be set.

The register unlocking sequence is necessary when writing to the Preload registers. The procedure of writing a value into preload value 1 and 2 register is as follows:

1. Write 80H to offset BAR + 0CH.
2. Write 86H to offset BAR + 0CH.
3. Write desired value to preload register. (BAR + 00H or BAR + 04H)

**General Interrupt Status Register**

This register is at Base + 08H. Bit 0 is set when the first stage of down-counter reaches zero.

Bit 0 = 0 – No Interrupt

Bit 1 = 1 – Interrupt Active

**Reload Register**

This register is at Base + 0CH. Write 1 to bit 8 will reload the down-counter's value. Instructions on preventing a timeout is as follows:

1. Write 80H to offset BAR + 0CH.
2. Write 86H to offset BAR + 0CH.
3. Write a '1' to RELOAD[8] of the reload register.

**Offset 60 – 61H: WDT Configuration Register**

Bit 5 indicates whether or not the WDT will toggle the WDT_TOUT# pin when WDT times out. (0=Enabled, 1=Disabled)

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Bit 2 provides two options for prescaling the main down-counter. (0=1ms – 10min, 1=1us—1sec)

Bit [1:0] allows the user to choose the type of interrupt when the WDT reaches the end of the first stage without being reset. (00 = IRQ, 01 = reserved, 10 = SMI, 11 = Disabled)

**Note:** At present, the WDT does not support SMI. IRQ uses APIC 1, INT 10 and it is active low, level triggered.

**Offset 68H: WDT Lock Register**

Bit 1 enables or disables the WDT. (0 = Disabled, 1 = Enabled)

Bit 0 will lock the values of this register until a hard reset occurs or power is cycled. (0 = unlocked, 1 = locked) The default is Unlocked.

## GPIO Control Registers

There are three GPIOs on the PXI-3800 related to the watchdog timer. They are listed as follows. The GPIO control base port is 480H.

**WDT_TOUT# pin selection**

The WDT_TOUT# signal is multiplexed with GPIO32. When using WDT, this signal must be switched to WDT_TOUT# function. It uses bit 0 of GPIOBASE + 30H to set WDT_TOUT function. (0 = WDT_TOUT#, 1 = GPIO32)

**RESET hardware circuit selection**

GPO24 of the 6300ESB is designed to control the reset circuit. When GPO24 is low, the system will reset according to the level of the WDT_TOUT# signal. When GPO24 is high, the system will not be reset by WDT_TOUT#. Set bit 24 of GPIOBASE + 04H to 0 for output use. Bit 24 of GPIOBASE + 0CH

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determines the level of GPO24 (0 = Low, 1 = High). A setting already exists in the BIOS setup menu. The user can set this item before programming WDT.

**WDT LED Control**

GPO25 of the 6300ESB is designed to control WDT LED. Two features of the WDT LED are supported on PXI-3800. WDT LED lights or blinks.

**WDT LED lights:** Set bit 25 of GPIOBASE + 04H to 0. Bit 24 of GPIOBASE + 0CH determines the state of WDT LED. (0 = light, 1= dark)

**WDT LED blinks:** Set bit 25 of GPIOBASE + 04H to 0. Bit 25 of GPIOBASE + 18H enables WDT LED blinking function. (0 = function normally, 1 = enable blinking) The high and low times have approximately 0.5 seconds each.

## WDT Programming Procedure

**Step 1:**

Set BIOS Setting in Integrated Peripherals\Onboard Device Page Watch Dog Timer Item to “Enabled”.

**Step 2:**

Make sure WDT_TOUT# signal is functional. (Not GPIO32 function).

**Step 3:**

Set WDT output enable, presecaler and interrupt type into WDT configuration register.

**Step 4:**

Obtain control base from Base Address register.

**Step 5:**

Program Preload register’s value according to unlocking sequence.

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**Step 6:**

Set WDT timer mode into WDT Lock Register.

**Step 7:**

Enable WDT from WDT Lock register and program the functionality of WDT LED.

To prevent the timer from causing an interrupt or driving WDT_TOUT#, the timer must be reloaded periodically. The frequency of reloads required is dependent on the value of the preload values. To reload the down-counter, the register unlocking sequence must be performed.

If the user wishes to disable WDT, set bit 1 of WDT lock Register to 0.

## W83627HF (Super IO) Watchdog Timer

The W83627HF watchdog timer circuit is implemented in a programmable logic device. The watchdog timer contains a "Control and Status Register." The register allows the BIOS or user application to determine if a watchdog time out was the source of a particular reset. The timeout period is 1-255 seconds. The watchdog is normally strobed by reading the Watchdog Register (3F0h). IF the host fails to reload the WDT before the timeout, the WDT drives the WDT_TOUT# pin low. Users can choose to reset the system or send a PXI Trigger signal through BIOS WDT setting.

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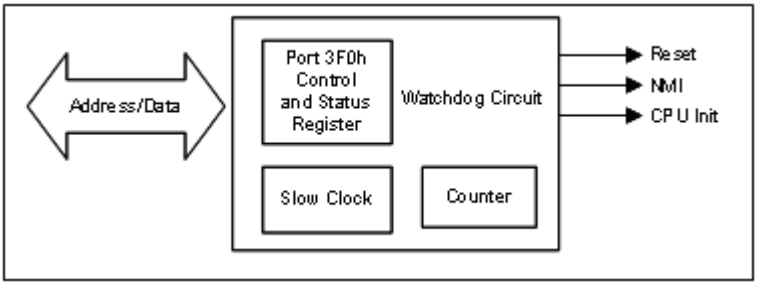



**Figure 5-2: W83267HF Watchdog Timer Architecture**

## 5.2 Intel Preboot Execution Environment (PXE)

The PXI-3800 series supports the Intel Preboot Execution Environment (PXE), which provides the capability of boot-up or executing an OS installation through Ethernet ports. There should be a DHCP server in the network with one or more servers running PXE and MTFTP services. It could be a Windows NT or Windows 2000 server running DHCP, PXE and MTFTP service or a dedicated DHCP server with one or more additional server running PXE and MTFTP service. This section describes the major items required for building a network environment with PXE support.

**Step 1:**

Setup a DHCP server with PXE tag configuration

**Step 2:**

Install the PXE and MTFTP services

**Step 3:**

Make boot image file on PXE server (that is the boot server)

**Step 4**

Enable the PXE boot function on the client computer

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For more detailed information, please refer to pdkrel30.pdf under the directory:

**X:\Utility\PXE_PDK**

## 5.3 PICMG 2.1 Hot Swap Support

The PXI-3800 Hot-Swap capability allows non-system slot boards to be added or removed while the system is powered up. PXI-3800 provides independent clocks for each slot and accesses to the ENUM# signal on the backplane, which are compatible with PICMG 2.1 Hot Swap Specification. However, the PXI-3800 itself is not hot swappable.

The hot swappable system is dependent on system controller, peripheral modules, backplane, operating system, driver, application support. If users use I/O modules that are designed to be hot swappable, please contact ADLINK for hot swap function support.

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# Appendix A PXI Trigger Function Description

This appendix provides a description of PXI Trigger functions, including data types and function reference.

## Data Types

We have defined some data types in the PXI-3800 header file. This header file can be found in P3800.H under the directory **X:\ADLINK\PXI3800\Include** after running the setup.exe file (where X is the drive you install the driver). These data types are used by the PXI-3800 Library. It is recommended that you use these data types in your application programs. The following table lists the data type names, their ranges, and the corresponding data types in C/C++, Visual Basic and Delphi.

| Type Name | Description | Range | Type | | |
|---|---|---|---|---|---|
| | | | C/C++ ( for 32-bit compiler) | Visual Basic | Pascal (Delphi) |
| U8 | 8-bit ASCII character | 0 to 255 | Unsigned char | Byte | Byte |
| I16 | 16-bit signed integer | -32768 to 32767 | Short | Integer | SmallInt |
| U16 | 16-bit unsigned integer | 0 to 65535 | Unsigned short | Not supported by BASIC, use the signed integer (I16) instead | Word |
| I32 | 32-bit signed integer | -2147483648 to 2147483647 | Long | Long | LongInt |

**Table 1-1: Data Types**


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| | | | | | |
|---|---|---|---|---|---|
| U32 | 32-bit unsigned integer | 0 to 4294967295 | Unsigned long | Not supported by BASIC, use the signed long integer (I32) instead | Cardinal |
| F32 | 32-bit single-precision floating-point | -3.402823E38 to 3.402823E38 | Float | Single | Single |
| F64 | 64-bit double-precision floating-point | -1.797683134862315E308 to 1.797683134862315E309 | Double | Double | Double |

**Table 1-1: Data Types**

## Function Reference

### P3800_Close

#### @ Description

This function is used to tell the PXI-3800 library that a registered card is not currently used and can be released, making room for the new card to register. At the end of a program, use this function to release all cards that were registered.

#### @ Cards Support

PXI-3800

#### @ Syntax

**Microsoft C/C++, Linux C/C++ and Borland C++**

```
I16 P3800_Close (U16 CardNumber)
```



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**Visual Basic**

```
P3800_Close (ByVal CardNumber As Integer) As
Integer
```

**@ Parameter**

**CardNumber:** The card ID of the card that want to be released.

**@ Return Code**

```
NoError
```

## P3800_GetGPIOBase

**@ Description**

Get the GPIO base address of the PXI-3800.

**@ Cards Support**

PXI-3800

**@ Syntax**

**Microsoft C/C++, Linux C/C++ and Borland C++**

```
I16 P3800_GetGPIOBase(U16 wCardNumber, U32
*BaseAddr)
```

**Visual Basic**

```
P3800_GetGPIOBase (ByVal CardNumber As Integer,
BaseAddr As Long) As Integer
```

**@ Parameter**

**CardNumber:** The card ID of the card to retrieve the DPIO address.

**Base Addr:** Returns the GPIO base address.


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### @ Return Code

```
NoError
```

## P3800_Init

### @ Description

Initializes the hardware and software states of a PXI-3800 device, and returns a numeric card ID that corresponds to the card initialized. P3800_Init must be called before any other PXI-3800 library functions can be called for that card. The function initializes the card and variables internal to the PXI-3800 library.

### @ Cards Support

PXI-3800

### @ Syntax

**Microsoft C/C++, Linux C/C++ and Borland C++**

```
I16 P3800_Init (U16 card_num)
```

**Visual Basic**

```
P3800_Init (ByVal card_num As Integer) As Integer
```

### @ Parameter

**card_num:** The sequence number of the device. This must be zero.

### @ Return Code

This function returns a numeric card ID for the card initialized. A negative error code would be returned in the even of an error. Possible error codes:

```
ERR_InvalidBoardNumber, ERR_BoardNoInit,
ErrorOpenDriverFailed, ERR_OpenDriverFail,
ERR_GetGPIOAddress, ERR_BoardBusy
```



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## P3800_SetSoftTrg

### @ Description

Generates a software trigger signal.

### @ Cards Support

PXI-3800

### @ Syntax

**Microsoft C/C++, Linux C/C++ and Borland C++**

```
I16 P3800_SetSoftTrg (U16 wCardNumber, U8 status)
```

**Visual Basic**

```
P3800_SetSoftTrg (ByVal CardNumber As Integer,
ByVal status As Byte) As Integer
```

### @ Parameter

**CardNumber:** The card ID of the card to perform this operation.

**status:** The trigger status.

Possible statuses:

1: High

0: Low

### @ Return Code

```
NoError, ERR_SoftTrg_Out
```

## P3800_Trigger_Clear

### @ Description

Resets all trigger routing configuration to the default settings.


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### @ Cards Support

PXI-3800

### @ Syntax

**Microsoft C/C++, Linux C/C++ and Borland C++**

```
I16 P3800_Trigger_Clear (U16 wCardNumber)
```

**Visual Basic**

```
P3800_Trigger_Clear (ByVal CardNumber As Integer)
As Integer
```

### @ Parameter

**CardNumber:** The card ID of the card to perform this operation.

### @ Return Code

```
NoError, ERR_Trigger_Clr
```

## P3800_Trigger_Route

### @ Description

Configures the source, destination, and halfway of the trigger path.

### @ Cards Support

PXI-3800

### @ Syntax

**Microsoft C/C++, Linux C/C++ and Borland C++**

```
I16 P3800_Trigger_Route(U16 wCardNumber, U32
      source, U32 dest, U32 halfway)
```



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### Visual Basic

```
P3800_Trigger_Route (ByVal CardNumber As Integer,
ByVal source As Long, ByVal dest As Long, ByVal
halfway As Long) As Integer
```

### @ Parameter

**CardNumber:** The card ID of the card to perform this operation.

**Source:** The trigger signal source or the starting point of the trigger path. Possible values of source:

P3800_VAL_WDT

P3800_VAL_SMB

P3800_VAL_SOFT

P3800_VAL_TTL0

P3800_VAL_TTL1

P3800_VAL_TTL2

P3800_VAL_TTL3

P3800_VAL_TTL4

P3800_VAL_TTL5

P3800_VAL_TTL6

P3800_VAL_TTL7

**dest:** The endpoint of the trigger path. Possible values of destination:

P3800_VAL_SMB

P3800_VAL_TTL0

P3800_VAL_TTL1

P3800_VAL_TTL2

P3800_VAL_TTL3

P3800_VAL_TTL4

P3800_VAL_TTL5


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P3800_VAL_TTL6

P3800_VAL_TTL7

**halfway:** Halfway of the trigger path. Possible values of halfway:

P3800_VAL_NONE

P3800_VAL_TTL0

P3800_VAL_TTL1

P3800_VAL_TTL2

P3800_VAL_TTL3

P3800_VAL_TTL4

P3800_VAL_TTL5

P3800_VAL_TTL6

P3800_VAL_TTL7

### @ Return Code

`NoError, ERR_Set_Path`



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   - For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ADLINK is not responsible for any loss of data.
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