PXI-9820

2-CH, 65MS/s, 14-Bit Digitizer with SDRAM

User's Guide



Recycle Paper

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Questions			
Product Model			
Environment	OS: Computer Brand: M/B: CPU: Chipset: BIOS: Video Card: NIC: Other:		
Detail Description			
Suggestions for ADLINK			

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How to Use This Guide

This user's guide is designed to help users understand and operate the PXI-9820. It is divided into three chapters:

Chapter 1 **Introduction**

Gives an overview of product features, applications, specifications and a functional block diagram.

Chapter 2 **Installation**

Describes how to install the PXI-9820.

Chapter 3 **Operation Theory**

Describes how to operate the PXI-9820, including the control and setting of signal, timebase, and trigger sources; trigger modes; data transfers; synchronizing multiple modules; and auto-calibration.

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1

Introduction

The ADLINK PXI-9820 is a 65MS/s, high-resolution PXI digitizer with deep SODIMM SDRAM memory that features flexible input configurations, including programmable input ranges and user-selectable input impedance. With deep onboard acquisition memory, the PXI-9820 is not limited by the PCI's 132MB/s bandwidth, and can record waveforms for extended periods of time. The PXI-9820 is ideal for high-speed waveform capturing such as radar, ultrasound, software radio, and other signal digitizing applications needing large amounts of memory for data storage. PXI-9820 uses the PXI trigger bus to send and receive trigger and timebase signals to and from other devices. In additional, the PXI-9820 can phase-lock the reference clock from the PXI backplane or from an external connector for better synchronization capabilities.

This chapter gives an overview of the PXI-9820 high speed digitizer, and covers the following topics:

- Features
- Applications
- Functional Block Diagram
- Specifications

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1.1 Features

- PXI specifications Rev. 2.1 compliant
- 3U Eurocard form factor, CompactPCI compliant (PICMG 2.0 R3.0)
- 14-bit A/D resolution
- Up to 60MS/s sampling rate per channel with internal timebase
- Up to 65MS/s sampling rate per channel with external timebase
- Up to 130MS/s sampling rate using “ping pong” mode for single-channel acquisition
- 2-CH simultaneous-sampled single-ended analog inputs
- Programmable input ranges of ±1V and ±5V
- User-selectable input impedance of 50Ω or high input impedance
- >30MHz -3dB bandwidth
- Up to 512MB on-board SODIMM SDRAM
- 2-CH synchronous digital inputs
- Scatter-gather DMA data transfers
- Analog and digital triggering
- Fully auto calibration
- Multiple modules synchronization through PXI trigger bus
- On-board phase-lock loop circuit

1.2 Applications

- Software Radio / Wireless Communication
- Radar / Sonar / Lidar
- Ultrasound
- Imaging
- Military / Laboratory / Research

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1.3 Functional Block Diagram

The following topics overview the PXI-9820 main features as shown in the functional block diagram below.

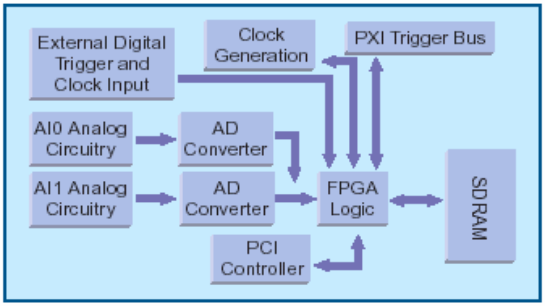


Figure 1.1 PXI-9820 Functional Block Diagram

1.3.1 Analog Input

The PXI-9820 features two analog input channels. Signal bandwidth of each channel exceeds 30MHz, satisfying the Nyquist sampling theory. The input ranges are programmable as either ±5V or ±1V. The 14-bit A/D resolution makes the PXI-9820 ideal both for time-domain and frequency-domain applications.

1.3.2 Acquisition System

The PXI-9820 uses a pair of 65MS/s, 14-bit pipeline ADCs to digitize input signals. It provides an internal 60MHz timebase for data acquisition. The maximum real-time sampling rate is 60MS/s with internal timebase and up to 65MS/s with external timebase. By using the “ping pong” mode, the sampling rate is up to 120MS/s with internal timebase or 130MS/s with external timebase.

1.3.3 Acquisition Memory

The PXI-9820 supports SODIMM SDRAM ranging from 128MB to 512MB. Digitized data is stored in the on-board SDRAM before being transferred to host memory. The PXI-9820 uses scatter-gather bus mastering DMA to move data to the host memory. If the data throughput from the PXI-9820 is less than the available PCI bandwidth, the PXI-9820 will bypass the

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SDRAM and use the on-board 3k-sample FIFO to achieve real-time transfer directly to the host memory.

1.3.4 Triggering

The PXI-9820 features flexible triggering functions, such as analog and digital triggering. The analog trigger features programmable trigger thresholds on rising or falling edges of both input channels. The 5V/TTL digital trigger comes from the external SMB connector, PXI trigger bus or PXI_STAR for synchronizing multiple devices.

Post-trigger, pre-trigger, delay-trigger and middle-trigger modes are available to acquire data around the trigger event. The PXI-9820 also features repeated trigger acquisition to acquire data in multiple segments coming with successive trigger events at extremely short rearming intervals.

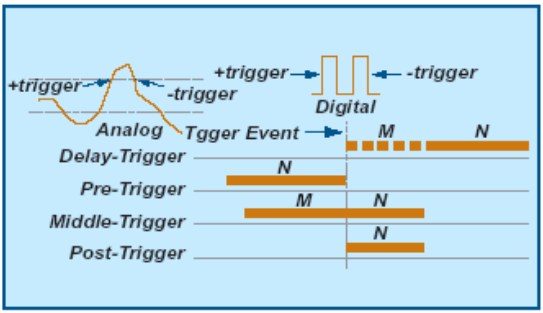


Figure 1.2 PXI-9820 Trigger Modes

1.3.5 Multiple-Instrument Synchronization

To achieve multiple-instrument synchronization, PXI-9820 routes timing and trigger signals between one or more PXI-9820 devices by the PXI trigger bus. Users can assign timebase or trigger signals to a specific PXI trigger bus[0:7] via software, providing better flexibility for multiple devices synchronization. The PXI-9820 also adopts PXI_STAR signal for better synchronization performance. Both trigger signals and timebase clock can be transferred to 13 peripheral slots through the PXI_STAR signal on slot 2.

The reference clock is used in the PXI-9820 phase-lock loop (PLL) circuit to synchronize the timebase clock to the reference. The PXI-9820 can

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accept a reference clock the CLK IN on the front panel as well as from PXI_CLK10. The reference clock should be a fixed and stable 10MHz clock.

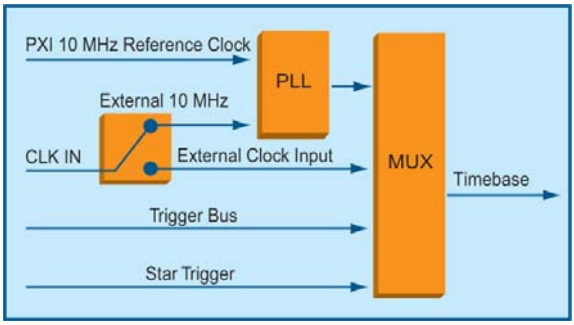


Figure 1.3 PXI-9820 Timebase Control

1.3.6 Synchronous Digital Input

The PXI-9820 features two high-speed digital input lines. User can clock in digital data synchronous to the analog input timebase clock. Viewing analog and digital correlated operations is effortless.

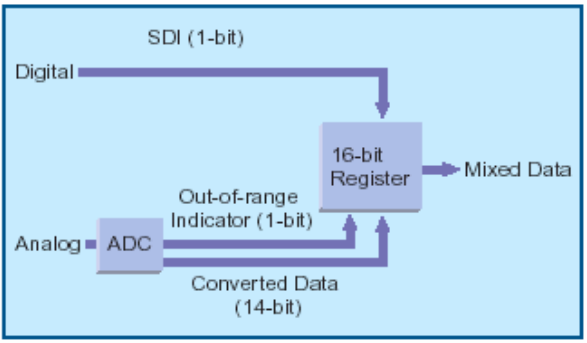


Figure 1.4 PXI-9820 Synchronous Digital Inputs

1.3.7 Auto Calibration

The auto-calibration function of the PXI-9820 is performed with trim DACs to calibrate offset and gain errors of the analog input channels. Once the

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calibration process is complete, the calibration constant will be stored in EEPROM. These values are loaded and used as needed by the board. Because all the calibration is conducted automatically by software commands, users do not have to adjust trimpots to calibrate the boards.

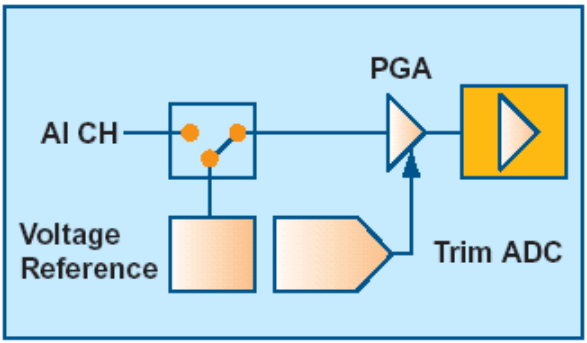


Figure 1.5 PXI-9820 Auto Calibration

1.4 Specifications

Analog Input

- **Number of channels:** 2 simultaneous-sampled single-ended
- **Resolution:** 14 bits
- **Max sampling rate:**
  60MS/s per channel with internal timebase
  65MS/s per channel with external timebase
  120MS/s using “ping pong” mode on CH0 with internal timebase
  130MS/s using “ping pong” mode on CH0 with external timebase
- **On-board memory size:**
  SODIMM SDRAM: 128MB standard, up to 512MB
  FIFO buffer: 3056 samples
- **Bandwidth (-3 dB):** 30MHz minimum, 42MHz typical
- **Passband flatness (typical, referenced at 250 kHz):**
  ±0.4dB, DC to 15 MHz
  ±1dB, 15 to 25 MHz
- **Input signal ranges:**
  ±5V, ±1V (software programmable)
- **Input coupling:** DC
- **Overvoltage protection:**

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Range	Overvoltage protection
±5V	±14V
±1V	±5V

- **Input impedance:**
  50Ω (default), 1.5MΩ (soldering selectable)
- **System Noise:** (typical)

Range	Noise (LSBrms)
±5V	1.21
±1V	1.68

- **Crosstalk:** < - 80dB, DC to 1MHz
- **Total Harmonic Distortion (THD)*:** -75 dB
- **Signal-to-noise ratio (SNR)*:**

Range	SNR (dB)
±5V	69
±1V	63.5

- **Spurious-free dynamic range (SFDR)*:** 76.9dB

*Measured using 200kHz sine wave input with amplitude of 95% of full scale at 60MS/s

Synchronous Digital Input

- **Number of channels:** 2
- **Compatibility:** 5V/TTL
- **Digital logic levels**
  Input high voltage: 0V to 0.8V
  Input low voltage: 2.0V to 5V
- **Maximum input overload:** -0.5V to +7V
- **Hysteresis voltage:** 0.7V minimum

Timebase System

- **Sources:**
  - **Internal, on-board 60MHz:**
    Internal sample clock frequency: 60 MHz / n, $1 \leqq n \leqq 2^{24}-1$
    Timebase accuracy: ±25 ppm
    Jitter: < 6ps
  - **External, CLK IN sine wave:**
    Connector: front panel SMB connector (CLK IN)
    Impedance: 50Ω
    Coupling: AC
    Input amplitude: $1V_{pp}$ to $2V_{pp}$
    Overvoltage protection: $2.5V_{pp}$

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Frequency range:
Ping-pong mode: 25MHz - 65MHz
Others: 500kHz - 65MHz

- External, PXI Trigger Bus[0:7]:
Source selection: from one of PXI Trigger bus[0:7], software selectable
Compatibility: 5V/TTL
Maximum input overload: -0.5V to +5.5V
Frequency range:
Ping-pong mode: 25MHz - 65MHz
Others: 500kHz - 65MHz

- External, PXI_STAR
Source selection: software selectable
Compatibility: 5V/TTL
Maximum input overload: -0.5V to +7.0V
Frequency range:
Ping-pong mode: 25MHz - 65MHz
Others: 500kHz - 65MHz

- **Timebase clock exporting**
  Destinations: PXI_STAR[0:12], PXI Trigger Bus[0:7]

PLL Reference Clock

- **Sources**: PXI 10MHz reference (backplane, PXI_CLK10), external 10MHz reference (front panel SMB, CLK IN)

- **Frequency requirement:** 10MHz ± 50ppm
  - **External 10MHz reference**
    Connector: front panel SMB connector (CLK IN)
    Impedance: 50Ω
    Coupling: AC
    Input amplitude: $1V_{pp}$ to $2V_{pp}$
    Overvoltage protection: $2.5V_{pp}$

  - **PXI 10MHz**
    Connector: from PXI backplane
    Compatibility: 5V/TTL
    Maximum input overload: -0.5V to +5.5V

Triggering

- **Sources:** software, analog trigger, external digital trigger (TRG IO), PXI_STAR, PXI Trigger Bus[0:7]
  - Analog triggering
  Sources: CH0 and CH1

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Slope: rising/falling
Coupling: DC
Trigger sensitivity: 256 steps in full-scale voltage range
Hysteresis: 1.5% of the full range
Offset error: 1.25% of the full range

- Digital triggering

Connectors: front panel SMB connector (TRG IO)
Slope: rising/falling
Compatibility: 5V/TTL
Minimum pulse width: 10ns

- PXI_STAR

Slope: rising/falling
Compatibility: 5V/TTL
Minimum pulse width: 10ns

- PXI Trigger Bus[0:7]

Source: software selectable from one of PXI trigger bus[0:7]
Compatibility: 5V/TTL
Minimum pulse width: 10ns

- **Modes:** pre-trigger, middle-trigger, post-trigger, delay-trigger
- **Repeated trigger rearming interval:** 2 cycles of timebase
- **Pre-trigger depth:** 128MB to 512MB, depending on memory size
- **Post-trigger depth:** 128MB to 512MB, depending on memory size
- **Trigger Exporting**

  Destinations: Front panel SMB connector (TRG IO), PXI Star Trigger[0:12], PXI Trigger Bus[0:7]

Calibration

- **Recommended warm-up time:** 15 minutes
- **On-board calibration reference:**

  Level: 5.000V
  Temperature coefficient: ±2ppm/°C
  Long-term stability: 6ppm/1000Hr

General Specifications

- **Dimensions:** (not including connectors)

  Single 3U PXI module, 100mm by 160mm
- **I/O connector:**

  BNC x 2 for analog inputs(CH0 & CH1)
  SMB x 4 for external timebase (CLK IN), external digital trigger (TRG IO) and synchronous digital input 0 & 1(SDI0, SDI1)
- **PCI signaling environment:**

  Supports a 32-bit 3.3V or 5V PCI bus

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- **Operating environment:**
  Ambient temperature: 0 to 50°C
  Relative humidity: 5% to 95% non-condensing
- **Storage environment :**
  Ambient temperature: -20 to 80°C
  Relative humidity: 5% to 95% non-condensing
- **Power requirement:** (typical)

Power Rail	Current (mA)
5V	900
12V	305
3.3V	360 (with 128MB onboard SDRAM memory) 500 (with 512MB onboard SDRAM memory)

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2

Installation

This chapter describes how to install the PXI-9820. Please read the contents of the package and unpacking information carefully before you install the module.

2.1 Contents of Package

Check the shipping carton for any visible damage. If the shipping carton and contents are damaged, notify the dealer for a replacement. Retain the shipping carton and packing materials for inspection by the dealer. Remember to obtain authorization before returning any products to ADLINK.

Check the following in the package. If there is any missing item, contact your dealer:

- PXI-9820 2CH, 65MS/s, 14-Bit Digitizer with SDRAM
- This User's Guide
- Software Installation Guide
- ADLINK All-In-One CD

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2.2 Unpacking

Your PXI-9820 module contains electro-static sensitive components that can be easily be damaged by static electricity.

Therefore, the module should be handled on a grounded anti-static mat. The operator should be wearing an anti-static wristband, grounded at the same point as the anti-static mat.

After opening the shipping carton, extract the module and place it only on a grounded anti-static surface with component side up.

Again, inspect the module for damage. Press down on all the socketed IC's to make sure that they are properly seated. Do this only with the module place on a firm flat surface.

Note: DO NOT APPLY POWER TO THE MODULE IF IT HAS BEEN DAMAGED.

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2.3 Mechanical Drawing

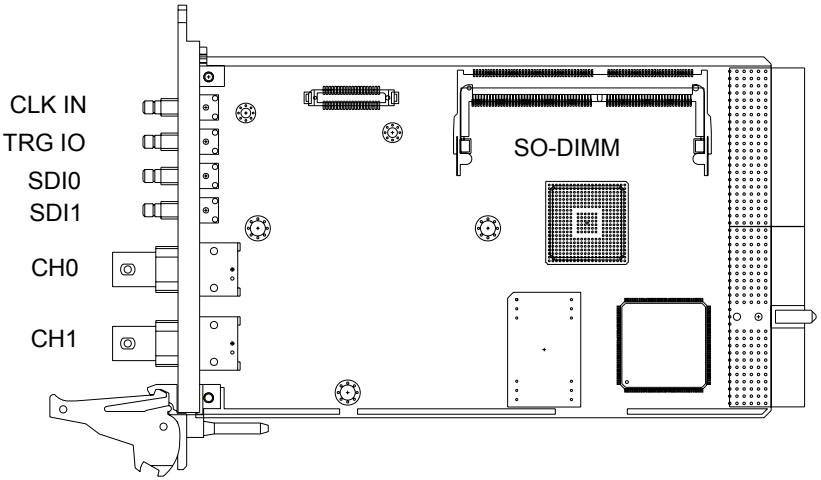


Figure 2.1 PXI-9820 Mechanical Drawing

The ADLINK PXI-9820 module is packaged in a Eurocard form factor compliant with PXI Specifications measuring 160mm in length and 100mm in height (not including connectors). The connector types and functions are described as follows.

CLK IN: The SMB connector is a 50Ω, AC-coupled external timebase input or external 10MHz reference clock input.

TRG IO: The SMB connector is for external digital trigger input or output.

SDI0: The SMB connector is for synchronous digital input channel 0.

SDI1: The SMB connector is for synchronous digital input channel 1.

CH0: The BNC connector is for attaching the analog input signal to measure on channel 0.

CH1: The BNC connector is for attaching the analog input signal to measure on channel1.

SO-DIMM: The SO-DIMM connector is for plugging the 144-pin SDRAM SODIMM.

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2.4 Analog Input Impedance Setting

CH0 and CH1 input impedance can be set to 50Ω or 1.5MΩ by soldering gap switches J6 and J7 on the backside of the PXI-9820. The location of J6, J7 and the corresponded input impedance setting are shown in Fig. 2.2 and Table 2.1. The default setting is 50Ω input impedance.

J6	CH0 Input Impedance
Open	High (1.5MΩ)
Close (Default)	Low (50Ω)

J7	CH1 Input Impedance
Open	High (1.5MΩ)
Close (Default)	Low (50Ω)

Table 2.1: Location of solder switches

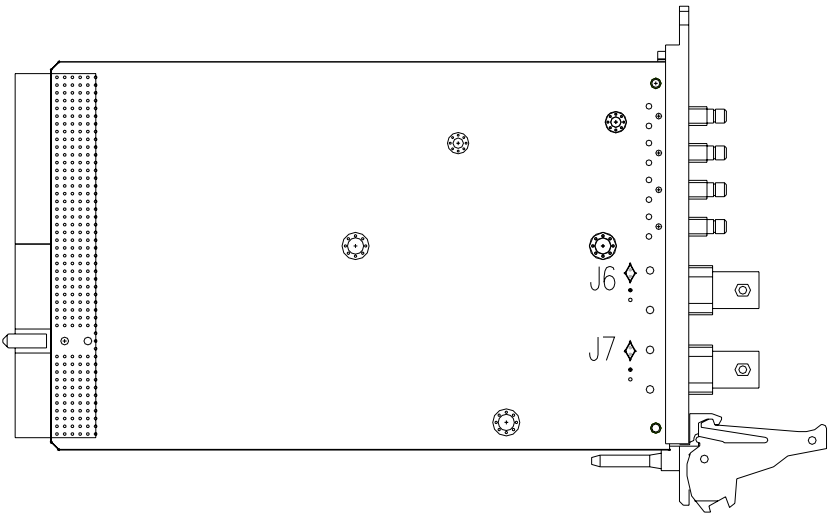


Figure 2.2: Location of solder switches

NOTE:

If the high input impedance 1.5MΩ is selected, the output impedance of the signal sources should be kept low to avoid of the offset voltage caused by the input bias current, which is 2μA min. and 25μA max.

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2.5 Installation

Windows will find the new PXI-9820 module automatically. If this is the first time the PXI-9820 is running on your Windows system, please refer to the following step-by-step installation procedures.

2.5.1 Software Installation

For Windows 98/2000/XP users:

1. Insert the ADLINK ALL-In-One CD. Under `X:\Software\WD-DASK\W98nt2k\DISK1`, you will find `SETUP.EXE` (`X` is the drive letter of your CDROM).
2. Execute `SETUP.EXE` and follow the installation shield to complete WD-DASK installation.
3. When you complete the software installation, turn off your system and follow the hardware installation guide to insert PXI-9820 into your system.

2.5.2 Hardware Installation/Removal Procedures

The PXI connectors are rigid and require careful handling when inserted and removed. Improper handling of modules can easily damage the backplane. To insert the ADLINK PXI-9820 module into a PXI chassis, please follow the procedures below.

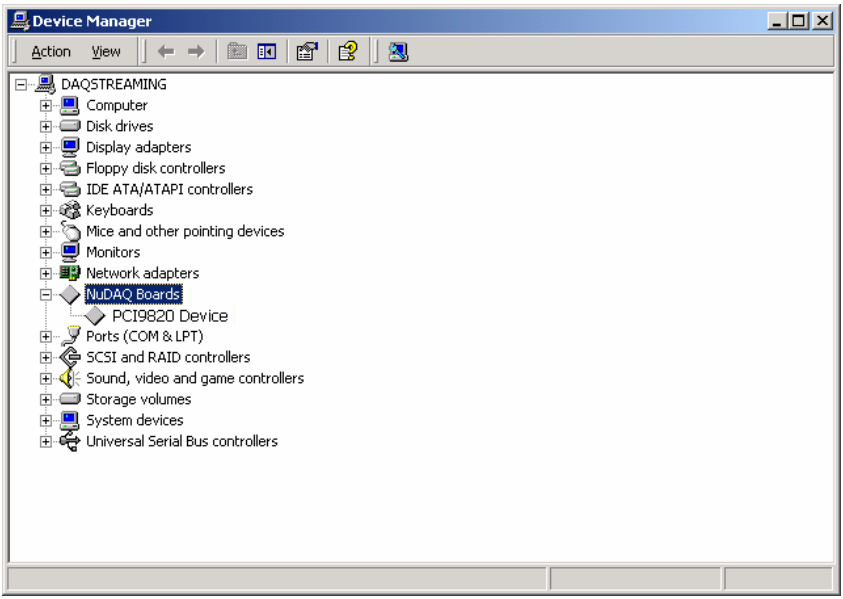
1. Turn off your system
2. Align the module's edge with the card guide in the PXI chassis.
3. Slide the module into the chassis, until resistance is felt from the PXI connector.
4. Push the ejector upwards and fully insert the module into the chassis
5. Once inserted, a "click" can be heard from the ejector latch.
6. Tighten the screw on the front panel.
7. Power on

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To remove the module, reverse steps 2 through 6 above.

2.5.3 Installation check

When you complete both software and hardware installations, you can check the list in device manager to confirm whether PXI-9820 is working properly. In the device manager, look for a device named “PCI9820 Device” under Nu-DAQ Boards. If it is found, installation was successful.



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2.6 Software Support

ADLINK provides versatile software drivers and packages for users' differing approaches to building up a system. ADLINK not only provides programming libraries such as DLLs for most Windows based systems, but also drivers for other software packages such as LabVIEW®.

All software options are included in the ADLINK All-In-One CD. Non-free software drivers are protected with licensing codes. Without the software code, you can install and run the evaluation version for two hours for trial/demonstration purposes. Please contact ADLINK dealers to purchase the formal license.

2.6.1 Programming Library

For customers who are writing their own programs, we provide function libraries for many different operating systems, including:

WD-DASK: Includes device drivers and DLLs for **Windows 98**, **Windows NT**, and **Windows 2000**. DLL is a binary compatible across Windows 98, Windows NT, and Windows 2000. All applications developed with WD-DASK are compatible across Windows 98, Windows NT, and Windows 2000. The developing environment can be VB, VC++, Delphi, BC5, or any Windows programming language that allows calls to a DLL. The function reference manual of WD-DASK are in the All-In-One CD (`\Manual_PDF\Software\WD-DASK`).

WD-DASK/X: Includes device drivers and shared libraries for Linux. The developing environment can be Gnu C/C++ or any programming language that allows linking to a shared library. The function reference manual of WD-DASK/X are in the All-In-One CD (`\Manual_PDF\Software\WD-DASK`).

2.6.2 DAQ-LVIEW PnP: LabVIEW® Driver

DAQ-LVIEW PnP contains the VIs, which are used to interface with National Instrument's LabVIEW® software package. DAQ-LVIEW PnP supports Windows 98/NT/2000. The LabVIEW® driver is shipped free with the device. Users can install and use them without a license. For detailed information about DAQ-LVIEW PnP, please refer to the user's guide and function reference manual in the All-In-One CD (`\Manual_PDF\Software\DAQ-LVIEW PnP`).

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2.6.3 WD-OCX: ActiveX Controls

We suggest customers who are familiar with ActiveX controls and VB/VC++ programming use WD-OCX ActiveX control component libraries for developing applications. WD-OCX is designed for Windows 98/NT/2000. For more detailed information about WD-OCX, please refer to the function reference manual in the All-In-One CD (`\Manual_PDF\Software\WD-OCX`)

In addition, ADLINK supplies ActiveX control software *DAQBench*.

DAQBench is a collection of ActiveX controls for measurement or automation applications. With *DAQBench*, users can easily develop custom interfaces to display data, analyze acquired data or data received from other sources, or integrate with popular applications or other data sources. For more detailed information about *DAQBench*, please refer to the All-In-One CD (`\Manual_PDF\Software\DAQBench`)

Users can obtain a 4-hour evaluation version of *DAQBench* for free from the All-In-One CD. Please contact ADLINK or an ADLINK dealer to purchase the software license.

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3

Operation Theory

The operation theory of the PXI-9820 is described in this chapter, including the control and setting of signal sources, timebase sources, trigger sources, trigger modes, data transfers, synchronizing multiple modules, and auto-calibration.

3.1 Block Diagram

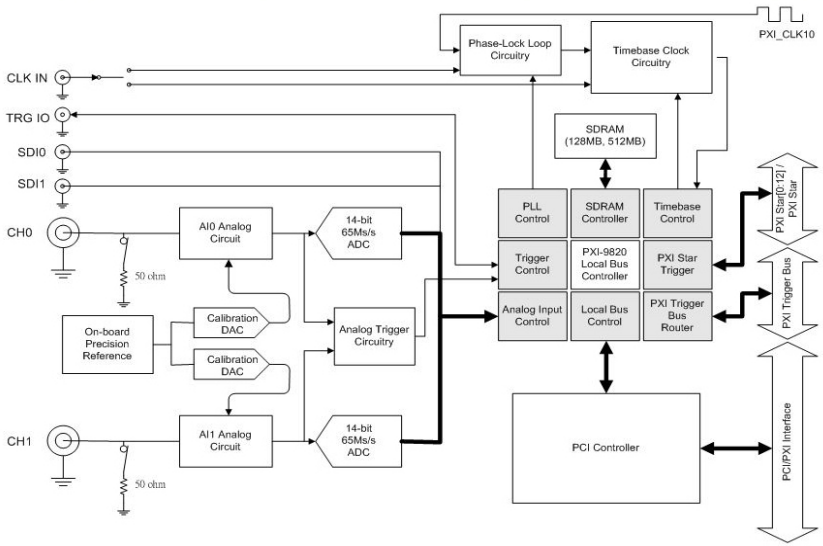


Figure 3.1 PXI-9820 Block Diagram

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3.2 Analog Input Signal Source Control

Number of Channels

The PXI-9820 provides two simultaneously sampled analog input channels in SE (single ended) connection. Each channel can be enabled individually.

Signal Range and Input impedance

The available signal input ranges are ±5V or ±1V, which can be set by software. All signals are DC-coupled. The input impedance for high-speed applications should also be considered. The selectable input impedance values are 50Ω and 1.5MΩ. Please refer to section 2.4 for setting impedance.

3.3 A/D Sampling rate and Timebase Control

The PXI-9820 supports six timebase sources for analog input conversion:

- Internal 60MHz (Internal VCXO free run mode)
- Internal 60MHz (timebase clock locked to PXI_CLK10)
- Internal 60MHz (timebase clock locked to external reference 10MHz)
- External sine wave
- PXI Trigger Bus[0:7]
- PXI_STAR

The following diagram shows the timebase clock architecture of the PXI-9820.

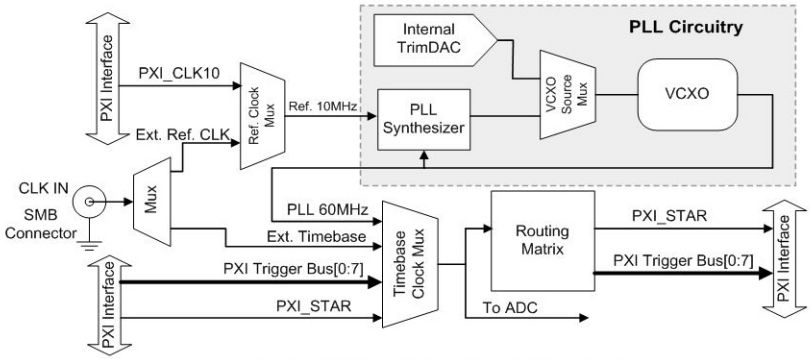


Figure 3.2 PXI-9820 Timebase Clock Architecture

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Once choosing the timebase source, users can set a 24-bit counter to divide the timebase to get the needed sampling rate. The following formula determines the ADC sampling frequency:

Sampling Rate = Timebase Frequency / ADC Clock Divisor

where the ADC Clock Divisor = 1,2,3,4,5… 2^{24}-1(maximum)

3.3.1 Internal Timebase Clock Source

The PXI-9820 has an onboard Voltage Control Crystal Oscillator (VCXO) running at 60MHz. When selects internal timebase clock, you can have free-run mode (none phase-locked) or PLL mode. In free-run mode, the 60MHz timebase clock is coming from the VCXO which is controlled by an internal trim DAC. In PLL mode, the onboard 60MHz timebase phase locked to the reference 10MHz clock. The reference 10MHz clock comes from PXI backplane (PXI_CLK10) or front panel SMB connector (CLK IN).

3.3.2 External Timebase Clock Source

When users need a specific timebase in some applications that the onboard 60MHz timebase is not achievable, a timebase clock from an external device can replace onboard timebase clock. In addition, external timebases also provides a method to synchronize PXI-9820 to other measurement modules by distributing/receiving a common clock to/from multiple modules. The PXI-9820 can receive an external timebase clock from the front panel connector (CLK IN), PXI Star trigger or one of the PXI Trigger bus line.

Users can supply the timebase from external SMB connector **CLK IN**, which should be a sine wave signal. This signal is AC coupled with 50Ω input impedance and the valid input level is from 1 to 2 volts peak-to -peak. Note that the external clock must be continuous for correct ADC operation because of the pipeline architecture of the ADC.

PXI-9820 can receive the timebase clock via one of the trigger bus lines by software selection. The eight PXI trigger bus lines (PXI_TRIG[0:7]) provide intermodule synchronization and communication. Note that this function is only available when the PXI-9820 is in a PXI system. It's not supported when PXI-9820 is in a CompactPCI system.

When PXI-9820 is plugged into a generic peripheral slot, it can receive timebase clock from PXI_STAR. The PXI_STAR signal comes from star trigger controller are matched in propagation delay within 1ns and the delay from star trigger slot to a peripheral slot is less than 5ns. According to these hardware features, PXI-9820 can achieve very good synchronization performance when using PXI_STAR as timebase clock source. Note that this

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function is only available when the PXI-9820 is in a PXI system. It's not supported when PXI-9820 is in a CompactPCI system.

3.3.3 PLL Reference Clock Source

The PXI-9820 equipped with a phase-locked loop circuit to synchronize the timebase clock to reference clock. The PXI-9820 can receive a reference clock from the front panel connector (CLK IN) as well as from PXI_CLK10. The reference clock from front panel connector should be a stable 10MHz clock. The input of CLK IN is AC coupled with 50Ω input impedance and the valid input level is from 1 to 2 volts peak-to -peak. Note that the reference clock must be continuous for correct PLL operation. Once the reference clock disconnected, the timebase clock will still exist but not phase lock to reference clock anymore. When using external timebase clock, it's not valid to lock to reference clock.

3.3.4 Timebase Clock Exporting

The PXI-9820 can export timebase clock to the following two destinations: PXI_STAR or one of PXI Trigger bus lines. When PXI-9820 plugged into star trigger controller slot of the PXI backplane, it can export timebase clock to the other 13 generic peripheral slots. The PXI-9820 can also export timebase clock onto one of the eight PXI trigger bus lines. By software programming, user can pick up a trigger line to transmit timebase clock. These two features are very useful when synchronize to multiple measurement modules.

3.3.5 Timebase 50% duty cycle restore function

Because the on-board sample-and-hold circuit is in hold mode when the timebase is high and in track mode when timebase is low, the PXI-9820 can get the best dynamic response performance for high-frequency analog inputs when the timebase has a 50% duty cycle. However, it is often difficult to maintain a 50% duty cycle; especially when driving the timebase with a single-ended or sinewave input. To ease the constraint of providing an accurate 50% timebase, the PXI-9820 has an optional duty cycle restore function to restore the timebase duty cycle to 50%, independent of the clock input duty cycle. Low jitter on the rising edge (sampling edge) of the timebase is preserved while the falling edge is interpolated.

It may be desirable to disable the duty cycle restore function when users use the external timebase input whose frequency is varied. Once the timebase frequency is changed, over 100 clock cycles may be required for the duty cycle restore circuit to settle to the new speed. Duty cycle restore function is software programmable when configuring your PXI-9820.

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3.3.6 130MS/s Sampling using Ping-Pong Mode

The PXI-9820 uses two A/D converters, each running at 60MS/s, to provide a dual-channel simultaneous real-time sampling rate of 60MS/s. (65MS/s with external timebase)

For the single-channel acquisition, the two ADCs can be clocked in a "ping-pong" mode to achieve up to 120MS/s sampling (130MS/s with external timebase). Figure 3.3 illustrates the operation. Note that only CH0 can be applied to ping-pong mode. The onboard auto-calibration circuitry allows the two channels to be matched in order to reduce the image signal.

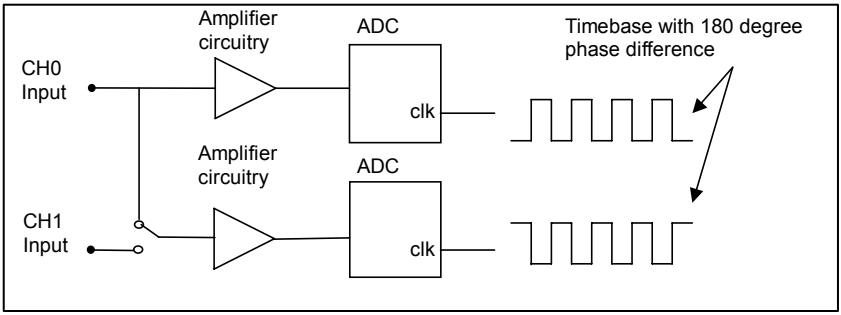


Figure 3.3 "Ping-pong" mode operations

3.3.7 Synchronous Digital Input

The PXI-9820 contains two synchronous digital input channels, SDI0 and SDI1. These two digital input lines can be sampled synchronously with timebase clock for mixed signal applications. Thus the data transfer can up to 60Mbit/s when using internal 60MHz timebase clock. These two digital input lines are combined with analog input channels, respectively. Please refer to Figure 3.4 for the data format of ADC and SDI. When the analog input channel of PXI-9820 is configured as "ping-pong" mode, only SDI0 is enabled.

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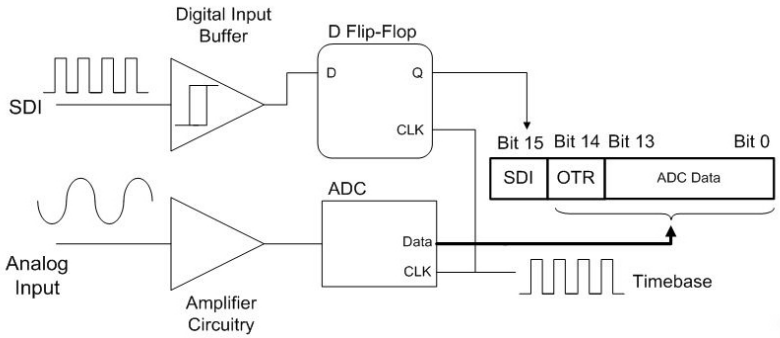


Figure 3.4 Synchronous digital input operations

3.4 Trigger Sources

In addition to the internal software trigger, the PXI-9820 also supports external analog triggers, external digital triggers, PXI_STAR triggers and PXI Trigger Bus[0:7]. Users can configure the trigger source by software. Refer to Figure 3.5 for PXI-9820 trigger architecture.

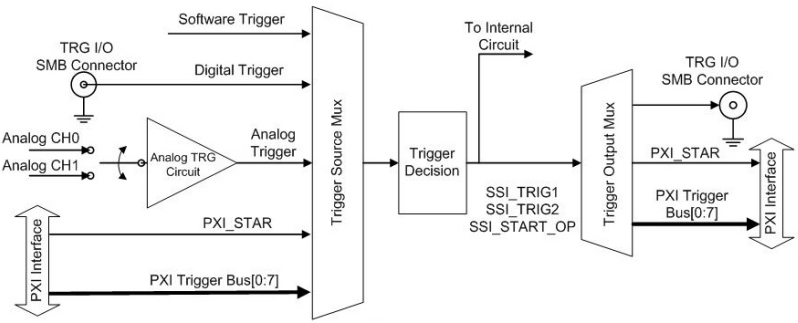


Figure 3.5 PXI-9820 Trigger Architecture

3.4.1 Software Trigger

This trigger mode does not need any external trigger source. The trigger asserts right after executing specified function calls to begin the operation.

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3.4.2 External Analog Trigger

Users can choose either CH0 or CH1 as the trigger signal while using external analog trigger source. The trigger level can be set by software with 8-bit resolution. Please refer to Table 3.1 for the ideal transfer characteristic.

Trigger Level digital setting	Trigger voltage (±5V range)	Trigger voltage (±1V range)
0xFF	4.96V	0.992V
0xFE	4.92V	0.984V
---	---	---
0x81	0.04V	0.008V
0x80	0	0
0x7F	-0.04V	-0.008V
---	---	---
0x01	-4.96V	-0.992V

Table 3.1 Analog trigger ideal transfer characteristic

The trigger conditions for analog triggers are illustrated in Figure 3.6 and described as follows:

- **Positive-slope trigger** - The trigger event occurs when the trigger signal (analog input signal) changes from a voltage that is lower than the specified trigger level to a voltage that is higher than the specified trigger level.

- **Negative-slope trigger** - The trigger event occurs when the trigger signal (analog input signal) changes from a voltage that is higher then the specified trigger level to a voltage that is lower than the specified trigger level.

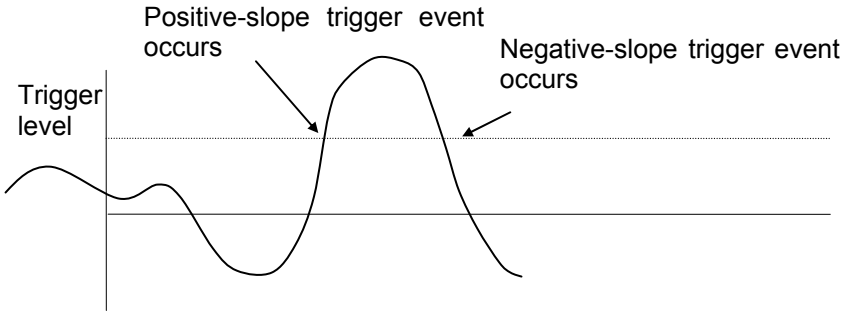


Figure 3.6 Analog trigger conditions

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3.4.3 External Digital Trigger

An external digital trigger occurs when a TTL rising edge or a falling edge is detected at the SMB connector **TRG IO** on the front panel, as illustrated in Figure 3.7. The trigger polarity can be selected by software. Note that the signal level of the external digital trigger signal should be TTL-compatible, and the minimum pulse width is 10ns.

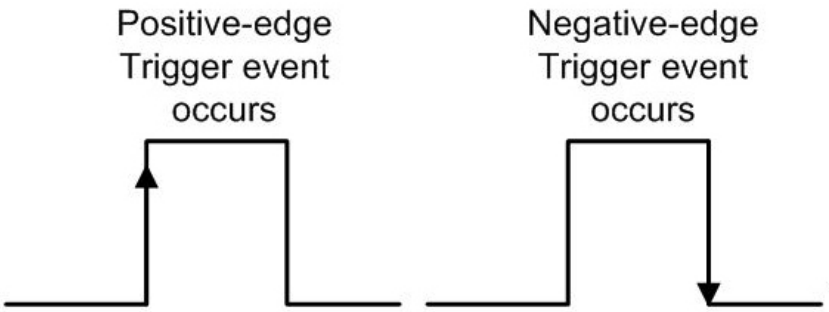


Figure 3.7 External digital trigger input

3.4.4 PXI_STAR Trigger

When users select PXI_STAR as trigger source, the PXI-9820 can accept a TTL-compatible digital signal as a trigger signal. The trigger occurs when a rising edge or falling edge is detected at PXI_STAR. User can use software to configure the trigger polarity. The minimum pulse width requirement of this digital trigger signal is 10ns.

3.4.5 Triggers from PXI Trigger Bus[0:7]

The PXI-9820 utilizes PXI Trigger Bus[0:7] as System Synchronization Interface (SSI). Using the interconnected bus provided by PXI Trigger Bus, user can easily synchronize multiple modules. When configured as input, the PXI-9820 can accept three different SSI signals, SSI_TRIG1, SSI_TRIG2 and SSI_START_OP (for more detail about these signals, please refer to section 3.9). Each signal can be routed from one of the PXI Trigger Bus[0:7] by software programming.

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3.5 Trigger Modes

The PXI-9820 provides 5 trigger sources (internal software trigger, external analog trigger, external digital trigger, PXI_Star trigger, and PXI Trigger Bus[0:7] signals). Users must select one of them as the source of the trigger event. A trigger event occurs when the specified condition is detected on the selected trigger source (For example, a rising edge on the external digital trigger input).

There are 4 trigger modes (pre-trigger, post-trigger, middle-trigger, and delay-trigger) working with the 5 trigger sources to initiate different data acquisition timing when a trigger event occurs. They are described as follows.

3.5.1 Post-trigger Acquisition

Use post-trigger acquisition when you want to collect data after the trigger event, as illustrated in Figure 3.8.

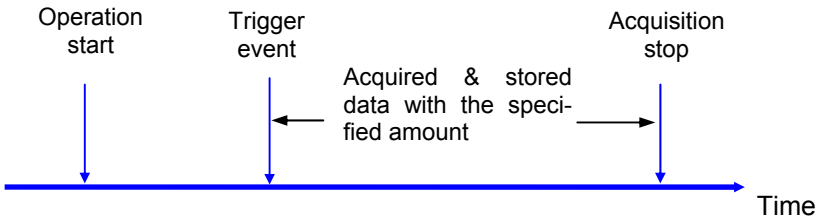


Figure 3.8 Post trigger

3.5.2 Pre-trigger Acquisition

Use pre-trigger acquisition to collect data before the trigger event. The acquisition starts once specified function calls are executed to begin the pre-trigger operation, and it stops when the trigger event occurs.

If the trigger event occurs after the specified amount of data has been acquired, the system only stores the data before the trigger event with the specified amount, as illustrated in Figure 3.9.

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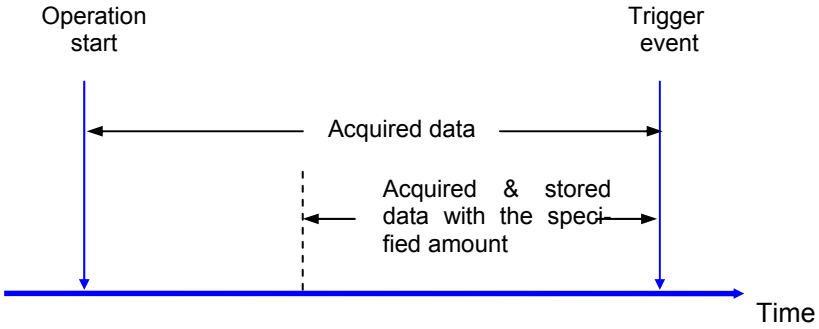


Figure 3.9 Pre trigger (the trigger event occurs after the specified amount of data has been acquired)

However, if the trigger event occurs before the specified amount of data has been acquired, the system can either stop the acquisition immediately (which implies the stored data will be less then the amount you specified) or ignore the trigger signal until the specified amount of data has been acquired (which assures the user can get the specified amount of data). These can be set by software and are illustrated in Figure 3.10 and Figure 3.11.

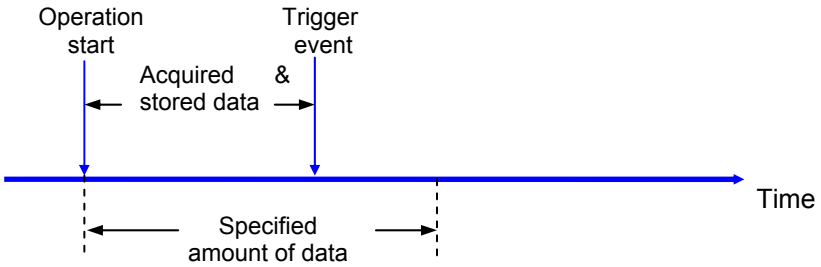


Figure 3.10 Pre trigger (The trigger signal is accepted anytime after the operation starts)

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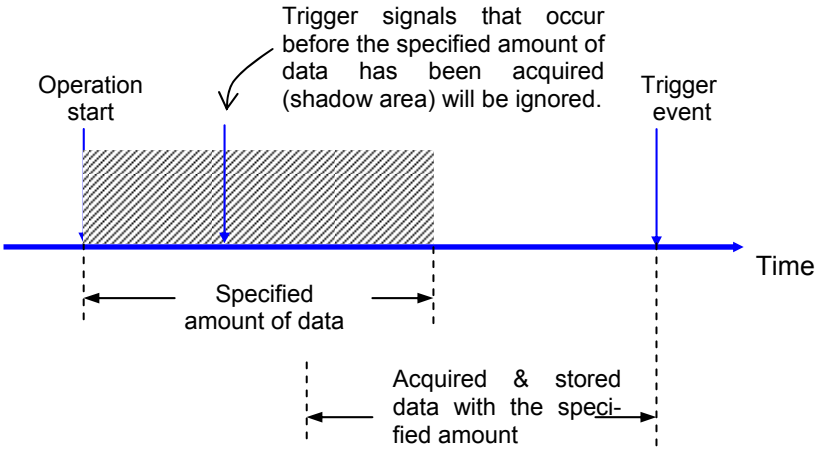


Figure 3.11 Pre trigger (The trigger signal will be ignored until the specified amount of data is acquired)

3.5.3 Middle-trigger Acquisition

Use middle-trigger acquisition when you want to collect data before and after the trigger event. The amount of stored data before and after the trigger can be set individually (M and N), as illustrated in Figure 3.12.

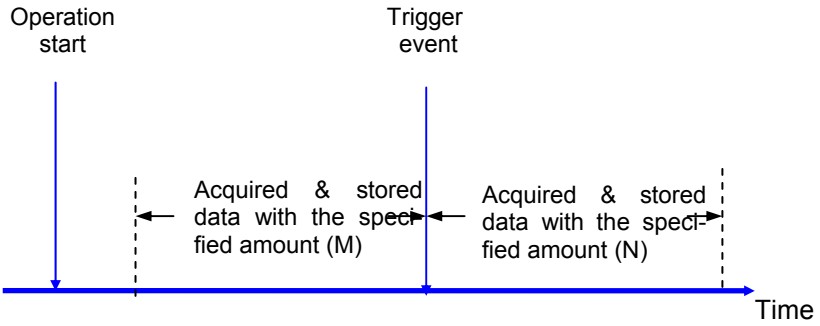


Figure 3.12 Middle trigger

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Like pre-trigger mode, the stored data may be less than the amount specified if the trigger event occurs before the specified amount of data (M) has been acquired. Users can also set by program to ignore trigger signals until the specified amount of data (M) has been acquired.

3.5.4 Delay-trigger Acquisition

Use delay trigger acquisition to delay the data collection after the trigger event, as illustrated in Figure 3.13. The delay time is specified by a 32-bit counter value so that the maximum delay time is the period of timebase * (2^{32} –1), while the minimum delay time is the period of timebase.

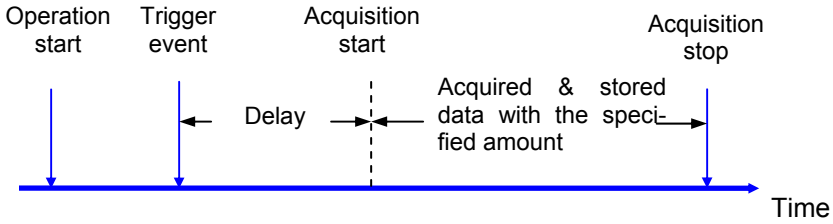


Figure 3.13 Delay trigger

3.5.5 Post-trigger or Delay-trigger Acquisition with Re-trigger

Use post-trigger or delay-trigger acquisition with re-trigger function to collect data after several trigger events, as illustrated in Figure 3.14. Users can program the number of triggers then the PXI-9820 will acquire an additional record each time a trigger is accepted until all the requested records have been stored in memory. After the initial setup, the process does not require software intervention.

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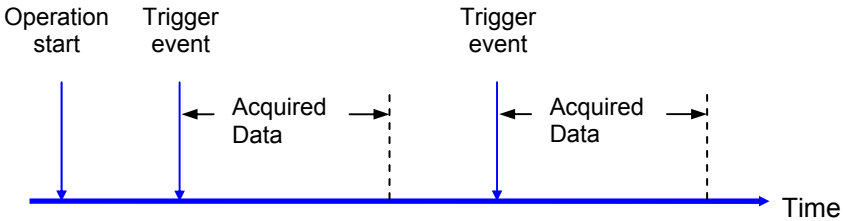


Figure 3.14 Post-trigger with re-trigger

3.6 Trigger Signals Exporting

The PXI-9820 can export trigger signals to the following connectors: TRG IO, PXI_STAR or PXI Trigger Bus[0:7].

The **TRG IO** on the front panel can also be programmed to output the trigger signal when the trigger source is from software trigger, analog trigger, PXI_STAR trigger, or PXI Trigger Bus[0:7]. The timing characteristic is in Figure 3.15.

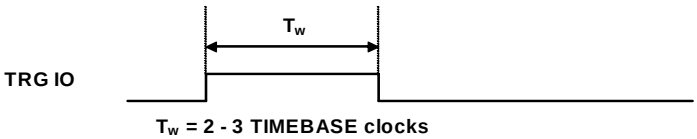


Figure 3.15 TRG IO output signal timing

When the PXI-9820 is plugged into the star trigger controller slot, i.e. slot 2, in a PXI system, it can export trigger signals to other 13 generic peripheral slots (PXI_STAR0 ~ PXI_STAR12) through the PXI star trigger pin. The trigger signal source can be from software trigger, external digital trigger signal from TRG IO, analog trigger and PXI Trigger Bus[0:7]. The output trigger signal timing characteristic is identical to the TRG IO which is shown in figure 3.15.

The PXI-9820 utilize PXI Trigger Bus[0:7] as System Synchronize Interface. When configured as output, the PXI-9820 can output 3 different trigger signals, SSI_TRIG1, SSI_TRIG2 and SSI_START_OP. User can route these signals to any one of PXI Trigger Bus[0:7] by software programming.

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3.7 Data Transfers

Since the maximum data throughput on the PXI-9820 (60MS/s * 2 channels * 2 Bytes/channel = 240MB/s) is much higher than the 32bit/33MHz PCI-bus bandwidth, samples are acquired into the onboard SDRAM memory before being transferred to the host computer. Since the number of stored samples per acquisition is limited by the amount of on-board memory, the PXI-9820 supports different sizes of SODIMM SDRAM ranging from 128MB to 512MB in order to meet application requirements.

Once all the data has been stored in the on-board memory, the data will be transferred to the host computer's memory through bus-mastering DMA.

In a multi-user or multi-tasking OS, like Microsoft Windows, Linux, and so on, it is difficult to allocate a large continuous memory block to do the DMA transfer. Therefore, the PXI-9820 provides the function of scatter /gather DMA to link the non-continuous memory blocks into a linked list so that users can transfer very large amounts of data without being limited by the fragment of small size memory, as illustrated in Figure 3.16.

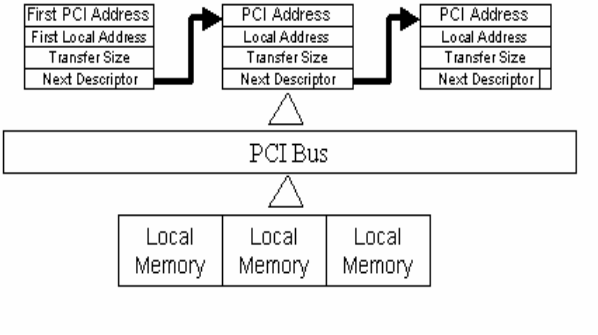


Figure 3.16 Scatter/gather DMA for data transfer

If the data throughput from the PXI-9820 is less than the available PCI bandwidth (For example: 20MS/s * 2 channels * 2 Bytes/channel = 80MB/s), the PXI-9820 also features on-board 3k-sample FIFO to achieve real-time transfer bypassing the SDRAM, directly to host memory.

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3.8 AI Data Format

Table 3.2 illustrates the ideal transfer characteristics of various input ranges of the PXI-9820. Bit13-0 is the acquired 14-bit A/D data with binary coding format while bit14 is the out-of-range (OTR) indicator (logic "1" means out-of-range). As described in section 3.3.7, bit 15 is the synchronous digital input data. SDI0 is within the data format of analog channel 0 while SDI1 is within the data format of analog channel 1.

Description	Analog Input Voltage		Digital code
Full-scale Range	±5V	±1V	
Least significant bit	0.61mV	0.122mV	
> = FSR	>= 5V	>= 1V	7FFF
FSR-1LSB	4.99939V	0.999878V	3FFF
Midscale +1LSB	0.61mV	0.122mV	2001
Midscale	0V	0V	2000
Midscale –1LSB	-0.61mV	-0.122mV	1FFF
-FSR	-5V	-1V	0000
< -FSR	< -5V	< -1V	4000

Table 3.2 Analog input voltage and the output digital code (Note that bit14 is the out-of-range indicator)

3.9 Synchronizing Multiple Devices

The eight interconnected lines on PXI backplane named as PXI Trigger Bus[0:7] provide a flexible interface for multiple modules synchronization. The PXI-9820 utilizes the PXI Trigger Bus[0:7] as the System Synchronization Interface (SSI). By providing flexible routing of timebase clock and trigger signals onto PXI Trigger Bus, the PXI-9820 makes the synchronization between multiple modules easy and simple.

The bi-directional SSI I/Os provide a flexible connection between modules, which allows one SSI master PXI-9820 to output the SSI signals to other slaves PXI-9820s to receive the signals. Table 3.3 lists the summary of SSI timing signals and the functionalities. Figure 3.17shows the architecture of SSI. Note that it's not allowed to route different signals onto the same trigger bus line.

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SSI timing signal	Functionality
SSI_TIMEBASE	Input/Output 60MHz timebase signal through SSI
SSI_TRIG1	Input/Output the trigger signal through SSI
SSI_TRIG2	Input/Output the clocked trigger signal through SSI
SSI_START_OP	Input/Output the acquisition start signal in pre-trigger or middle-trigger mode

Table 3.3 Summary of SSI timing signals and the corresponding function

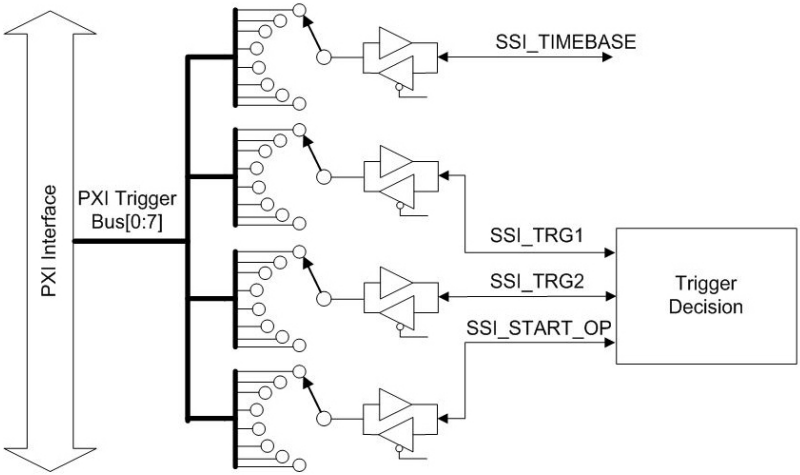


Figure 3.17 SSI Architecture

3.9.1 SSI_TIMEBASE

As an output, the SSI_TIMEBASE signal outputs the onboard 60MHz LVTTL timebase through PXI Trigger Bus.

As an input, the PXI-9820 accepts the SSI_TIMEBASE signal to be the source of timebase.

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3.9.2 SSI_TRIG1

As an output, the SSI_TRIG1 signal reflects the trigger event signal in an acquisition sequence. Users can use the function SSI_SourceConn() to output the SSI_TRIG1 signal.

As an input, the PXI-9820 accepts the SSI_TRIG1 signal to be the trigger event source. The signal is configured in the rising edge-detection mode. When selecting the trigger sources of the PXI-9820, Users can select **TRSRC_SSI_1** to set SSI_TRIG1 as the source of trigger event.

Figure 3.18 and Figure 3.19 show the input and output timing requirements.

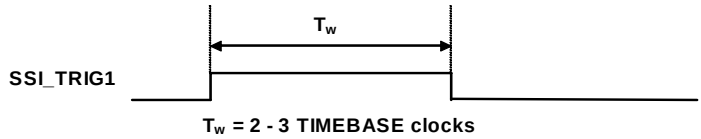


Figure 3.18 SSI_TRIG1 output signal timing

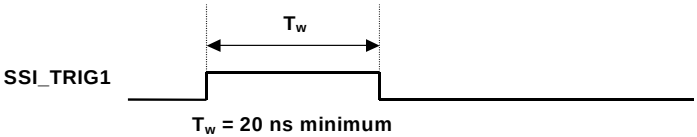


Figure 3.19 SSI_TRIG1 input signal timing

3.9.3 SSI_TRIG2 and SSI_START_OP

As an output, the SSI_TRIG2 signal is a clocked SSI_TRIG1 signal by TIMEBASE, as illustrated in Figure 3.20.

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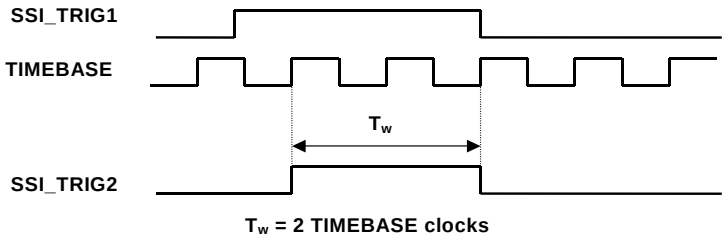


Figure 3.20 SSI_TRIG2 output signal timing

As an input, the PXI-9820 accepts the SSI_TRIG2 signal to be the source of a one-clock delayed trigger event. The controller on the PXI-9820 will then compensate the one-clock delay if using SSI_TRIG2 as the source of trigger event. The signal is configured in the rising edge-detection mode.

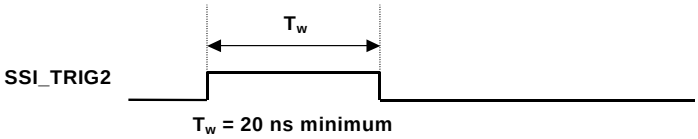


Figure 3.21 SSI_TRIG2 input signal timing

As an output, the SSI_START_OP signal reflects the operation start signal in a pre-trigger or middle-trigger acquisition sequence. Please refer to Figure 3.9 - Figure 3.12 for the relationship between the operation start signal and the acquisition sequence.

As an input, the PXI-9820 accepts the SSI_START_OP signal to be the operation start signal in a pre-trigger or middle-trigger acquisition sequence. The signal is configured in the rising edge-detection mode. Figure 3.22 and Figure 3.23 show the SSI_START_OP signal input and output timing requirements.

For enabling output operations, users can use the function SSI_SourceConn() to output the SSI_TRIG2 and SSI_START_OP signals.

For the input operations, users can select **TRSRC_SSI_2** to set SSI_TRIG2 and SSI_START_OP as the source of the trigger event and operation start signal.

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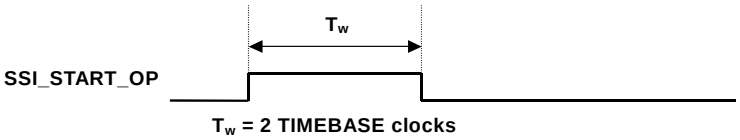


Figure 3.22 SSI_START_OP output signal timing

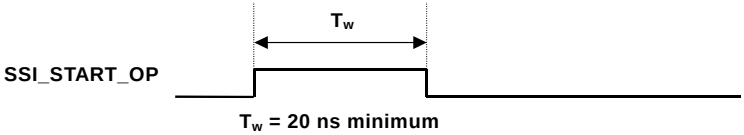


Figure 3.23 SSI_START_OP input signal timing

3.9.4 Comparing the different trigger sources from SSI

When selecting **TRSRC_SSI_1** as the trigger source input, the signal SSI_TRIG1 reflects the trigger event signal in an acquisition sequence. However, when synchronizing multiple PXI-9820 devices, each PXI-9820 may recognize the trigger signal with one-clock time difference because the signal is not related to the timebase.

There is another phenomenon if using **TRSRC_SSI_2** in pre-trigger and middle-trigger mode. The operation start signal is generated by a software command so multiple PXI-9820 devices don't start the data acquisition simultaneously, which may result in the fact that the amount of stored samples are different if the trigger event occurs before the specified amount of data has been acquired.

When selecting **TRSRC_SSI_2** as the trigger source input, SSI_TRIG2 and SSI_START_OP can achieve better synchronization between multiple PXI-9820 devices. A clocked SSI_TRIG2 can guarantee all PXI-9820 devices recognize the trigger event at the same clock edge if they use the same timebase. In pre-trigger and middle-trigger mode, SSI_START_OP guarantees all the PXI-9820 devices start the data acquisition at the same time.

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3.10 Auto-calibration

By using the auto-calibration feature of the PXI-9820, the calibration software can measure and correct offset and gain errors without any external signal connections, reference voltages, or measurement devices.

After the auto-calibration procedure finishes, the calibration constants can be saved into the EEPROM. In addition to the default bank of factory calibration constants, there are three extra user-modifiable banks in the EERPOM for users to store three sets of calibration constants according to different environments and re-load the calibration constants when necessary.

Because of the fact that errors in measurements will vary with time and temperature, it is recommended that users re-calibrate the PXI-9820 when the module is installed in a new environment.

Note: Before auto-calibration procedure starts, please warm up the module for at least 15 minutes.

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   - Peripherals and third-party products not manufactured by ADLINK will be covered by the original manufacturers' warranty.
   - For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ADLINK is not responsible for any loss of data.
   - Please ensure the use of properly licensed software with our systems. ADLINK does not condone the use of pirated software and will not service systems using such software. ADLINK will not be held legally responsible for products shipped with unlicensed software installed by the user.
   - For general repairs, please do not include peripheral accessories. If peripherals need to be included, be certain to specify which items you sent on the RMA Request & Confirmation Form. ADLINK is not responsible for items not listed on the RMA Request & Confirmation Form.

3. Our repair service is not covered by ADLINK's guarantee in the following situations:
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   - Damage caused by carelessness on the user's part during product transportation.
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   - Damage caused by inappropriate storage environments such as with high temperatures, high humidity, or volatile chemicals.
   - Damage caused by leakage of battery fluid during or after change of batteries by customer/user.
   - Damage from improper repair by unauthorized ADLINK technicians.

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4. Customers are responsible for all fees necessary to transport damaged products to ADLINK.

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