# PXIe-3935

PXIe Express Embedded Controller

**User's Manual**



| | |
|---|---|
| **Manual Rev.:** | 2.00 |
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| **Part No:** | 50-17052-1000 |

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# Revision History

| Revision | Release Date | Description of Change(s) |
|---|---|---|
| 2.00 | 2017/3/24 | Initial Release |


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# Preface

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## Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.




Additional information, aids, and tips that help users perform tasks.




Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.




Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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# 1 Introduction

The ADLINK PXIe-3935 PXI Express embedded controller, based on the Intel® Celeron® 2000E 2.2GHz processor, pairs superior performance with an unprecedented price point. Specifically conceived for hybrid PXI Express-based testing systems, the ADLINK PXIe-3935 delivers a rugged and stable platform for a wide variety of testing and measurement applications.

The PXIe-3935 provides ample interface flexibility, including two DisplayPort connectors, allowing connection to two monitors, dual USB 3.0 connections for high speed peripheral devices, dual Gigabit Ethernet ports with one for LAN connection and the other for controlling LXI instruments, four USB 2.0 ports for peripheral devices and USB instrument control, a Micro-D GPIB connector for GPIB instrument connection, and one RS-232/422/485 D-SUB9 connector for hybrid PXI-based testing systems control.

ADLINK's PXIe-3935 significantly reduces maintenance burdens with easily replaceable battery and upgradable storage and SODIMM modules. Backup BIOS also eases recovery in the event of a main BIOS crash.




Memory addressing over 4GB is OS-dependent, such that a 32-bit operating system may be unable to address memory space over 4GB. To fully utilize memory, 64-bit operating systems are required.

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## 1.1 Features

- Ideal balance between performance and price point
- Intel® Celeron® 2000E 2.2GHz processor
- Dual channel DDR3L SODIMM up to 16GB 1600MHz
- 8 GB/s maximum system throughput
- Dual display port support
- 2.5" HDD or SSD support
- SATA 3Gb/s
- AHCI support
- Integrated I/O
  - Dual Gigabit Ethernet ports
  - Two USB3.0 Ports
  - Four USB 2.0 Ports
  - Built-in GPIB (IEEE488) controller
  - Dual DisplayPort connector
  - One COM port (D-sub9 serial)
  - Trigger I/O for advanced PXITM trigger functions
- Dual BIOS support for backup

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## 1.2 Specifications

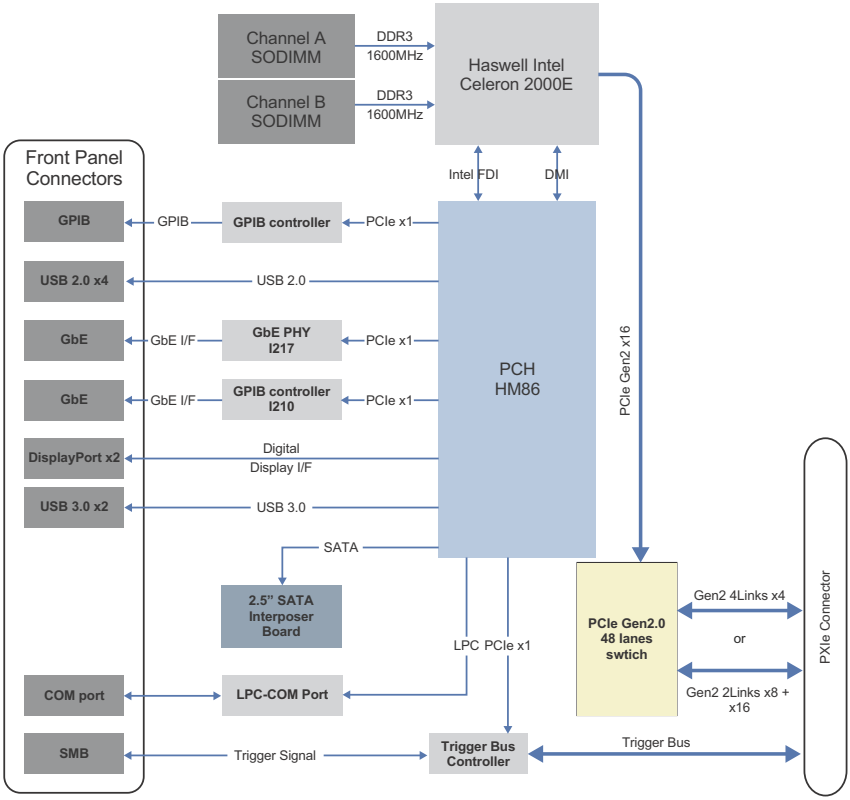



**Figure 1-1: PXIe-3935 Functional Block Diagram**

### Processor

- Intel® Celeron® 2000E 2.20GHz processor for maximum computing power
- DMI (Direct Media Interface) with 5 GT/s of bandwidth in each direction

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## Chipset

Mobile Intel® HM86

## Memory

- 2x standard 204-pin DDR3L SODIMM sockets
- Support for 1333/1600MHz RAM up to 16 GB total
- Support for non-ECC unbuffered memory



NOTE:

The externally accessible SODIMM socket can accept replacement DDR3L DRAM DIMM modules. PXIe-3935 specifications and stability guarantees are only supported when ADLINK-provided DDR3L DRAM DIMM modules are used.

## Video

- DisplayPort supports up to 3840x 2160 @60Hz resolution
- DVI (with passive DisplayPort-to-DVI adapter) supports resolutions up to 1920 x 1200 @60Hz



NOTE:

DisplayPort adapters for other standards are supported, with maximum available resolution dependent on the adapter chosen

## Hard Drive

Built-in 2.5” 500GB SATA hard drive or 240GB SATA solid state hard drive.

## I/O Connectivity

Dual Gigabit Ethernet through two RJ-45 connectors with speed/link/active LED indicators on the front panel, with both supporting Wake on LAN.

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## USB

Four USB 2.0 and two USB 3.0 ports on the front panel.

## COM port

One RS-232/422/485 D-SUB9 connector.

## GPIB

Onboard IEEE488 GPIB controller through Micro-D 25-pin connector on the front panel.

## Trigger I/O

One SMB connector on the front panel to route an external trigger signal to/from PXIe trigger bus

## Dimensions (3U PXI module)

3U/4-slot PXI standard.

80.94 W x 128.7 H x 212.9 D mm (3.15 x 5.01 x 8.3 in.)

## Weight

1.0kg (exclusive of packaging)

## Environmental

| | |
|---|---|
| Operating temperature with SSD | 0 to 55°C |
| Operating temperature with HDD | 0 to 50°C |
| Storage temperature | -20 to 70°C |
| Relative humidity , non-condensing | 5 to 95% |

## Shock and Vibration

Functional shock 30 G, half-sine, 11 ms pulse duration

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**Random vibration:**

- Operating 5 to 500 Hz, 0.21 Grms, 3 axes
- Non-operating 5 to 500 Hz, 2.46 Grms, 3 axes



NOTE:

Environmental & Shock and Vibration values are only guaranteed with use of an ADLINK-provided SSD/HDD

**Certification**

Electromagnetic compatibility:

- EMC/EMI: CE, FCC Class A
- CE Compliance EN 61326-1

The PXIe-3935 meets the essential requirements of applicable European Directives.

## Power Requirements

| Voltage Rail | +3.3V | +5V | +12V | Total (W) |
|---|---|---|---|---|
| Maximum power consumption | 3.3 | 38 | 1.2 | 42.5 |
| Idle power consumption | 3.3 | 22.5 | 1.2 | 27 |

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## 1.3 Front Panel I/O & Indicators




**Figure 1-2: Front Panel**

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The PXIe-3935 provides the following I/O and indicators, as labeled on the front panel.

- PXI Trigger Connector (SMB jack)
- 2X DisplayPort Connectors
- GPIB Connector (Micro D-Sub 25P)
- Reset Button
- LED indicators
- 4X Type-A USB 2.0
- connectors
- 2X Gigabit Ethernet
- 2X USB 3.0
- 1X COM port (D-sub9 serial)

### 1.3.1 PXIe Trigger Connector

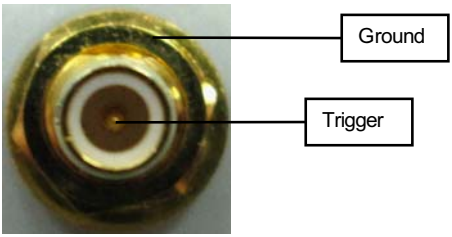



**Figure 1-3: PXIe Trigger SMB Jack**

The PXIe trigger connector is a SMB jack, used to route external trigger signals to or from the PXIe backplane. Trigger signals are TTL-compatible and edge sensitive. The PXIe-3935 provides four

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trigger routing modes from/to the PXIe trigger connector to synchronize PXIe modules, including

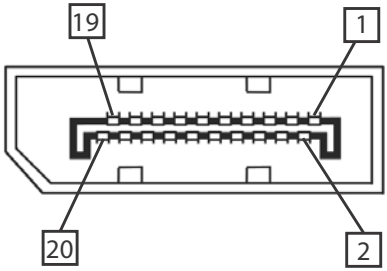
- From a selected trigger bus line to PXIe trigger connector
- From the PXIe trigger connector to a selected trigger bus line
- From software trigger to a selected trigger bus line
- From software trigger to PXIe trigger connector

All trigger modes are programmable by the provided driver. Please refer to Section A: PXIe Trigger I/O Function Reference for further information.

### 1.3.2 DisplayPort Connectors

Supporting monitor connection, with, if connecting to VGA/DVI/HDMI monitors, installation of requisite adapters required. Dual display function is also supported

.




| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | CN_DDPx0+ | 11 | GND |
| 2 | GND | 12 | CN_DDPx3- |
| 3 | CN_DDPx0- | 13 | CN_DDPx_AUX_SEL |
| 4 | CN_DDPx1+ | 14 | CN_DDPx_CONFIG2 |
| 5 | GND | 15 | CN_DDPx_AUX+ |

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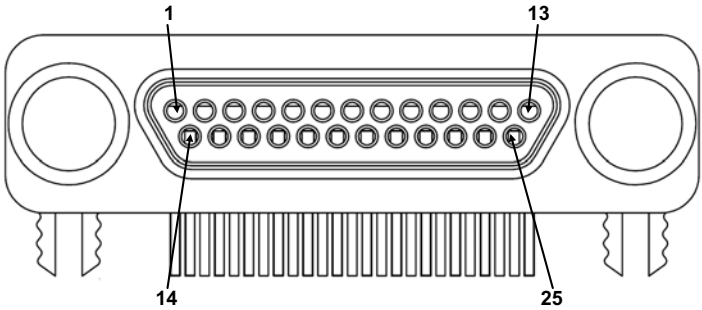
| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 6 | CN_DDPx1- | 16 | GND |
| 7 | CN_DDPx2+ | 17 | CN_DDPx_AUX- |
| 8 | GND | 18 | CN_DDPx_HPD |
| 9 | CN_DDPx2- | 19 | GND |
| 10 | CN_DDPx3+ | 20 | +V3.3_DDPx_PWR |

**Table 1-1: Display Port Pin Assignment**

### 1.3.3 GPIB Connector

The GPIB connector on PXIe-3935 is a micro D-sub 25P connector, controlling external bench-top instruments. Connection to other instruments requires the ACL-IEEE488-MD1-A cable. The on-board GPIB controller provides:

- Full compatibility with IEEE 488 standard
- Up to 1.5MB/s data transfer rates
- Onboard 2 KB FIFO for read/write operations
- Driver APIs compatible with NI-488.2 driver software
- Connection with up to 14 instruments




| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 1 | DIO1# | GPIB Data 1 | 14 | DIO5# | GPIB Data 5 |
| 2 | DIO2# | GPIB Data 2 | 15 | DIO6# | GPIB Data 6 |

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| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 3 | DIO3# | GPIB Data 3 | 16 | DIO7# | GPIB Data 7 |
| 4 | DIO4# | GPIB Data 4 | 17 | DIO8# | GPIB Data 8 |
| 5 | EOI | End Or Identify | 18 | REN | Remote Enable |
| 6 | DAV | Data Valid | 19 | Ground | Signal Ground |
| 7 | NRFD | Not Ready For Data | 20 | Ground | Signal Ground |
| 8 | NDAC | No Data Accepted | 21 | Ground | Signal Ground |
| 9 | IFC | Interface Clear | 22 | Ground | Signal Ground |
| 10 | SRQ | Service Request | 23 | Ground | Signal Ground |
| 11 | ATN | Attention | 24 | Ground | Signal Ground |
| 12 | Chassis Ground | Chassis Ground | 25 | Ground | Signal Ground |
| 13 | Ground | Signal Ground | | | |

**Table 1-2: GPIB Pin Description**

### 1.3.4 Reset Button

The reset button, activated by insertion of any pin-like implement, executes a hard reset for the PXIe-3935.

### 1.3.5 LED Indicators

Four LED indicators on the front panel indicate operational status of the PXIe-3935, as follows.




**Figure 1-4: LED Indicators**

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| LED | Color | Description |
|---|---|---|
| PW | Green | Indicates system power, remaining lit when the system boots normally and main power supply is functioning |
| HD | Yellow | Indicates operating state of the HDD or SSD, flashing during access to or activity on the SATA HDD. |
| USR | Blue | User-programmable LED indicator |

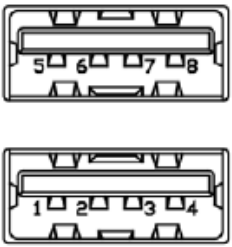
**Table 1-3: LED Indicator Legend**

NOTE:

In the event of malfunction, clear the CMOS (See “Clearing CMOS” on page 23.) and reboot the system. If the system fails to respond properly, please contact ADLINK for assistance.

### 1.3.6 USB 2.0 Ports

The PXIe-3935 provides four USB 2.0 ports via USB Type A connectors on the front panel, all compatible with hi-speed, full-speed and low-speed USB devices. Supported boot devices include USB flash drive, USB floppy, USB CD-ROM, and others, with boot priority and device settings configurable configured in BIOS. See “Boot Setup” on page 38. for more information.




| Pin | Signal |
|---|---|
| 1/5 | Power 5V |

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| Pin | Signal |
|---|---|
| 2/6 | USB Data- |
| 3/7 | USB Data + |
| 4/8 | Ground |

**Table 1-4: USB 2.0 Port Pin Assignment**

### 1.3.7 Gigabit Ethernet Ports

Dual Gigabit Ethernet connection is provided on the PXIe-3935 front panel.

| Pin | 1000Base-T Signal | 100/10Base-T Signal |
|---|---|---|
| 1 | MDI0+ | TX+ |
| 2 | MDI0- | TX- |
| 3 | MDI1+ | RX+ |
| 4 | MDI2+ | Reserved |
| 5 | MDI2- | Reserved |
| 6 | MDI1- | RX- |
| 7 | MDI3+ | Reserved |
| 8 | MDI3- | Reserved |

**Table 1-5: PXIe-3935 Ethernet Port Pin Assignments**

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The Ethernet ports each include two LED indicators, one Active/ Link indicator and one Speed indicator, functioning as follows.

| | LED | Status | Description |
|---|---|---|---|
|  | Active/Link (Yellow) | Off | Ethernet port is disconnected |
| | | On | Ethernet port is connected with no data transmission |
| | | Flashing | Ethernet port is connected with data transmitted/received |
| | Speed (Green/ Orange) | Off | 10 Mbps |
| | | Green | 100 Mbps |
| | | Orange | 1000 Mbps |

### 1.3.8 COM Port

The COM port with D-sub 9P connectors supports RS-232/RS-422/RS-485 according to BIOS setting.

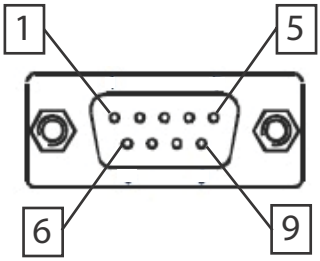



**Figure 1-5: COM Port**

| Pin | Signal | | |
|---|---|---|---|
| | RS-232 | RS-422 | RS-485 |
| 1 | DCD# | TXD422- | 485DATA- |
| 2 | RXD | TXD422+ | 485DATA+ |

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| Pin | Signal | | |
|---|---|---|---|
| 3 | TXD | RXD422+ | N/S |
| 4 | DTR# | RXD422- | N/S |
| 5 | GND | N/S | N/S |
| 6 | DSR# | N/S | N/S |
| 7 | RTS# | N/S | N/S |
| 8 | CTS# | N/S | N/S |
| 9 | RI# | N/S | N/S |

**Table 1-6: D-Sub 9p COM Port Signal Functions**

### 1.3.9 USB 3.0 Ports

The PXIe-3935 provides two Type A USB 3.0 ports on the front panel, supporting SuperSpeed, Hi-Speed, full-speed, and low-speed transmission for downstream. Multiple boot devices, including USB flash, USB external HD, and USB CD-ROM drives are supported, with boot priority configured in BIOS.


NOTE:

While the USB 3.0 ports allow boot from CD-ROM, OS installation via CD-ROM is not supported

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### 1.3.10 Onboard Connections and Settings

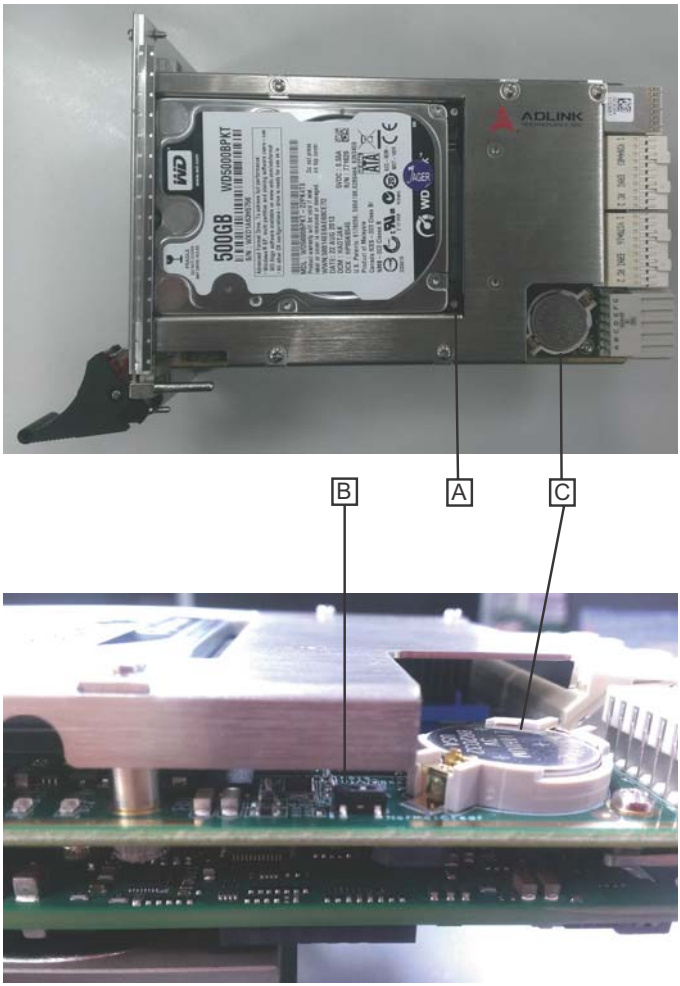



**Figure 1-6: PXIe-3985 Onboard Configuration**

| | |
|---|---|
| A | SATA Connector |
| B | Clear CMOS switch |
| C | System Battery |

**Table 1-7: Onboard Configuration Legend**

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# 2 Getting Started

This chapter describes procedures for installing the PXIe-3935 and making preparations for its operation, including hardware and software setup. Please note that the PXIe-3935 is shipped with RAM and HDD or SSD preinstalled. Please contact ADLINK or authorized dealer if there are any problems during the installation.




Diagrams and illustrated equipment are for reference only. Actual system configuration and specifications may vary.

## 2.1 Package Contents

Before beginning, check the package contents for any damage and ensure that the following items are included:

- PXIe-3985 Controller (equipped with RAM and HDD or SSD)
- DisplayPort-to-DVI adapter
- Quick Start Guide

If any of these items are missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.




Do not install or apply power to equipment that is damaged or missing components. Retain the shipping carton and packing materials for inspection. Please contact your ADLINK dealer/ vendor immediately for assistance and obtain authorization before returning any product.

## 2.2 Operating System Installation

For more detailed information about the operating system, refer to the documentation provided by the operating system manufacturer. Preferred/supported operating systems for PXIe-3935 are:

- Windows 7 32/64-bit
- For other OS support, please contact ADLINK

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Most operating systems require initial installation from a hard drive, floppy drive, or CD-ROM drive. The PXIe-3935 controller supports USB CD-ROM drive, USB flash disk, USB external hard drive, or a USB floppy drive as the first boot device. See “Boot Setup” on page 38. for information about setting the boot devices. These devices should be configured, installed, and tested with the supplied drivers before attempting to load the new operating system.


NOTE:

Read the release notes and installation documentation provided by the operating system vendor. Be sure to read all the README files or documents provided on the distribution disks, as these typically note documentation discrepancies or compatibility problems.

1. Select the appropriate boot device order from the BIOS Boot Setup Menu based on the OS installation media used. For example, if the OS is distributed on a bootable installation CD, select USB CD-ROM as the first boot device and reboot the system with the installation CD in the USB CD-ROM drive
2. Proceed with the OS installation as directed and be sure to select appropriate device types if prompted. Refer to the appropriate hardware manuals for specific device types and compatibility modes of ADLINK PXIe products.
3. When installation is complete, reboot the system and set the boot device order in the SETUP boot menu accordingly.

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### 2.2.1 Driver Installation

Download requisite drivers, as follows, from http://www.adlink-tech.com.

1. Fully install Windows, which contains most standard I/O device drivers
2. Install the chipset driver
3. Install the graphic driver
4. Install the Ethernet driver
5. Install the GPIB driver
6. Install the management engine driver
7. Install the PXIe trigger driver
8. Install the USB 3.0 driver

### 2.2.2 Installation Environment

When preparing to install any equipment described in this manual, see “Chapter A: Important Safety Instructions.

Only install equipment in well lit areas on flat, sturdy surfaces with access to basic tools such as flat- and cross-head screwdrivers, preferably with magnetic heads as screws and standoffs are small and easily misplaced.

#### Recommended Installation Tools

- Phillips (cross-head) screwdriver
- Flat-head screwdriver
- Anti-static wrist strap
- Anti-static mat

ADLINK PXIe-3935 system controllers are electrostatically sensitive and can be easily damaged by static electricity. The equipment must be handled on a grounded anti-static mat, and operators must wear an anti-static wristband, grounded at the same point as the anti-static mat.

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Inspect the carton and packaging for damage. Shipping and handling may cause damage to the contents. Ensure that all contents are undamaged before installing.




All equipment must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the equipment and wear a grounded wrist strap when servicing or installing.

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### 2.2.3 Installing the PXIe-3935

1. Locate the system controller slot (Slot 1)
2. Depress the red locking lever and release the latch
3. Align the controller's top and bottom edges with the card guides, and carefully slide the PXIe-3935 into the chassis, as shown




4. Elevate the latch until the PXIe-3935 is fully seated in the chassis backplane.
5. Fasten the four mounting screws on the front panel of PXIe-3935, and connect all peripheral devices.

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### 2.2.4 Replacing the Hard Drive or Solid State Drive

The PXIe-3935 provides a SATA 2.0 port with a pre-installed 2.5" SATA hard drive or solid state drive. Replacing the HDD or SSD is accomplished as follows.

1. Locate the five screws attaching the drive to the bracket on the side of the PXIe-3935.
2. Remove the screws, as shown.




3. Gently lift and remove the SATA HDD or SSD
4. To install a HDD or SSD or other compatible SATA hard drive, reverse the steps and reinstall the PXIe-3935 into the PXIe system.

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### 2.2.5 Replacing the Battery Backup

The PXIe-3935 is provided with a 3.0 V “coin cell” lithium battery, replacement of which is as follows.

1. Turn off the PXIe chassis.
2. Remove the PXIe-3935 embedded controller from the chassis. Observe all anti-static precautions.
3. To remove the battery, gently insert a small (approx. 5 mm) flathead screwdriver under the battery at the negative retaining clip. Gently pry up and the battery should easily pop out.
4. Place a fresh identical battery (CR2032 or equivalent) in the socket, ensuring that the positive pole (+) is facing upwards. The battery is most easily seated by first being inserted under the positive retaining clip, and then pushed downward at the negative retaining clip. The battery should easily snap into position.
5. Reinstall the embedded controller into the PXIe chassis and restore power.

### 2.2.6 Clearing CMOS

In the event of a system malfunction causing the PXIe-3935 to halt or fail to boot, clear the CMOS and restore the controller BIOS to its default settings. To clear the CMOS:

1. Shut down the controller operating system and turn off the PXIe Chassis.
2. Remove the PXIe-3935 from the chassis. Observe all anti-static precautions.
3. Locate the CMOS clear switch (SW1) on the board (See “Onboard Connections and Settings” on page 16.). Move the switch from Normal position




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to Clear position




and wait for 5 seconds, then return the switch to Normal position.

4. Remount the controller into the PXIe chassis.
5. Press "Delete" or "ESC" to enter the BIOS setup when the splash logo appears.
6. Press "F3" to load Optimized defaults in BIOS setup
7. Modify the system date and time
8. Press "F4" to save configuration and exit

### 2.2.7 Initiating Backup BIOS Flash

BIOS flash on the PXIe-3935 is divided into Backup and Normal sections. In the event of a system malfunction causing the active PXIe-3935 BIOS to crash and then fail to boot, the system automatically switches to the secondary backup BIOS.

NOTE: Please contact technical support to resolve halting or failure to boot issues caused by corrupted BIOS.

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# Appendix A - PXIe Trigger I/O Function Reference

This appendix describes use of the PXIe trigger I/O function library for the PXIe-3935 controller, to program routing of trigger signals between the trigger I/O SMB connector on the front panel and the PXIe trigger bus on the backplane.

## A.1 Data Types

The PXIe-3935 library uses these data types in pxitrigio.h in the directory X:\ADLINK\PXIe Trigger IO\Include. It is recommended that you use these data types in your application programs. The table shows the data type names, ranges, and corresponding data types in C/C++, Visual Basic, and Delphi for reference.

| Type | Description | Range | Type | | |
|---|---|---|---|---|---|
| | | | C/C++ (for 32-bit compiler) | Visual Basic | Pascal (Delphi) |
| U8 | 8-bit ASCII character | 0 to 255 | unsigned char | Byte | Byte |
| I16 | 16-bit signed integer | -32768 to 32767 | short | Integer | SmallInt |
| U16 | 16-bit unsigned integer | 0 to 65535 | unsigned short | Not supported by BASIC, use the signed integer (I16) instead | Word |
| I32 | 32-bit signed integer | -2147483648 to 2147483647 | long | Long | LongInt |
| U32 | 32-bit unsigned integer | 0 to 4294967295 | unsigned long | Not supported by BASIC, use the signed long integer (I32) instead | Cardinal |

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| Type | Description | Range | Type | | |
|---|---|---|---|---|---|
| | | | C/C++ (for 32-bit compiler) | Visual Basic | Pascal (Delphi) |
| F32 | 32-bit single-precision floating-point | -3.402823E38 to 3.402823E38 | float | Single | Single |
| F64 | 64-bit double-precision floating-point | 1.797683134862315E308 to 1.797683134862315E309 | double | Double | Double |

## A.2 Function Library

This section provides detailed definitions of the functions available in the PXIe-3935 function library. Each function includes a description, list of supported cards, syntax, parameter list and Return Code information.

### A.2.1 TRIG_Init

**Description**

Initializes trigger I/O function of PXIe-3935 controller. TRIG_Init must be called before the invocation of any other trigger I/O function.

**Supported Controllers**

PXIe-3935, PXI-3980

**Syntax**

C/C++

```
I16 TRIG_Init()
```

Visual Basic

```
TRIG_Init As Integer
```

**Parameter**

*None*

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**Return Code**

```
ERR_NoError
ERR_BoardBusy
ERR_OpenDriverFail
ERR_GetGPIOAddress
```

### A.2.2 TRIG_Close

**Description**

Closes trigger I/O function of PXIe-3935 controller, releasing resources allocated for the trigger I/O function. Users must invoke TRIG_Close before exiting the application.

**Supported Controllers**

PXIe-3935, PXI-3980

**Syntax**

C/C++

```
I16 TRIG_Close()
```

Visual Basic

```
TRIG_Close() As Integer
```

**Parameter**

None

**Return Code**

```
ERR_NoError
ERR_BoardNoInit
```

### A.2.3 TRIG_SetSoftTrg

**Description**

Generates a TTL trigger signal to the trigger I/O SMB connector on the front panel or the PXIe trigger bus on the backplane by software command

**Supported Controllers**

PXIe-3935, PXI-3980

**Syntax**

C/C++

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```
I16 TRIG_SetSoftTrg(U8 Status)
```

Visual Basic

```
TRIG_SetSoftTrg (ByVal status As Byte) As
Integer
```

**Parameters**

*Status*

Logic level of trigger signal.

*Available value description:*

0: Logic low

1: Logic high

**Return Code**

```
ERR_NoError
ERR_BoardNoInit
```

### A.2.4 TRIG_Trigger_Route

**Description**

Routes the trigger signal between the trigger I/O SMB connector on the front panel and the PXIe trigger bus on the backplane. This function also allows routing of the software-generated trigger signal to SMB connector or trigger bus.

**Supported Controllers**

PXIe-3935, PXI-3980

**Syntax**

C/C++

```
I16 TRIG_Trigger_Route (U32 source, U32 dest,
U32 halfway)
```

Visual Basic

```
TRIG_Trigger_Route (ByVal source As Long,
ByVal dest As Long, ByVal halfway As Long) As
Integer
```

**Parameters**

*source*

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Source of trigger routing. It can be one of the following values.

| Available value | Description |
|---|---|
| PXI_TRIG_VAL_SMB | SMB connector on the front panel |
| PXI_TRIG_VAL_SOFT | Software-generated trigger signal |
| PXI_TRIG_VAL_TRIG0 | PXIe trigger bus #0 |
| PXI_TRIG_VAL_TRIG1 | PXIe trigger bus #1 |
| PXI_TRIG_VAL_TRIG2 | PXIe trigger bus #2 |
| PXI_TRIG_VAL_TRIG3 | PXIe trigger bus #3 |
| PXI_TRIG_VAL_TRIG4 | PXIe trigger bus #4 |
| PXI_TRIG_VAL_TRIG5 | PXIe trigger bus #5 |
| PXI_TRIG_VAL_TRIG6 | PXIe trigger bus #6 |
| PXI_TRIG_VAL_TRIG7 | PXIe trigger bus #7 |

*dest*

Destination of trigger routing. It can be one of the following values.

| Available value | Description |
|---|---|
| PXI_TRIG_VAL_SMB | SMB connector on the front panel |
| PXI_TRIG_VAL_TRIG0 | PXIe trigger bus #0 |
| PXI_TRIG_VAL_TRIG1 | PXIe trigger bus #1 |
| PXI_TRIG_VAL_TRIG2 | PXIe trigger bus #2 |
| PXI_TRIG_VAL_TRIG3 | PXIe trigger bus #3 |
| PXI_TRIG_VAL_TRIG4 | PXIe trigger bus #4 |
| PXI_TRIG_VAL_TRIG5 | PXIe trigger bus #5 |
| PXI_TRIG_VAL_TRIG6 | PXIe trigger bus #6 |
| PXI_TRIG_VAL_TRIG7 | PXIe trigger bus #7 |

*halfway*

Halfway point of trigger routing. This parameter is used only to route the software-generated trigger signal to the SMB connector on the front panel. In this case, the halfway

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should be set as one of the trigger bus lines, otherwise as PXI_TRIG_VAL_NONE.

| Available value | Description |
|---|---|
| PXI_TRIG_VAL_NONE | No halfway point |
| PXI_TRIG_VAL_TRIG0 | PXIe trigger bus #0 |
| PXI_TRIG_VAL_TRIG1 | PXIe trigger bus #1 |
| PXI_TRIG_VAL_TRIG2 | PXIe trigger bus #2 |
| PXI_TRIG_VAL_TRIG3 | PXIe trigger bus #3 |
| PXI_TRIG_VAL_TRIG4 | PXIe trigger bus #4 |
| PXI_TRIG_VAL_TRIG5 | PXIe trigger bus #5 |
| PXI_TRIG_VAL_TRIG6 | PXIe trigger bus #6 |
| PXI_TRIG_VAL_TRIG7 | PXIe trigger bus #7 |

**Return Code**

```
ERR_NoError
ERR_BoardNoInit
ERR_Set_Path
```

### A.2.5 TRIG_Trigger_Clear

**Description**

Clears the trigger routing setting

**Supported Controllers**

PXIe-3935, PXI-3980

**Syntax**

C/C++

```
I16 TRIG_Trigger_Clear()
```

Visual Basic

```
TRIG_Trigger_Clear() As Integer
```

**Parameters**

None

**Return Code**

```
ERR_NoError
ERR_BoardNoInit
```

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```
ERR_Trigger_Clr
```

### A.2.6 TRIG_GetSoftTrg

#### Description

Acquires the current software trigger state, with default state after system boot of Logic Low

#### Supported Controllers

PXIe-3935, PXI-3980

#### Syntax

C/C++

```
I16 TRIG_GetSoftTrg(U8 *Status)
```

Visual Basic

```
TRIG_GetSoftTrg (status As Byte) As Integer
```

#### Parameters

*Status*

Returns the logic level of software trigger signal

Returned value:

0: Logic low

1: Logic high

#### Return Code

```
ERR_NoError
ERR_BoardNoInit
ERR_Query_Status
```

### A.2.7 TRIG_Trigger_Route_Query

#### Description

Acquires the current trigger signal routing path

#### Supported Controllers

PXIe-3935, PXI-3980

#### Syntax

C/C++

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```
I16  TRIG_Trigger_Route_Query  (U32*  source,
U32* dest, U32* halfway)
```

Visual Basic

```
TRIG_Trigger_Route_Query (source As Long, dest
As Long, halfway As Long) As Integer
```

**Parameters**

*source*

Returns to the current source of trigger routing, with possible values including:

| Available Definition | Defined Value |
|---|---|
| PXI_TRIG_VAL_NONE | 0 |
| PXI_TRIG_VAL_SMB | 2 |
| PXI_TRIG_VAL_SOFT | 3 |
| PXI_TRIG_VAL_TRIG0 | 111 |
| PXI_TRIG_VAL_TRIG1 | 112 |
| PXI_TRIG_VAL_TRIG2 | 113 |
| PXI_TRIG_VAL_TRIG3 | 114 |
| PXI_TRIG_VAL_TRIG4 | 115 |
| PXI_TRIG_VAL_TRIG5 | 116 |
| PXI_TRIG_VAL_TRIG6 | 117 |
| PXI_TRIG_VAL_TRIG7 | 118 |

*dest*

Returns to the current destination of trigger routing, with possible values including:

| Available Definition | Defined Value |
|---|---|
| PXI_TRIG_VAL_NONE | 0 |
| PXI_TRIG_VAL_SMB | 2 |
| PXI_TRIG_VAL_TRIG0 | 111 |
| PXI_TRIG_VAL_TRIG1 | 112 |
| PXI_TRIG_VAL_TRIG2 | 113 |
| PXI_TRIG_VAL_TRIG3 | 114 |
| PXI_TRIG_VAL_TRIG4 | 115 |

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| Available Definition | Defined Value |
|---|---|
| PXI_TRIG_VAL_TRIG5 | 116 |
| PXI_TRIG_VAL_TRIG6 | 117 |
| PXI_TRIG_VAL_TRIG7 | 118 |

*halfway*

Returns to the current halfway point of trigger routing, with possible values including:

| Available Value | Description |
|---|---|
| PXI_TRIG_VAL_NONE | 0 |
| PXI_TRIG_VAL_TRIG0 | 111 |
| PXI_TRIG_VAL_TRIG1 | 112 |
| PXI_TRIG_VAL_TRIG2 | 113 |
| PXI_TRIG_VAL_TRIG3 | 114 |
| PXI_TRIG_VAL_TRIG4 | 115 |
| PXI_TRIG_VAL_TRIG5 | 116 |
| PXI_TRIG_VAL_TRIG6 | 117 |
| PXI_TRIG_VAL_TRIG7 | 118 |

**Return Code**

```
ERR_NoError
ERR_BoardNoInit
ERR_Query_Status
```

### A.2.8 TRIG_GetDriverRevision

**Description**

Acquires the PXIe Trigger software driver version; format of the version number is major.minor1.minor2

**Supported Controllers**

PXIe-3935, PXI-3980

**Syntax**

C/C++

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```
I16    TRIG_GetDriverRevision(unsigned    short
*major, unsigned short *minor1, unsigned short
*minor2)
```

Visual Basic

```
TRIG_GetDriverRevision   (major   As   Integer,
minor1 As Integer, minor2 As Integer) As Inte-
ger
```

**Parameters**

*major*

Returns the major version number of the PXIe trigger software driver

*minor1*

Returns the first minor version number of the PXIe trigger software driver

*minor2*

Returns the second minor version number of the PXIe trigger software driver

**Return Code**

```
ERR_NoError
ERR_Query_Revision
```

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# Appendix B BIOS Setup

The Basic Input/Output System (BIOS) provides a basic level of communication between the processor and peripherals. In addition, the BIOS also contains code for various advanced features applied to the PXIe-3935 controller. The BIOS setup program includes menus for configuring settings and enabling PXIe-3935 controller features.




Changing BIOS settings may result in incorrect operation and possibly an inability to boot. If this occurs, follow the instructions in Section 2.2.6: Clearing CMOS to clear CMOS and restore default settings. In general, do not change a BIOS setting unless you are absolutely certain of the consequences.

## B.1 Starting the BIOS

1. Power on or reboot the PXIe-3935 controller.
2. Press the <Delete> key when the controller beeps. This should be concurrent with the main startup screen. The BIOS setup program loads after a short delay.
3. The Main menu is displayed when you first enter the BIOS setup program.




In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

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## Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most BIOS setup utility hot keys can be used at any time during setup navigation, as follows.

| Key(s) | Function |
|---|---|
| Right Arrow, Left Arrow | Moves between different setup menus |
| Up Arrow, Down Arrow | Moves between options within a setup menu |
| <Enter> | Opens a submenu or displays all available settings for a highlighted configuration option |
| <Esc> | Returns to the previous menu and shortcuts to the Exit menu from top-level menus |
| <+> and <–> | Cycles between all available settings |
| <Tab> | Selects time and date fields |
| <F1> | Opens the general help window for the BIOS |
| <F2> | Loads previous values into the BIOS |
| <F3> | Loads the optimal default BIOS settings |
| <F4> | Saves the current configuration and exits BIOS setup |

**Table B-1: BIOS Hot Key Functions**

NOTE: A hot key legend is located in the right frame on most setup screens.

The < F8 > key on your keyboard is the Fail-Safe key. It is not displayed on the key legend by default. To set the Fail-Safe settings of the BIOS, press the < F8 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

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## B.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab.

The Main Setup menu provides basic controller information and allows the system time and date to be set, as follows.

| Item | |
|---|---|
| BIOS Information | Includes BIOS version and date |
| System Information | Lists processor and PCH information |
| System Management | Includes board information and system health data |
| **System Date & Time** | |
| System Date | Sets system date, entered in MM/DD/YY format |
| System Time | Sets system time, entered in HH:MM:SS format. |
| Access Level | Displays current access level, default is Administrator |

**Table B-2: BIOS Main Setup Menu**

## B.3 Advanced Setup

Select the Advanced tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the submenu for that item. Display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. The Advanced BIOS Setup options are as follows.

| Item | |
|---|---|
| CPU Configuration | Displays processor type, speed, system bus speed, and other information |
| Memory Configuration | Displays memory information |
| Graphics Configuration | Configures graphics |

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| Item | |
|---|---|
| USB Configuration | Provides USB support and lists devices in USB ports |
| Hardware Health Configuration | Displays system voltages and temperatures |
| Onboard Device Configuration | Enables/disables LAN and SATA ports |
| Advanced Power Management | Shows Watch Dog Timer status |

**Table B-3: BIOS Advanced Setup Menu**

## B.4 Boot Setup

| Item | |
|---|---|
| **Boot Configuration** | |
| Setup Prompt Timeout | Sets time window in which Setup key can be selected, in seconds |
| Boot Numlock State | Sets keyboard Numlock status |
| Quiet Boot | When disabled, allows POST messages to be viewed, with default Enabled |
| Fast Boot | Sets boot with initialization of minimal devices required to launch active boot option |
| **Boot Option Priorities** | |
| 1st Boot | Selects primary boot source, with default SATA HDD |
| 2nd Boot | Selects secondary boot source |
| Hard Drive BBS Priorities | Sets order of legacy devices in this group |

**Table B-4: BIOS Boot Setup Menu**

## B.5 Security Setup

The system can be configured to require all users to enter a password (either Administrator or User) every time the system boots or when Setup is executed. Administrators and User passwords activate different levels of security.

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If passwords are used, the system prompts for a three- to twenty-character password. Typed passwords are not displayed.

| Item | |
|---|---|
| **Password Description** | |
| Administrator Password | Sets administrative level password for BIOS |
| User Password | Sets user level passwords for BIOS |

**Table B-5: BIOS Security Setup Menu**




Passwords are not recoverable. Please ensure that all passwords are recorded elsewhere. If your passwords are lost, NVRAM must be erased and reconfigured.

## B.6 Save & Exit Setup

The following options for saving and exiting can be chosen in this menu.

### Save Changes and Exit

- Save Changes and Reset
- Discard Changes and Reset

### Save Option

- Save Changes
- Discard Changes
- Restore Defaults
- Save as User Defaults
- Restore User Defaults

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NOTE:

The "Restore the default values for all setup options” selection does not restore the original boot priority sequence. You must use the Boot Setup Menu (see “Boot Setup” on page 38) to manually restore the boot priority sequence.

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# Important Safety Instructions

For user safety, please read and follow all instructions, Warnings, Cautions, and Notes marked in this manual and on the associated device before handling/operating the device, to avoid injury or damage.

*S'il vous plaît prêter attention stricte à tous les avertissements et mises en garde figurant sur l'appareil , pour éviter des blessures ou des dommages.*

- Read these safety instructions carefully
- Keep the User's Manual for future reference
- Read the Specifications section of this manual for detailed information on the recommended operating environment
- The device can be operated at an ambient temperature of 50ºC
- When installing/mounting or uninstalling/removing device; or when removal of a chassis cover is required for user servicing (See "Getting Started" on page 17.):
  - Turn off power and unplug any power cords/cables
  - Reinstall all chassis covers before restoring power
- To avoid electrical shock and/or damage to device:
  - Keep device away from water or liquid sources
  - Keep device away from high heat or humidity
  - Keep device properly ventilated (do not block or cover ventilation openings)
  - Always use recommended voltage and power source settings
  - Always install and operate device near an easily accessible electrical outlet
  - Secure the power cord (do not place any object on/over the power cord)
  - Only install/attach and operate device on stable surfaces and/or recommended mountings
- If the device will not be used for long periods of time, turn off and unplug from its power source

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- Never attempt to repair the device, which should only be serviced by qualified technical personnel using suitable tools
- A Lithium-type battery may be provided for uninterrupted backup or emergency power.

---




Risk of explosion if battery is replaced with one of an incorrect type; please dispose of used batteries appropriately.
*Risque d'explosion si la pile est remplacée par une autre de type incorrect. Veuillez jeter les piles usagées de façon appropriée.*

---

- The device must be serviced by authorized technicians when:
  - The power cord or plug is damaged
  - Liquid has entered the device interior
  - The device has been exposed to high humidity and/or moisture
  - The device is not functioning or does not function according to the User's Manual
  - The device has been dropped and/or damaged and/or shows obvious signs of breakage
- Disconnect the power supply cord before loosening the thumbscrews and always fasten the thumbscrews with a screwdriver before starting the system up
- It is recommended that the device be installed only in a server room or computer room where access is:
  - Restricted to qualified service personnel or users familiar with restrictions applied to the location, reasons therefor, and any precautions required
  - Only afforded by the use of a tool or lock and key, or other means of security, and controlled by the authority responsible for the location

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| | |
|---|---|
|  | **BURN HAZARD**<br>Touching this surface could result in bodily injury. To reduce risk, allow the surface to cool before touching.<br>***RISQUE DE BRÛLURES***<br>*Ne touchez pas cette surface, cela pourrait entraîner des blessures.*<br>*Pour éviter tout danger, laissez la surface refroidir avant de la toucher.* |

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# Getting Service

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