PXIe-9529H

User's Manual

8-CH 24-Bit 256 kS/s
Dynamic Signal Acquisition Module



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Revision History

Revision	Description	Date	By
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1.1	Crosstalk spec updated	2025-06-12	CC

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Preface

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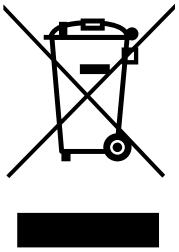
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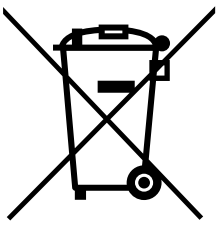
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Battery Labels (for products with battery)









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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.



NOTE:

Additional information, aids, and tips that help users perform tasks.



CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.



WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

1.1 Overview

The PXIe-9529H is a high-performance 8-CH 24-bit 256 kS/s dynamic signal acquisition module, specifically designed for structural health monitoring, noise, vibration, and harshness (NVH) measurement, and phased array data acquisition.

The PXIe-9529H features 24-bit simultaneous sampling at 256 kS/s over 8 channels, and a 105 dB dynamic range, providing ample power for high-density, high channel count signal measurement, and vibration-optimized lower AC cutoff frequency of 0.3 Hz. All input channels incorporate a 4 mA bias current for integrated electronic piezoelectric (IEPE) signal conditioning for accelerometers and microphones.

The PXIe-9529H is auto-calibrated with an onboard reference circuit calibrating offset and acquiring analog input errors. Following auto-calibration, the calibration constant is stored in EEPROM, so these values can be loaded and used as needed by the board. There is no requirement to calibrate the module manually.

1.2 Features

- 24-bit high-resolution
- 8 simultaneous analog inputs
- 256 kS/s maximum sampling rate with 105 dB dynamic range
- AC(0.3Hz), or DC coupling, software selectable
- IEPE – 4mA, software configurable

1.3 Applications

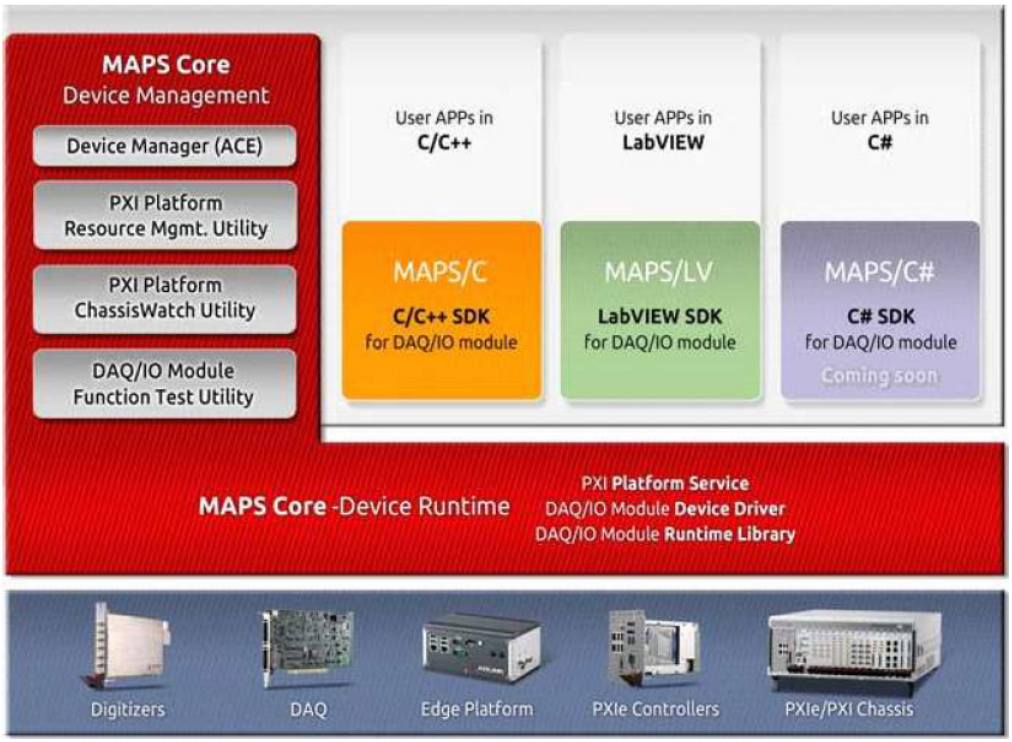
- Structural health monitoring
- Phase array data acquisition
- Noise, vibration, and harshness (NVH) detection
- Machine status monitoring

1.4 Software Support

ADLINK provides versatile software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW. All software can be downloaded from the ADLINK official website. Commercial software drivers are protected with licensing authorization codes. Without an authorization code, you can install and run the demo version for trial/demonstration purposes for up to two hours. Contact your ADLINK dealer to purchase a software license. ADLINK Measurement, Automation & Platform Service (MAPS) is a software service package designed for data acquisition, automation, and PXI platforms.

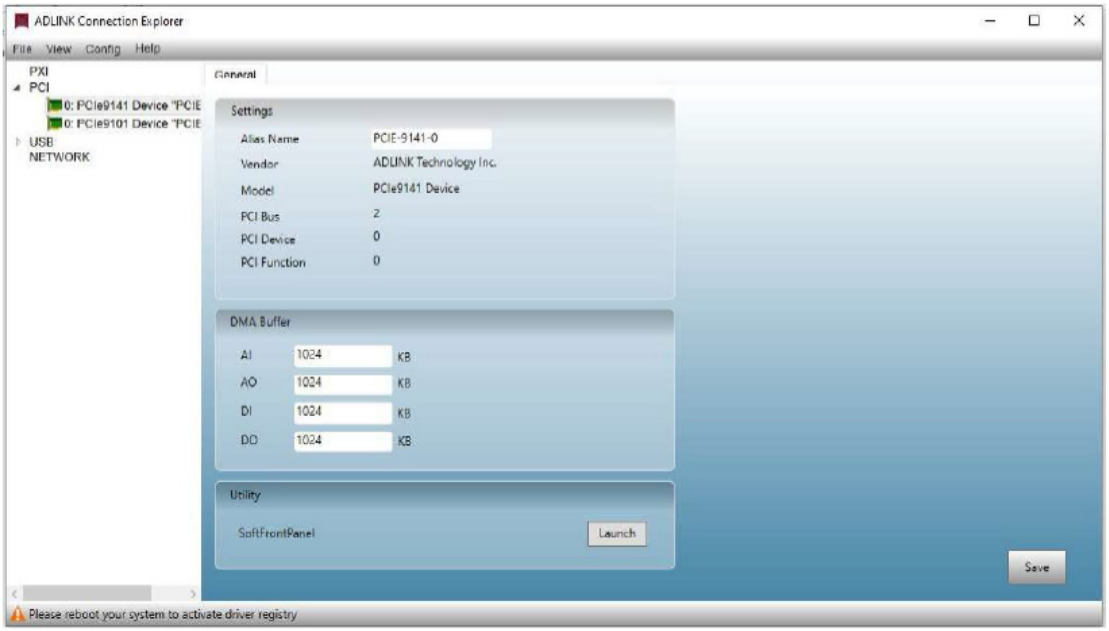
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By leveraging low-level kernel management and a user-friendly API, users can easily manage devices under a Windows environment and focus on developing applications.



1.4.1 MAPS Core

ADLINK MAPS Core is a software package that includes all the device drivers for Windows and a system-level management tool called ACE (ADLINK Connection Explorer). With MAPS Core installed, the operating system can identify ADLINK devices and assign the necessary resources for low-level access, such as IO read/write or direct memory access. MAPS Core is necessary for all ADLINK DAQ modules. To ensure the user has the latest software, go to the ADLINK product webpage or contact ADLINK technical service. MAPS Core also comes with a system management portal called ADLINK Connection Explorer (ACE). Through ACE, users can discover and manage ADLINK DAQ modules to reserve a certain size of memory buffer for DMA operation or set the user alias name for operating the module in a LabVIEW environment.



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ADLINK Connection Explorer (ACE) also provides a ready-to-use soft-front panel for digitizer products. Clicking the Launch button in the "Utility" block allows users to control DAQ cards through the UI and display the acquired waveform/data on the screen.

1.4.2 MAPS/LV, LabVIEW Support

Customers who develop their own programs in LabVIEW must install the MAPS/LV software package. MAPS/LV, also called DAQ-LabVIEW Plus, includes the software library and sample program for LabVIEW. For more information, download and install the latest MAPS/LV software from the following website and refer to the MAPS/LV manual:

https://www.adlinktech.com/Products/Data_Acquisition/DAQSoftware_Utility/MAPS_LV

1.4.3 MAPS/C, C& C++ Support

Customers who develop their own programs in a C or C++ environment must install the MAPS/C software package. MAPS/C includes all the software components required for developing applications in C/C++, such as header files, a device API library, and versatile sample programs for understanding how to manipulate the device correctly. Find the latest MAPS/C on the ADLINK website.

https://www.adlinktech.com/Products/Data_Acquisition/DAQSoftware_Utility/MAPS_C

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2 Getting Started

This chapter describes proper installation environment, installation procedures, package contents, and basic information users should be aware of regarding the PCIe-9529H.



Diagrams and illustrated equipment are for reference only.

Actual system configuration and specifications may vary.

2.1 Installation Environment

When unpacking and preparing to install, please refer to Important Safety Instructions.

Only install equipment in well-lit areas on flat, sturdy surfaces with access to basic tools such as flat- and cross-head screwdrivers, preferably with magnetic heads as screws and standoffs are small and easily misplaced.

Recommended Installation Tools

- Philips (cross-head) screwdriver
- Flat-head screwdriver
- Anti-static wrist strap
- Antistatic mat

ADLINK PXIe-9529H DSA modules are electrostatically sensitive and can be easily damaged by static electricity. The module must be handled on a grounded anti-static mat. The operator must wear an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the carton and packaging for damage, as shipping and handling could affect the equipment inside. Ensure that the equipment and its components are undamaged before installation.



The equipment must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the equipment and wear a grounded wrist strap when servicing.

Package Contents

- PXIe-9529H dynamic signal acquisition module

If the item is missing or damaged, please contact the dealer.



Do not install or power on damaged equipment or equipment missing components. Retain the shipping carton and packing materials for inspection. Contact your ADLINK dealer/vendor immediately for assistance and obtain authorization before returning any product.

2.2 Module Installation

1. Turn off the PXI system/chassis and disconnect the power cable from the power source.
2. Align the module edge with the module guide in the PXI chassis.
3. Slide the module into the chassis until resistance is felt from the PXI connector.
4. Push the ejector upwards and firmly seat the module into the chassis.
5. Once the module is fully seated, a “click” can be heard from the ejector latch.
6. Tighten the screw on the front panel.
7. Connect the power plug to a power source and turn on the PXI system/chassis.

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3 Specifications

3.1 Analog Input

Analog Input		
Number of Channels		8 (simultaneously)
Resolution		24-bit
Sampling Rate		8 kS/s to 256 kS/s
Bandwidth (-3 dB)		0.433FS
Input Range		±1 V, ±10 V
Input configuration		Differential, Pseudo-differential
Input impedance	Between positive input and system ground	1 MΩ
	Between negative input and system ground	Differential Configuration: 1 MΩ Pseudo-differential Configuration: 50 Ω
Input coupling		AC, DC (software selectable)
AC coupling cutoff frequency (-3 dB)		0.3 Hz
Integrated Electronic Piezoelectric (IEPE)		Current: 4 mA for each channel IEPE compliance: 24 V
Overvoltage protection	Differential	± 42.4V
	Pseudo-differential	Positive terminal: ± 42.4V Negative terminal: Not protected, rated at ± 2.5V
Offset error		± 0.2 mV max
Gain error		± 0.05% max
System Noise		40 μVrms (f_s = 256 kS/s)
SNR	±1 V Input Range	91 dB (f_s = 256 kS/s)
	±10 V Input Range	93 dB (f_s = 256 kS/s)
THD	±1 V Input Range	-118 dB (f_s = 256 kS/s)
	±10 V Input Range	-113 dB (f_s = 256 kS/s)
Dynamic range	±1 V Input Range	104 dB (f_s = 256 kS/s)
	±10 V Input Range	105 dB (f_s = 256 kS/s)
Crosstalk		-105 dB

3.2 Timebase

Timebase	
Delay trigger timebase	125 MHz
Sample clock timebase	Internal: Onboard synthesizer (10 MHz) External: PXIe backplane 10 MHz

3.3 Triggers

Trigger	
Trigger source	Software trigger, Analog trigger, External digital trigger, PXI STAR trigger, PXI trigger bus [0..7]
Trigger mode	Post trigger, Delay trigger
External digital trigger	5 V TTL compatibility Trigger polarity: Rising edge, Falling edge Pulse width : 20 ns minimum

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3.4 General Specifications

General Specifications	
I/O Connector	SMB x 8 for analog inputs SMB x 1 for external digital input
Dimensions	160 (W) x 100 (H) mm (6.24” x 3.9”) (not including connectors)
Ambient Temperature	Operation: 0°C to 55°C (32˚F to 131˚F) Storage: -20°C to 80°C (-4˚F to 176˚F)
Relative Humidity	10% to 90%, non-condensing
Certifications	EMC/EMI : CE, FCC Class A

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4 Mechanical Layout

NOTE: All dimensions shown are in millimeters.

4.1 Device Layout

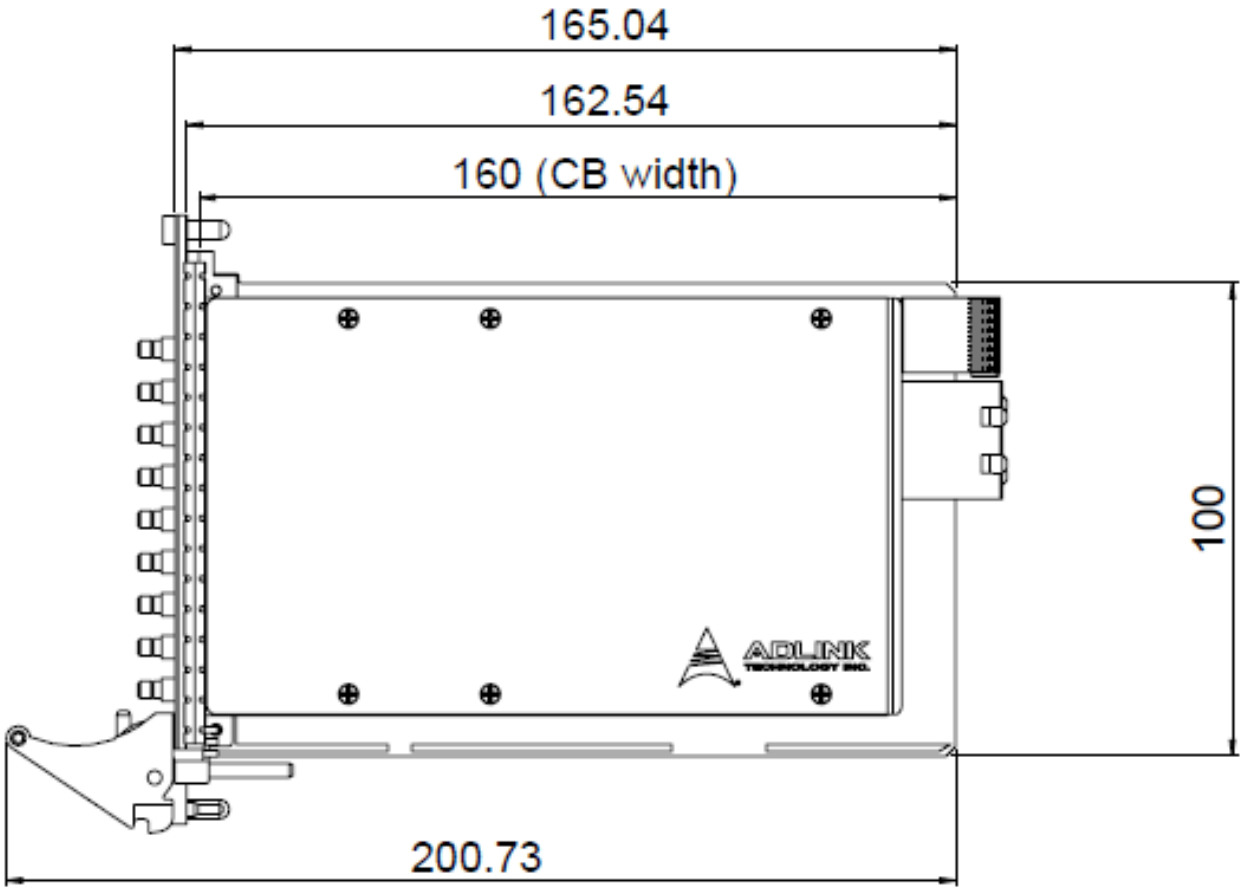


Figure 1: PXIe-9529H schematic

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4.2 I/O Array

The PXIe-9529H I/O array is labeled to indicate connectivity, as shown below.

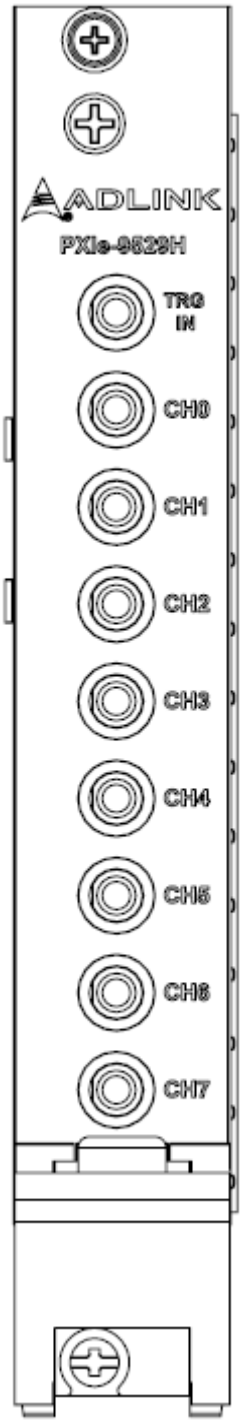


Figure 2: PCIe-9529H I/O array

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5 Operations

This chapter contains information regarding analog input, triggering, and timing for the PXIe-9529H.

5.1 Functional Block Diagram

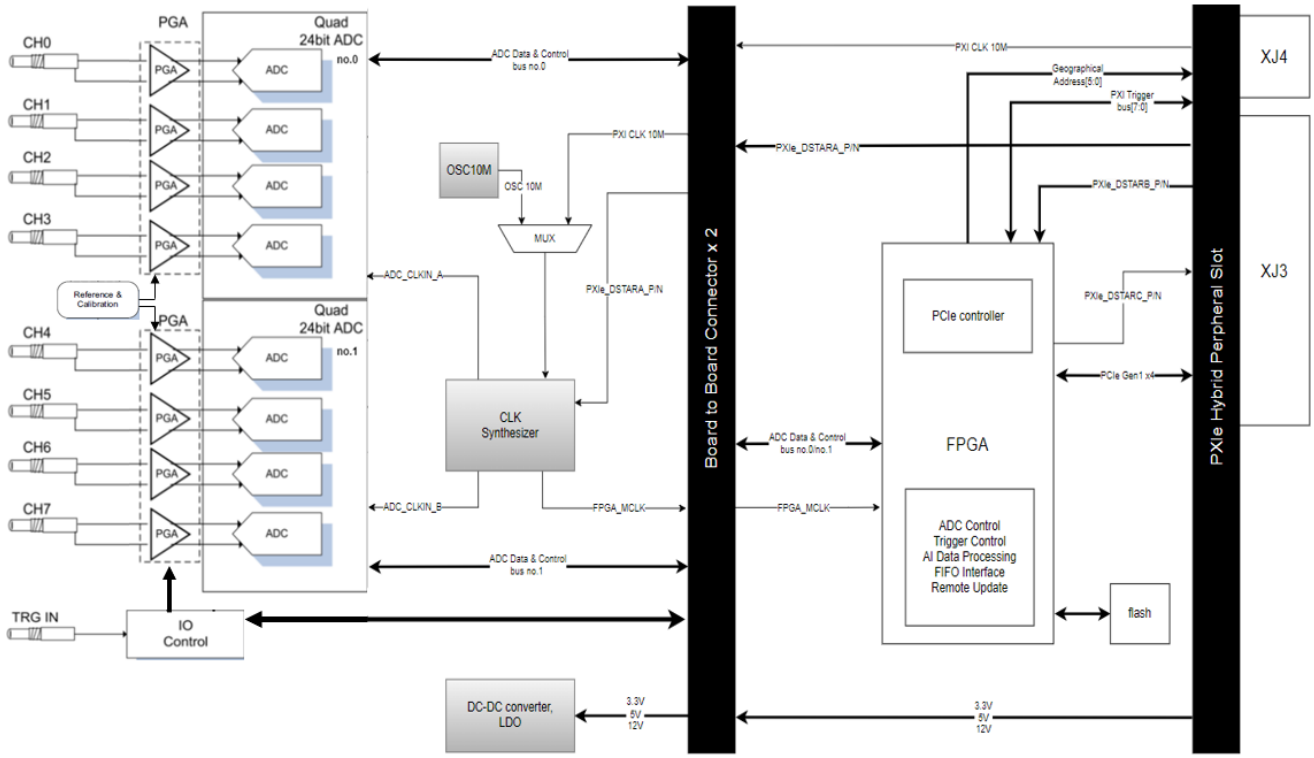


Figure 3: Functional block diagram

5.2 Analog Input Chanel

5.2.1 Analog Input Front-End Configuration

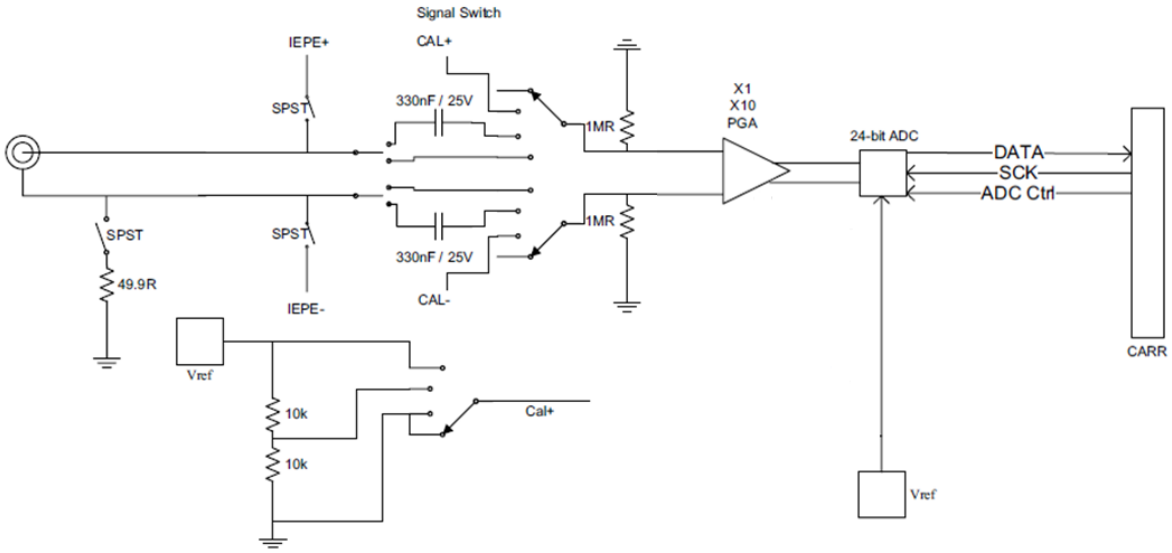


Figure 4: Analog input architecture

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Differential and Pseudo-Differential Input Configuration

The PXIe-9529H provides both differential and pseudo-differential input configurations, with differential input mode providing voltage to the anode and cathode inputs of the SMB connector according to the signal voltage difference between them. If the signal source is ground-referenced, differential input mode can be used for common-mode noise rejection. If the signal source is a floating signal, pseudo-differential input mode can provide a reference ground connected to the cathode input of the SMB through a 50 Ω resistor, preventing the floating source from drifting over the input common-mode range.

Recommended configurations for the signal sources are as follows.

Signal Source Type	Card Configuration
Floating	Pseudo Differential
Ground-Reference	Differential

AC and DC Input Coupling

AC and DC coupling are available. With DC coupling, the DC offset present in the input signal is passed to ADC, and is indicated if the signal source has a small level of offset voltage or if the DC content of the signal is important. In AC coupling, the DC offset present in the input signal is erased, and is indicated if the DC content of the input signals is to be rejected. AC coupling enables a high-pass R-C filter through the input signal path. The corner frequency (-3dB) is about 0.3Hz.

Input for IEPE

For applications that require sensors such as accelerometers or microphones, the PXIe-9529H provides an excitation current source. The common excitation current is usually about 4mA for these IEPE sensors. A DC voltage offset is generated due to the excitation current and sensor impedance. When IEPE current sources are enabled, the PXIe-9529H automatically sets input configuration to AC coupling.

5.2.2 Input Range and Data Format

Table 1: Input range and data format

Description	Full-scale range	Least significant bit	FSE-1LB	-FSR
Bipolar Analog Input	±10 V	1.19 µV	9.99999881 V	-10 V
	±1 V	0.119 µV	0.999999881V	-1 V
Digital Code	N/A	N/A	7FFFFF	800000

Table 2: Input range midscale values

Description	Midscale +1LSB	Midscale	Midscale-1LB
Bipolar Analog Input	1.19 µV	0V	-1.19 µV
	0.119 µV	0V	-0.119 µV
Digital Code	000001	000000	-FFFFFF

5.2.3 DMA Data Transfer

The PXIe-9529H, as a PCI Express Gen1 X 4 device, provides a 256 kS/s sampling rate ADC, generating an 8.192 MByte/second rate. To provide efficient data transfer, a PCI bus-mastering DMA is essential for continuous data streaming, as it helps to achieve the full potential PCI Express bus bandwidth. The bus-mastering controller releases the burden on the host CPU since data is directly transferred to the host memory without intervention. Once the analog input operation begins, the DMA returns control of the program. During DMA transfer, the hardware temporarily stores acquired data in the onboard AD Data FIFO, and then transfers the data to a user-defined DMA buffer in the computer.

Using a high-level programming library for high-speed DMA data acquisition, the sampling period and the number of conversions need simply to be assigned into specified counters. After the AD trigger condition is met, the data will be transferred to the system memory by the bus-mastering DMA. In a multi-user or multi-tasking OS, such as Microsoft Windows, Linux, or others, it is difficult to allocate a large continuous memory block.

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Therefore, the bus controller provides DMA transfer with a scatter-gather function to link non-contiguous memory blocks into a linked list to enable the transfer of large amounts of data without memory limitations. In non-scatter-gather mode, the maximum DMA data transfer size is 2 MB double words (8 MB bytes); in scatter-gather mode, there is no limitation on DMA data transfer size except the physical storage capacity of the system. Users can also link descriptor nodes circularly to achieve a multibuffered DMA. A linked list comprising three DMA descriptors.

Each descriptor contains a PCI address, a PCI dual address, a transfer size, and the pointer to the next descriptor. PCI address and PCI dual address support 64-bit addresses which can be mapped into more than 4 GB of address space, as shown.

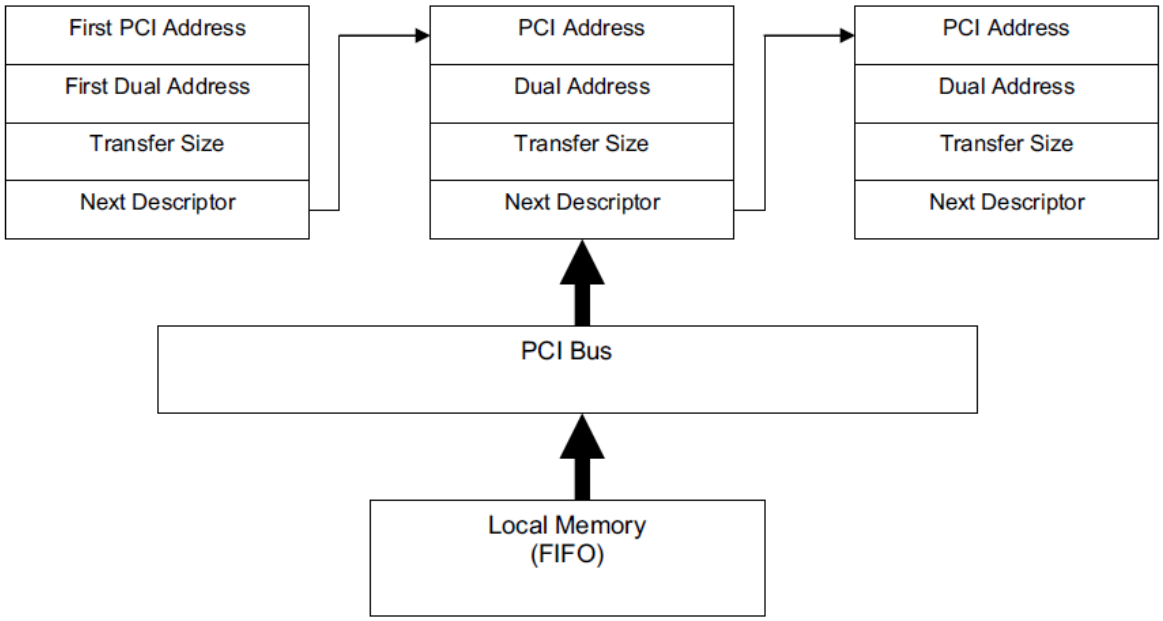


Figure 5: Linked list of PCI address DMA descriptors

5.3 Trigger Source and Trigger Modes

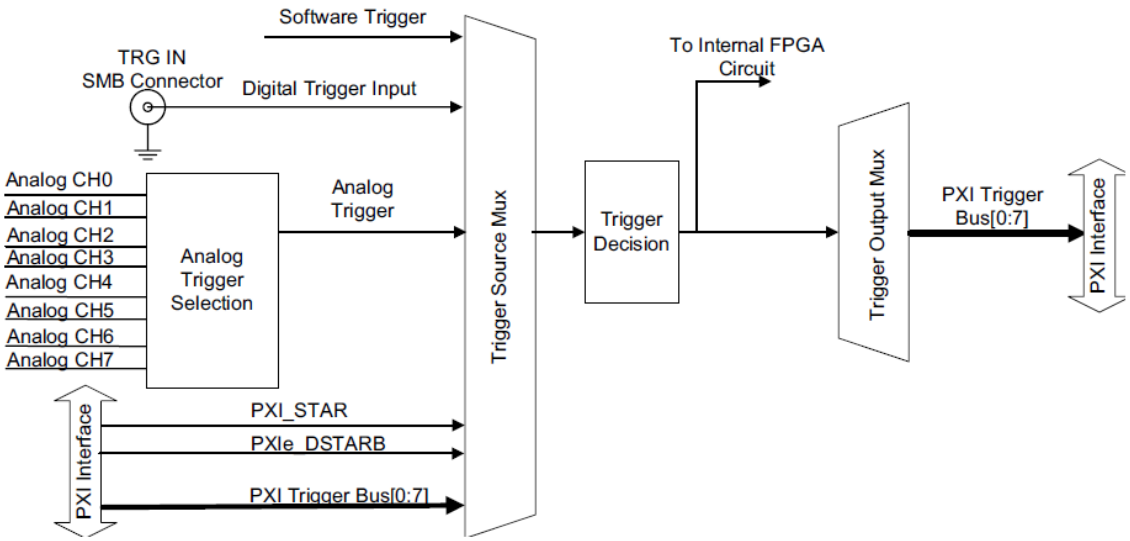


Figure 6: Trigger architecture

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The PXIe-9529H requires a trigger to implement acquisition of data. Configuration of triggers requires identification of trigger source. The PXIe-9529H supports an internal software trigger, external digital trigger, PXI_STAR trigger, PXIe_DSTARB, PXI Trigger Bus [0.7], and SSI bus as well as the analog trigger.

Software Trigger

The software trigger, generated by the software command, is asserted immediately following the execution of specified function calls to begin the operation.

External Digital Trigger

An external digital trigger is generated when a TTL rising edge or a falling edge is detected at the SMB connector on the front panel. As shown, trigger polarity can be selected by software. Note that the signal level of the external digital trigger signal should be TTL compatible, with a minimum pulse width of 10ns.

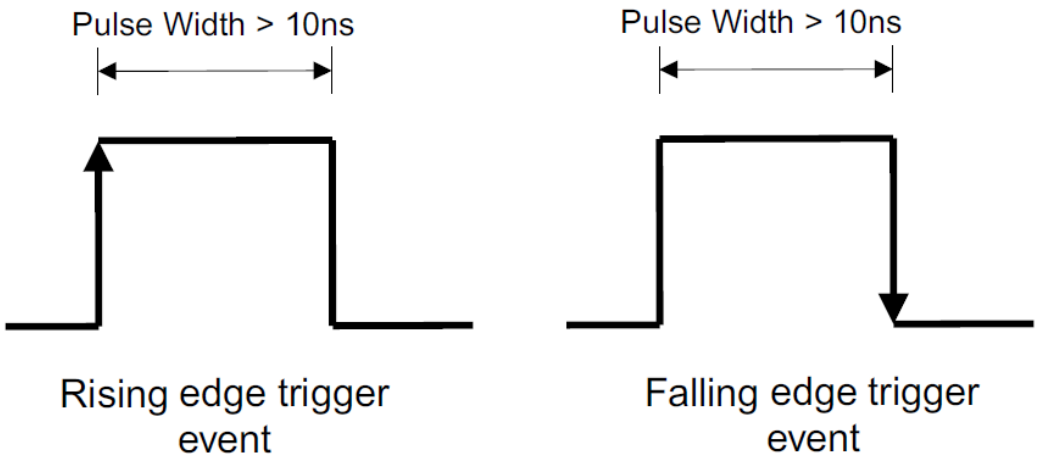


Figure 7: External digital trigger

PXI STAR Trigger

When PXI STAR is selected as the trigger source, the PXIe-9529H accepts a TTL-compatible digital signal as a trigger signal. The trigger occurs when a rising edge or falling edge is detected at PXI STAR, with trigger polarity configurable by software, with a minimum pulse width requirement of the digital trigger signal of 300ns.

PXIe_DSTARB Trigger

The PXIe_DSTARB signal, a differential signal transmitted via the PXI Express Chassis backplane, distributes high-speed, high-quality trigger signals. When PXIe_DSTARB is selected as the trigger source, the PXIe-9529H accepts a fast-switching LVDS digital signal as a trigger signal. Triggering occurs when a rising edge or falling edge is detected at PXIe_DSTARB, with trigger polarity configurable by software, with a minimum pulse width requirement 300ns.

PXI Trigger Bus

The PXIe-9529H utilizes PXI Trigger Bus Numbers 0 through 7 to act as a System Synchronization Interface (SSI). With the interconnected bus provided by the PXI Trigger Bus, multiple modules are easily synced. When configured as input, the PXIe-9529H serves as a slave module and can accept trigger signals from one of the buses 0 through 7. When configured as output, the PXIe-9529H serves as a master module and can output trigger signals to the PXI Trigger Bus Numbers 0 through 7.

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Analog Trigger

The PXIe-9529H analog trigger circuitry can be configured to monitor one analog input channel from which data is acquired. The selection of an analog input channel as the analog trigger channel does not influence the input channel acquisition operation. The analog trigger circuit generates an internal digital trigger signal based on the condition between the analog signal and the defined trigger level.

Analog trigger conditions are as follows:

- Positive-slope trigger: The trigger event occurs when the analog input signal changes from a voltage lower than the specified trigger level to a voltage exceeding the specified trigger level.
- Negative-slope trigger: The trigger event occurs when the analog input signal changes from a voltage exceeding the specified trigger level to a voltage lower than the specified trigger level.

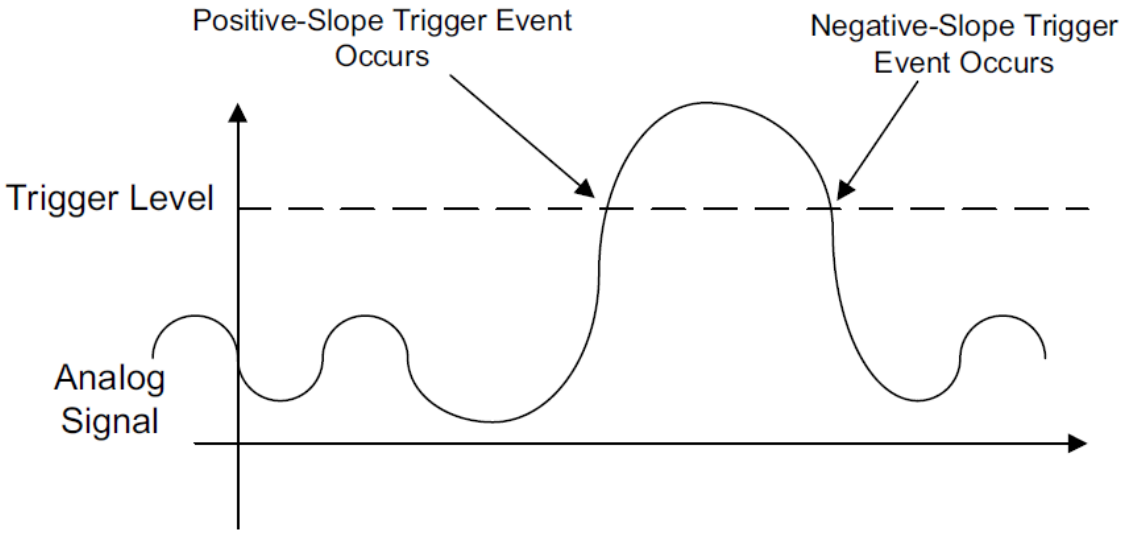


Figure 8: Analog trigger conditions

The trigger signal can be chosen from among CH0, CH1, CH2, CH3, CH4, CH5, CH6, and CH7 during the use of an external analog trigger source. The trigger level can be set by software with 24-bit resolution, with characteristics as shown.

Table 3: Preferred characteristics for analog triggers

Trigger Level Setting (Hex)	Trigger Voltage (-10V to +10V Range)	Trigger Voltage (-1V to +1V Range)
7FFFFF	9.99999881 V	0.999999881 V
7FFFFE	9.99999762 V	0.999999762 V
1	1.19 µV	0.119 µV
0	0V	OV
FFFFFF	-1.19 µV	-0.119 µV
800001	-9.99999881 V	-0.999999881 V
800000	-10 V	-1 V

Trigger Export

The PXIe-9529H can export trigger signals to PXI Trigger Bus Numbers 0 through 7, utilizing them to act as the System Synchronization Interface. When configured as the output, the PXIe-9529H serves as a master module and can output trigger signals to synchronize the slave modules, with the trigger signal routed to any of the seven PXI Trigger Bus Numbers via software.

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5.4 Trigger Mode

Two trigger modes applied to trigger sources initiate different data acquisition timings when a trigger event occurs, as applied to analog input and output functions.

Post Trigger Mode

If post-trigger mode is configured, activity commences once the following trigger conditions are met:

- The analog input channel acquires a programmed number of samples at a specified sampling rate.
- The analog output channel outputs pre-defined voltage at a specified output rate.

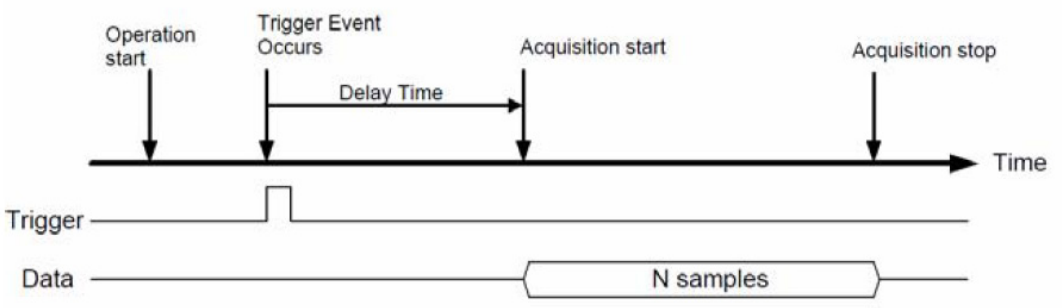


Figure 9: Post-trigger acquisition

Delay Trigger Mode

If delay trigger mode is configured, the delay time from when the trigger event asserts to the beginning of the acquisition and waveform generation can be specified, as shown. The delay time is specified by a 32-bit counter value with the counter clocking based on the PCIe clock. Accordingly, the maximum delay time is the period of PCIe_CLK X (2^32 - 1) and the minimum is the period of PCIe_CLK (8 ns).

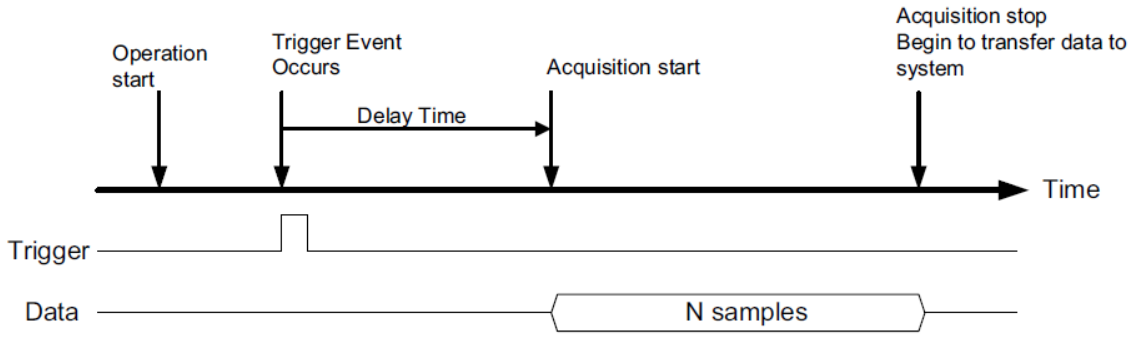


Figure 10: Delay trigger mode acquisition

Post-Trigger or Delay-Trigger Acquisition with Re-Trigger

Post-trigger or delay trigger acquisition with re-trigger function enables collection of data after several trigger events, as shown. When the number of triggers is defined, the PXIe-9529H acquires specific sample data each time a trigger is accepted. All sampled data is stored in onboard memory first until all trigger events have occurred, such that the time between the previous sampled data and the subsequent trigger event can be only one clock period of PCIe CLK. After the initial setup, no additional software intervention is required.

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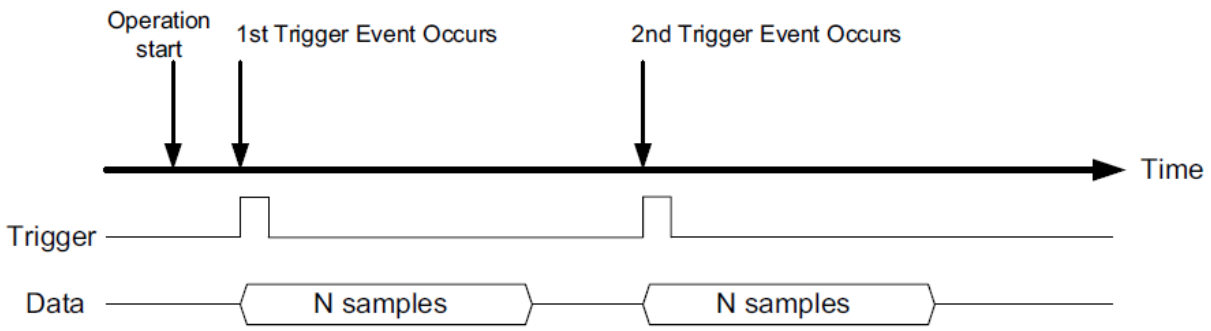


Figure 11: Re-trigger mode acquisition

5.5 ADC Timing Control

5.5.1 Timebase

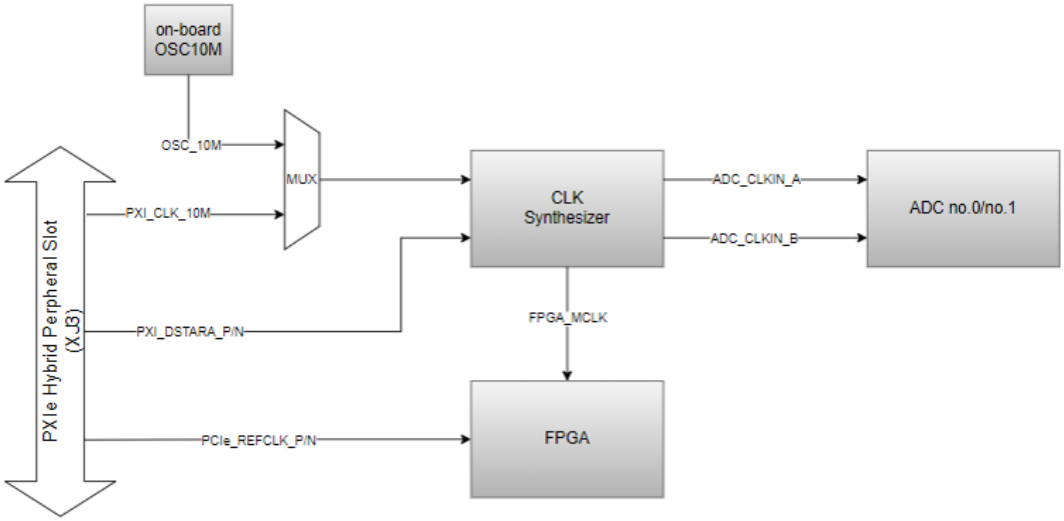


Figure 12: Timebase architecture

An onboard timebase clock drives the sigma-delta ADC, with a frequency exceeding the sample rate and produced by a PLL chip, with output frequency programmable to superior resolution. The PXIe- 9529H accepts the external 10MHz and 100MHz clocks from the PXI Express backplane for improved synchronization between modules.

5.6 Synchronizing Multiple Modules

The SSI (System Synchronization Interface) provides DAQ timing synchronization between multiple cards, with a bidirectional SSI I/O providing a flexible connection between cards and allowing a single SSI master to output the signal to other slave modules. SSI signals are designed for card synchronization only, not external devices. In the PXI Express form factor, the PXI trigger bus built on the PXI Express backplane provides the necessary timing signal connections. All SSI signals are routed to the XJ4 connector, with no requirement for additional cabling. The eight interconnected lines on the PXI Express backplane, labeled PXI Trigger Bus[0:7] provide a flexible interface for syncing multiple modules.

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Table 4: Configuration for synchronizing multiple modules

Module	Trigger source	Trigger out to PXI backplane	Timebase
Master	External Trigger	PXI Trigger Bus	PXI backplane 10MHz
		PXI Star Trigger	
	Software Trigger	PXI Trigger Bus	
		PXI Star Trigger	
Slave [1..n]	PXI Trigger Bus	N/A	PXI backplane 10MHz
	PXI Star Trigger	N/A	

The PXIe-9529H utilizes the PXI Trigger Bus [0:7] as a System Synchronization Interface (SSI). Flexible routing of trigger signals onto the PXI Trigger Bus enables the PXIe-9529H to simplify synchronization between multiple modules. SSI timing signals and functions are as shown, as is the SSI architecture.

Table 5: SSI timing signal definitions

SSI Timing Signal	Functionality
SSI_AD_TRIG	SSI master: issues internal AD_TRIG SSI slave: accepts SSI_AD_TRIG as the digital trigger signal.



Different signals cannot be routed onto the same trigger bus line.

The internal timing signals can be routed to the PXI trigger bus through software drivers. Physically, signal routing is accomplished in the FPGA, with cards connected through the PXI trigger bus achieving synchronization on the timing signal.

5.6.1 SSI_TRIG

As output, the SSI_TRIG signal reflects the trigger event signal in an acquisition sequence. As input, the PXIe-9529H accepts the SSI_TRIG signal as the trigger event source. The signal is configured in the rising edge-detection mode, with minimum pulse width of 8ns.

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6 Appendix A Calibration

This chapter introduces the calibration process to minimize analog input measurement errors.

6.1 Calibration Constant

The PXIe-9529H is factory-calibrated before shipment, with associated calibration constants written to the onboard EEPROM. At system boot, the PXIe-9529H driver loads these calibration constants, such that analog input path errors are minimized. ADLINK provides a software API for calibrating the PXIe-9529H.

The onboard EEPROM provides two banks for calibration constant storage. Bank 0, the default bank, records the factory-calibrated constants, providing written protection and preventing erroneous auto-calibration. Bank 1 is a user-defined space, provided for the storage of self-calibration constants. Upon execution of auto-calibration, the calibration constants are recorded to Bank 1.

When PXIe-9529H boots, the driver accesses the calibration constants and is automatically set to hardware. In the absence of user assignment, the driver loads constants stored in bank 0. If constants from Bank 1 are to be loaded, the preferred bank can be designated as a boot bank by software. Following the re-assignment of the bank, the driver will load the desired constants on the system reboot. This setting is recorded to EEPROM and is retained until reconfiguration.

6.2 Auto-Calibration

Errors in measurements and outputs will vary with time and temperature, recalibration is recommended when the module is installed. Auto-calibration can measure and minimize errors without external signal connections, reference voltages, or measurement devices.

The PXIe-9529H has an onboard calibration reference to ensure the accuracy of auto-calibration. The reference voltage is measured on the production line and recorded in the onboard EEPROM.

Before initializing auto-calibration, it is recommended to warm up the PXIe-9529H for at least 20 minutes and remove connected cables.



It is not necessary to manually factor delay into applications, as the PXIe-9529H driver automatically adds the compensation time.

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Safety Instructions

For user safety, please read and follow all instructions, Warnings, Cautions, and Notes marked in this manual and on the associated device before handling/operating the device, to avoid injury or damage.

S'il vous plaît prêter attention stricte à tous les avertissements et mises en garde figurant sur l'appareil , pour éviter des blessures ou des dommages.

- Read these safety instructions carefully.
- Keep the User's Manual for future reference.
- Read the Specifications section of this manual for detailed information on the recommended operating environment.
- The device can be operated at an ambient temperature of 50ºC.
- When installing/mounting or uninstalling/removing device; or when removal of a chassis cover is required for user servicing (See "Getting Started" on page 9.):
  - Turn off power and unplug any power cords/cables.
  - Reinstall all chassis covers before restoring power.
- To avoid electrical shock and/or damage to device:
  - Keep device away from water or liquid sources.
  - Keep device away from high heat or humidity.
  - Keep device properly ventilated (do not block or cover ventilation openings).
  - Always use recommended voltage and power source settings.
  - Always install and operate device near an easily accessible electrical outlet.
  - Secure the power cord (do not place any object on/over the power cord).
  - Only install/attach and operate device on stable surfaces and/or recommended mountings.
- If the device will not be used for long periods of time, turn off and unplug from its power source.
- Never attempt to repair the device, which should only be serviced by qualified technical personnel using suitable tools.
- A Lithium-type battery may be provided for uninterrupted backup or emergency power.



Risk of explosion if battery is replaced with one of an incorrect type; please dispose of used batteries appropriately.

Risque d'explosion si la pile est remplacée par une autre de type incorrect. Veuillez jeter les piles usagées de façon appropriée.

- The device must be serviced by authorized technicians when:
  - The power cord or plug is damaged.
  - Liquid has entered the device interior.
  - The device has been exposed to high humidity and/or moisture.
  - The device is not functioning or does not function according to the User's Manual.
  - The device has been dropped and/or damaged and/or shows obvious signs of breakage.
- Disconnect the power supply cord before loosening the thumbscrews and always fasten the thumbscrews with a screwdriver before starting the system up.
- It is recommended that the device be installed only in a server room or computer room where access is:
  - Restricted to qualified service personnel or users familiar with restrictions applied to the location, reasons therefore, and any precautions required.

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- Only afforded by the use of a tool or lock and key, or other means of security, and controlled by the authority responsible for the location.

- If PoE (Power over Ethernet) is enabled for the device, the system can ONLY be deployed indoors. Unless otherwise noted, the PoE system is NOT designed to withstand the rigors of outdoor use.

	**BURN HAZARD** Touching this surface could result in bodily injury. To reduce risk, allow the surface to cool before touching. ***RISQUE DE BRÛLURES*** *Ne touchez pas cette surface, cela pourrait entraîner des blessures.*

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