PXIe-9834

4CH 16-bit 80MS/s PXIe Digitizer

User's Manual



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Part No: 50-17057-1000

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Revision History

Revision	Release Date	Description of Change(s)
1.0	September 12, 2019	Initial release

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Preface

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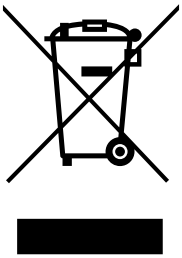
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Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.


NOTE:

Additional information, aids, and tips that help users perform tasks.


CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.


WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

The ADLINK PXIe-9834 PXI Express digitizer delivers high speed, high quality data acquisition, with each of four input channels supporting up to 80MS/s sampling with 16-bit resolution A/D converter. This provides simultaneous recording of signals on all channels with no inter-channel phase delay, and the extremely large onboard memory enables long recording times even at the highest sampling rates.

The PXIe-9834 features flexible input, ±10V (only for 1MΩ), ±5V, ±1V and ±0.5V along with software selectable 50Ω or 1MΩ input impedance. Four high resolution 16-bit A/D converters combined with low-noise, high bandwidth analog front-end enable highly accurate signal acquisition. Providing extremely large onboard memory, the PCI Express 4 lane interface supports data streaming even at the highest sampling rates. The PXIe-9834 is also auto-calibrated with an onboard reference circuit compensating the offset and gain error of acquired analog input signals.

The PXIe-9834 is, accordingly, ideal for applications such as radar signal acquisition, fiber optic detection, and many others.

1.1 Features

- Up to 80MS/s sampling
- 4 simultaneous analog inputs
- High resolution 16-bit ADC
- Up to 40 MHz bandwidth for analog input
- 1GB onboard storage
- Programmable input voltage of ±0.5V, ±1V, ±5V, or ±10V
- 10 or 20MHz onboard digital filter
- Support for external sampling clock (20MHz to 80MHz) or external reference clock (10MHz)
- Scatter-Gather DMA data transfer for high speed data streaming
- PXI/PXIe instrumentation signals supported for triggers and timebase
- Full auto-calibration

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1.2 Applications

- Testing/monitoring for Energy Management applications, including:
  - Partial discharge
  - Power line/device monitoring
- Non-destructive testing
- Radar acquisition
- LiDAR

1.3 Specifications

1.3.1 Analog Input

Item	Specification	Comment
Channels	4 single-ended	
Connector type	SMA	
Input coupling	DC or AC, software selectable	
ADC resolution	16-Bit	
Input range	±0.5 V, ±1 V, ± 5V, or ± 10V	±10V range support only for 1MΩ input impedance
Bandwidth (-3dB)	40MHz	
Maximum input overload	7Vrms	For 50Ω: ±0.5V or ±1V or ± 5V input range
	±10V	For 1MΩ: ±0.5V or ±1V
	±30V	For 1MΩ: ±5V or ±10V
Input impedance	50Ω or 1MΩ, software selectable	
Digital filter	10MHz or 20MHz, software selectable	

Table 1-1: Analog Input Channel Characteristics

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1.3.2 Accuracy

Input Range	Offset Error		Gain Error
	50Ω Input Impedance	1MΩ Input Impedance	
±0.5V	±0.8mV	±0.8mV	±0.6%
±1V	±0.8mV	±1.2mV	
±5V	±1.5mV	±4.0mV	
±10V	N/A	±8mV	

Table 1-2: Accuracy

1.3.3 System Noise

Input Range	System Noise
±0.5V	$0.1mV_{rms}$
±1V	$0.15mV_{rms}$
±5V	$1mV_{rms}$
±10V	$1.5mV_{rms}$

Table 1-3: System Noise

1.3.4 Crosstalk, DC to 10MHz

Input Range	Crosstalk	Comment
±0.5V	<-80dB	1MHz sine wave, 90% of full scale range
±1V, ±5V, ±10V	<-90dB	1MHz sine wave, 90% of full scale range

Table 1-4: Crosstalk, DC to 10MHz

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1.3.5 Spectral Characteristics

Index	Specification	Comment
SINAD	68dB	±0.5V, ±1V, ±5V
	65dB	±10V
THD	-78dB	For all ranges
SFDR	78dB	For all ranges
SNR	69dB	±0.5V, ±1V, ±5V
	65dB	±10V

NOTE: Values reflect 50Ω and 1MΩ input impedance with digital filter off.

Table 1-5: Spectral Characteristics

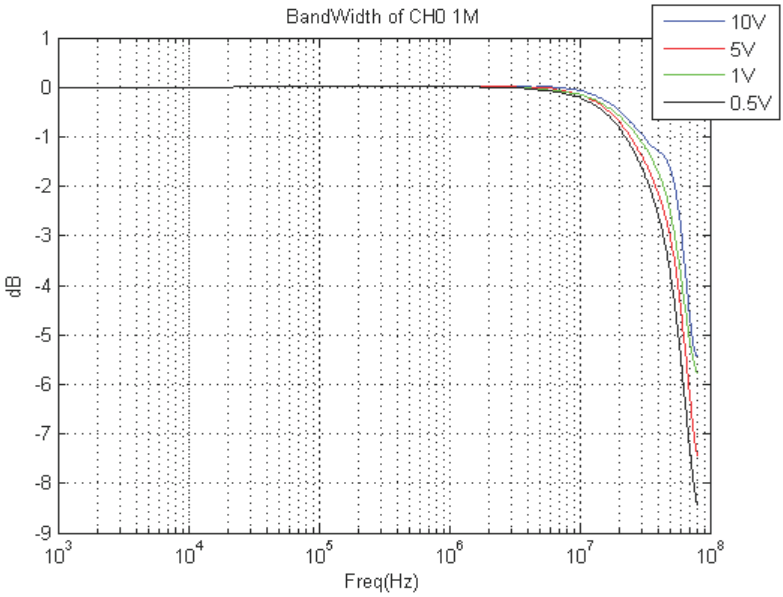


Figure 1-1: Typical Frequency Response, 1MΩ input impedance

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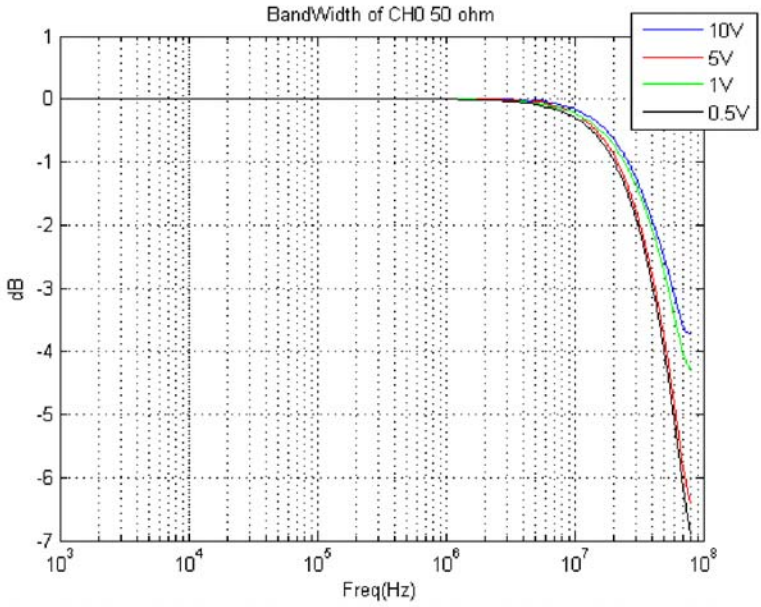


Figure 1-2: Typical Frequency Response, 50Ω input impedance

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1.3.6 Timebase

Sample Clock	Detail	Comment
Timebase options	Internal: Onboard oscillator	
	External: CLK IN (front panel SMA connector)	
	External reference clock: ▶ CLK IN (front panel SMA connector) ▶ PXI_10M (PXIe backplane 10MHz reference clock)	The reference clock supplies an onboard PLL circuit and generates 80MHz for ADC.
Sampling clock frequency	Internal 80MS/s maximum, ranges from 1.22KS/s to 80MS/s	1.22kS/s to 80MS/s
	External sample clock: 20MHz to 80MHz (through CLK IN)	
	External reference clock: 10MHz	
Internal onboard oscillator accuracy	< ± 25ppm	

Table 1-6: Timebase Specifications

External Sample Clock	Specification
Clock input range	$0.45V_{pp}$ to $5V_{pp}$
Clock input coupling	AC
Clock input impedance	50Ω
Duty cycle tolerance	45% to 55%

Table 1-7: External Sample Clock

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External Reference Clock	Specification
Clock input range	$0.45V_{pp}$ to $5V_{pp}$
Clock input coupling	AC
Clock input impedance	50Ω
Duty cycle tolerance	45% to 55%
Reference clock frequency range	10MHz ± 2KHz

Table 1-8: External Reference Clock

1.3.7 Triggers

Trigger Source & Mode	
Trigger source	Internal: software trigger
	External: ▶ External digital trigger from TRG IN (front panel) ▶ Analog trigger from any of analog input channels ▶ PXI Trigger Bus[0..7] ▶ PXI STAR Trigger ▶ PXIe_DSTARB
Trigger modes	▶ Post-trigger ▶ Delay trigger ▶ Pre-trigger ▶ Middle trigger ▶ Re-trigger for post-trigger and delay trigger modes

Table 1-9: Triggers

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External Digital Trigger Input	
Sources	TRG IN, front panel SMA connector
Compatibility	3.3 V TTL, 5 V tolerant
Input high threshold (VIH)	2.0 V
Input low threshold (VIL)	0.8 V
Maximum input overload	-0.5 V to +5.5 V
Trigger polarity	Rising or falling, software selectable
Trigger pulse width	20 ns minimum

Table 1-10: External Digital Trigger Input

Onboard Reference (Calibration)	
Calibration	**Specification**
Onboard reference	+1.8V, +0.9V, +0.45V
Temperature coefficient	5.0 ppm/°C
Warm-up time	15 minutes (recommended)

Table 1-11: Onboard Reference (Calibration)

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1.3.8 Mechanical and Environmental

Item	Specification	Comment
Dimensions	165mm (W) x 100mm (H) (PCB)	3U, one-slot, PXI Express module
Bus Interface	PCI Express x4 Gen1	
Operating Conditions	Temperature: 0°C to 50°C Relative humidity: 5% to 95%, non-condensing	
Storage Conditions	Temperature: -20°C to 80°C Relative humidity: 5% to 95%, non-condensing	
Compliance & Certification	▶ EN 55032: 2015 / AC: 2016, Class B ▶ EN 55024 (2010 + A1: 2015): Immunity ▶ EN61326-1/2: Class B ▶ FCC 47 CFR Part 15B: Class B ▶ ICES-003 Issue 6-2016: Class B ▶ ANSI C63.4-2014: Class B	

Table 1-12: Specifications

1.3.9 Power Consumption

Power Rail	Standby	Maximum
+3.3V	18 mA	70 mA
+12V	450 mA	753 mA
Total Power	5.46W	9.28W

Table 1-13: Power Consumption

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1.4 Software Support

ADLINK provides versatile software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW. All software options are included in the ADLINK All-in-One CD. Commercial software drivers are protected with licensing codes. Without the code, you may install and run the demo version for trial/demonstration purposes for only up to two hours. Contact your ADLINK dealer to purchase the software license. The ADLINK Measurement, Automation & Platform Service (MAPS) is a software service package designed for data acquisition, automation and PXI platform. By leveraging the sophisticated architecture in low-level kernel management and user friendly API, users can easily manage devices under a Windows environment and focus on developing applications.

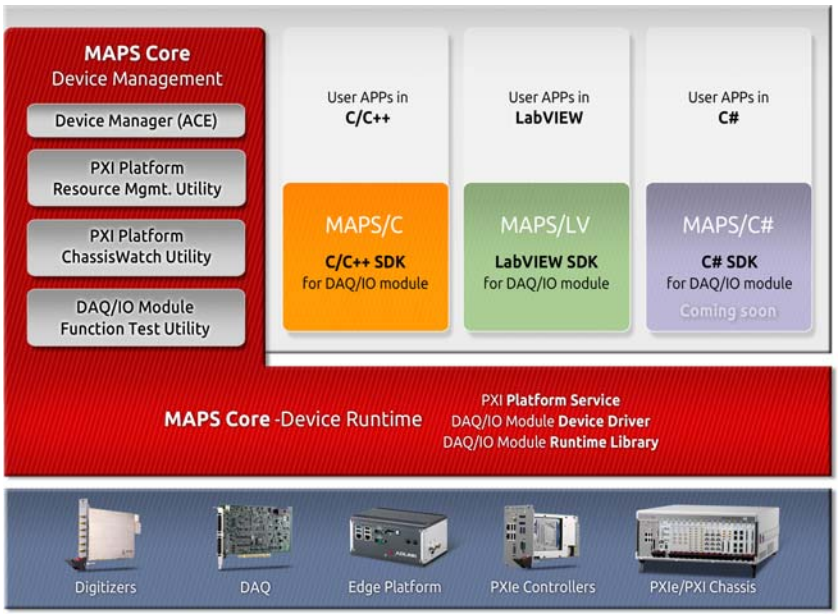


Figure 1-3: ADLINK Measurement, Automation & Platform Service (MAPS) Architecture

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1.4.1 MAPS Core

ADLINK MAPS Core is a software package that includes all the device drivers for Windows and a system level management tool called ACE (ADLINK Connection Explorer). With MAPS Core installed in a user-provided PC, the operating system can identify ADLINK's devices correctly and assign necessary resources for low-level access, such as IO read/write or direct memory access. MAPS/Core is necessary for all ADLINK DAQ modules. To ensure the user has the latest software, go to the ADLINK product web-page or contact ADLINK technical service.

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MAPS Core also comes with a system management portal called ADLINK Connection Explorer (ACE). Through ACE, users can discover and manage ADLINK DAQ modules. For example, the user can reserve a certain size of memory buffer for DMA operation or set the user alias name for operating the module in a LabVIEW environment.

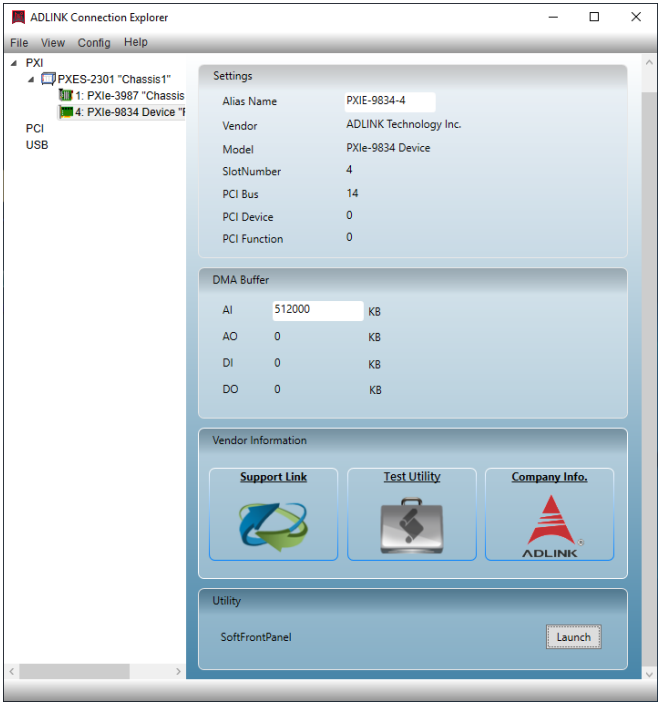


Figure 1-4: ADLINK Connection Explorer (ACE)

ADLINK Connection Explorer (ACE) also provides a ready-to-use soft-front panel for digitizer products. By clicking the Launch button in the lowest "Utility" block, this soft-front panel allows users to control digitizers through the UI and display the acquired waveform/data on the screen.

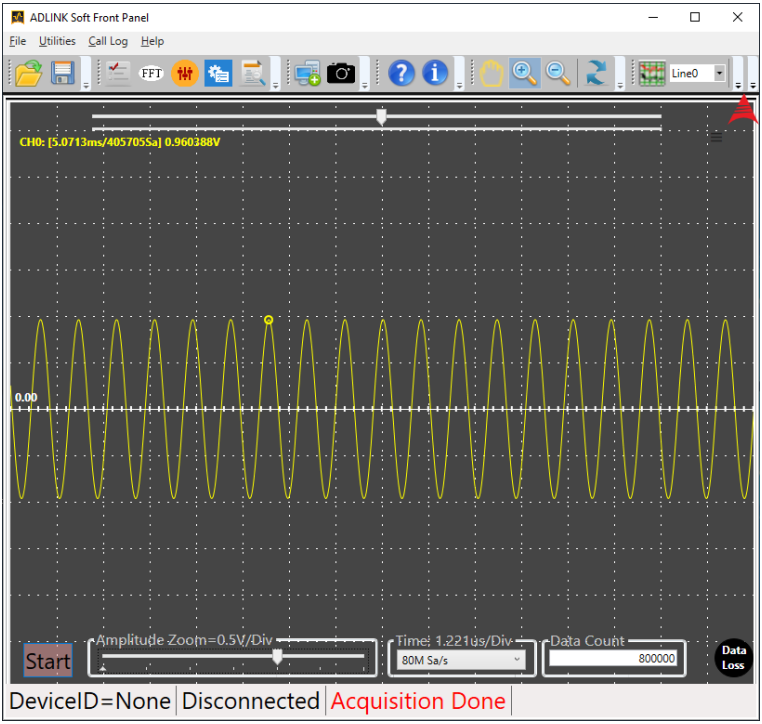


Figure 1-5: The ADLINK Connection Explorer (ACE) Soft Front Panel

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1.4.2 MAPS/LV, LabVIEW Support

For customers who develop their own programs in LabVIEW, please install the MAPS/LV software package. The MAPS/LV, also called DAQ-LabVIEW Plus, includes the software library and sample program for LabVIEW. Download and install the latest MAPS/LV software from the following website and refer to the MAPS/LV manual: https://www.adlinktech.com/Products/Data_Acquisition/DAQSoftware_Utility/MAPS_LV?Lang=en

1.4.3 MAPS/C, C & C++ Support

For customers who develop their own programs in C or C++ environments, install the MAPS/C software package. MAPS/C includes all the software components required for developing applications in C/C++, such as header files, device API library and versatile sample programs for understanding how to manipulate the device correctly. Find the latest MAPS/C on the ADLINK website.

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1.5 Device Layout and I/O Connectors

All dimensions are in mm.

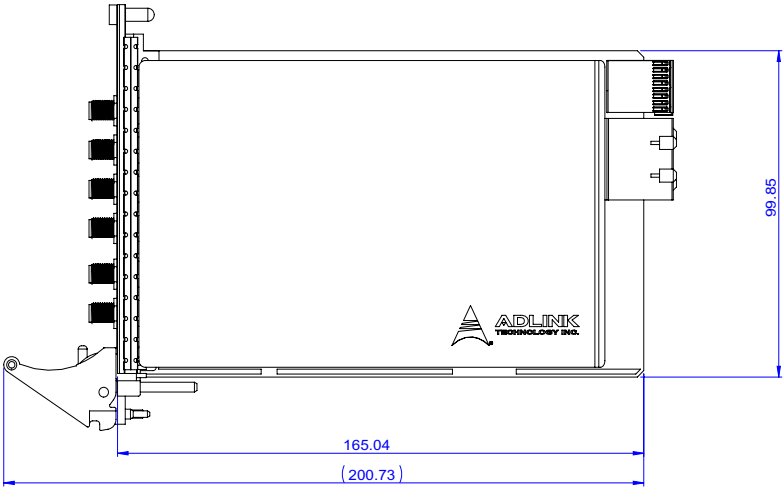


Figure 1-6: PXIe-9834 Dimensions

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The PXIe-9834 I/O array is labeled to indicate connectivity, as shown. All I/O connectors are SMA.

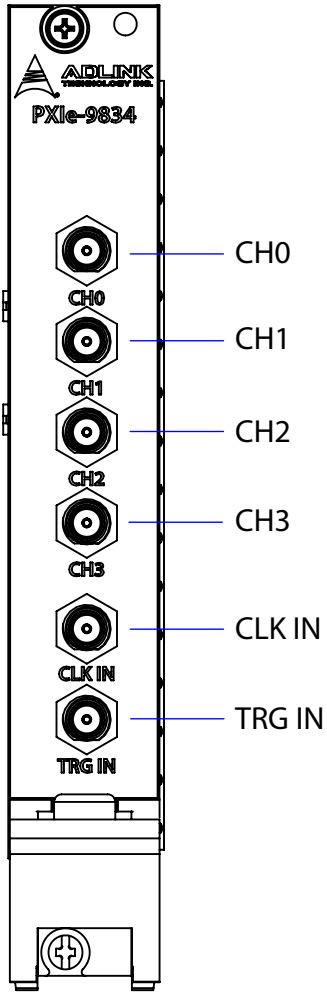


Figure 1-7: PXIe-9834 Front Panel

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Input	Faceplate Label	Comment
Analog	CH0	Analog Input Channel
Analog	CH1	
Analog	CH2	
Analog	CH3	
External sampling clock and reference clock	CLK IN	Input for external sampling clock or reference clock to the digitizer
External Digital Trigger	TRG IN	External digital trigger input, receiving trigger signal from external instrument, thus initiating acquisition

Table 1-14: PXIe-9834 I/O Array Legend

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2 Getting Started

This chapter describes proper installation environment, installation procedures, package contents and basic information users should be aware of regarding the PXIe-9834.



NOTE:

Diagrams and illustrated equipment are for reference only. Actual system configuration and specifications may vary.

2.1 Installation Environment

When unpacking and preparing to install, please refer to Important Safety Instructions.

Only install equipment in well-lit areas on flat, sturdy surfaces with access to basic tools such as flat- and cross-head screwdrivers, preferably with magnetic heads as screws and standoffs are small and easily misplaced.

Recommended Installation Tools:

- Phillips (cross-head) screwdriver
- Flat-head screwdriver
- Anti-static wrist strap
- Antistatic mat

The ADLINK PXIe-9834 is electrostatically sensitive and can be easily damaged by static electricity. The module must be handled on a grounded anti-static mat. The operator must wear an anti-static wristband, grounded at the same point as the anti-static mat.

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Inspect the carton and packaging for damage. Shipping and handling could cause damage to the equipment inside. Make sure that the equipment and its associated components have no damage before installation.



The equipment must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the equipment and wear a grounded wrist strap when servicing.

2.2 Package Contents

- PXIe-9834 digitizer
- PXIe-9834 Quick Start Guide

If any of these items are missing or damaged, contact the dealer.



Do not install or apply power to equipment that is damaged or missing components. Retain the shipping carton and packing materials for inspection. Please contact your ADLINK dealer/ vendor immediately for assistance and obtain authorization before returning any product.

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2.3 Installing the Module



The power cable provides grounding to prevent hazardous ESD (electrostatic discharge).



Do not to perform "hot swapping", replacement, disconnecting or connecting of any components (including cards and cabling) on chassis while the system is powered up. By not observing this Warning, system damage and/or data loss, and physical injury (due to possible shock hazard) may result.

1. Turn off the PXIe system/chassis and ensure the power cable from the power source is connected.
2. Align the module's edge with the module guide in the PXIe chassis.
3. Slide the module into the chassis until resistance is felt from the PXIe connector.
4. Push the ejector latch upwards and fully insert the module into the chassis.
5. Once the module is fully seated, a "click" can be heard from the ejector latch.
6. Tighten the screw on the faceplate.
7. Power up the PXIe system/chassis.

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3 Operations

This chapter contains information regarding analog input, triggering and timing for the PXIe-9834.

3.1 Functional Block Diagram

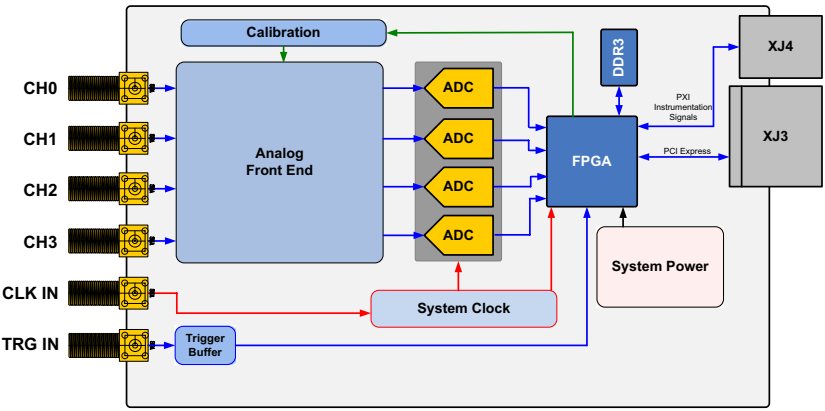


Figure 3-1: Functional Block Diagram

3.2 Analog Input Channel

3.2.1 Analog Input Front-End Configuration

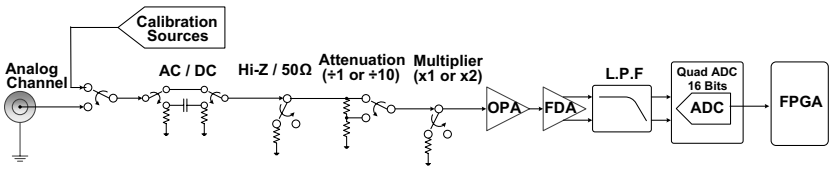


Figure 3-2: Analog Input Architecture

The PXIe-9834's 50Ω or 1MΩ input impedance circuit, along with AC/DC coupling, makes it easy to acquire a wide variety of signals. Sophisticated attenuation circuit design offers several

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input ranges with high noise-to-signal ratio and high spurious-free dynamic range in AC performance. Analog bandwidth up to 40MHz and two digital filters provide more options to filter out unwanted high frequency signals and lower incoming noise. The overall analog path design provides flexible configuration, acquiring high speed signals and restore them in digital data, with all designs applied to four analog input channels independently.

For auto-calibration, an elaborate onboard reference circuit provides stable and low drift voltage, of particular benefit whenever auto-calibration is executed in response to environmental temperature change. For more details about auto-calibration, please see “Calibration” on page 45.

3.2.2 Input Range and Data Format

Data format of the PXIe-9834 is 2’s complement.

D15	D14	D13	D12	...	D3	D2	D1	D0
D15 to D0 bits represent the 16-bit data from ADC (2’s complement)								

Table 3-1: Input Range and Data Format

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The following table shows the represented digital code when input voltage is at negative full scale and positive full scale. Since the data format for the PXIe-9834 is 2's complement, the most significant bit represents the sign of input voltage.

	Input Range	Least Significant Bit	FSR-1LSB	-FSR
Bipolar Analog Input	± 10.0V	0.305 mV	9.999694824	-10V
	± 5.0V	0.153 mV	4.999847412	-5V
	± 1.0V	0.031 mV	0.999969482	-1V
	± 0.5V	0.015 mV	0.499984741	-0.5V
Digital Code	N/A	N/A	7FFF	8000

Table 3-2: Input Range FSR and -FSR Values

The following table shows the digital code when input voltage is roughly midscale, approximately 0 V.

	Midscale +1LSB	Midscale	Midscale -1LSB
Bipolar Analog Input	0.305 mV	0 V	-0.305 mV
	0.153 mV	0 V	-0.153 mV
	0.031 mV	0 V	-0.031 mV
	0.015 mV	0 V	-0.015 mV
Digital Code	0001	0000	FFFF

Table 3-3: Input Range Midscale Values

In the PXIe chassis, a system timing slot distributes trigger signals through PXI_STAR and PXIe differential star triggers. The 8-bit parallel PXI Trigger bus provides additional channels to transmit and receive triggers between peripheral slots. The PXIe chassis further provides 10MHz (PXI_CLK10) clock options distributed to each peripheral slot with minimal clock skew.

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3.2.3 DMA Data Transfer

The PXIe-9834, a PXIe Gen 1 X 4 device, is equipped with four 80MS/s high sampling rate ADCs, generating a 640 MByte/second rate.

To provide efficient data transfer, a PCI bus-mastering DMA is essential for continuous data streaming, as it helps to achieve full potential PCI Express bus bandwidth. The bus-mastering controller releases the burden on the host CPU since data is directly transferred to the host memory without intervention. Once analog input operation begins, the DMA returns control of the program. During DMA transfer, the hardware temporarily stores acquired data in the onboard AD Data FIFO, and then transfers the data to a user-defined DMA buffer in the computer.

Using a high-level programming library for high speed DMA data acquisition, the sampling period and the number of conversions needs simply to be assigned into specified counters. After the AD trigger condition is met, the data will be transferred to the system memory by the bus-mastering DMA.

In a multi-user or multi-tasking OS, such as Microsoft Windows, Linux, or other, it is difficult to allocate a large continuous memory block. Therefore, the bus controller provides DMA transfer with scatter-gather function to link non-contiguous memory blocks into a linked list so users can transfer large amounts of data without being limited by memory limitations. In non-scatter-gather mode, the maximum DMA data transfer size is 2 MB double words (8 MB bytes); in scatter-gather mode, there is no limitation on DMA data transfer size except the physical storage capacity of the system.

Users can also link descriptor nodes circularly to achieve a multi-buffered DMA. Figure 3-3 illustrates a linked list comprising three DMA descriptors. Each descriptor contains a PCI address, PCI dual address, a transfer size, and the pointer to the next descriptor. PCI address and PCI dual address support 64-bit addresses which can be mapped into more than 4 GB of address space, but the subsequent descriptor address must be less than 4GB.

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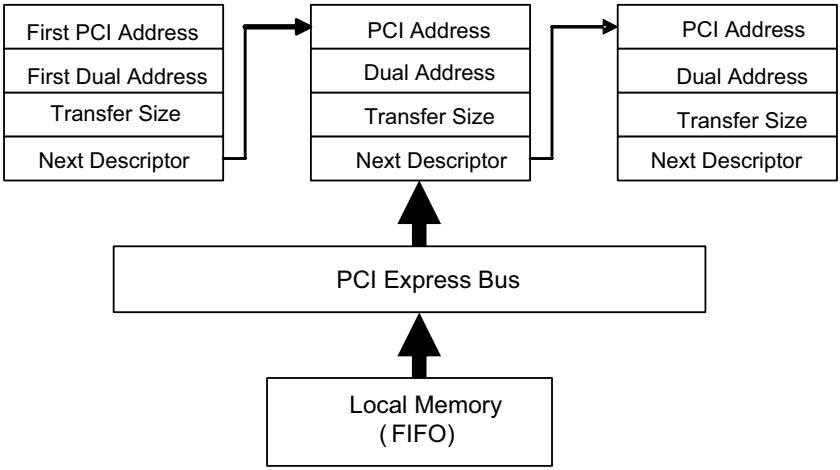


Figure 3-3: Linked List of PCI Address DMA Descriptors

3.3 Trigger Source

This section details PXIe-9834's triggering operations.

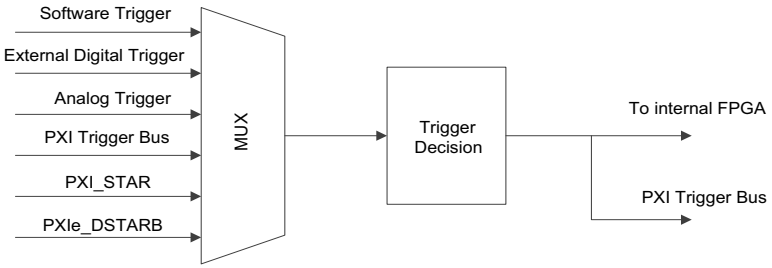


Figure 3-4: Trigger Architecture

The PXIe-9834 requires a trigger to implement acquisition of data. Configuration of triggers requires identification of trigger sources. The PXIe-9834 supports internal software trigger, external digital trigger, analog trigger from AI CH0 to CH3, PXI Trigger Bus [0..7],

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PXI Star and PXIe differential star (PXIe_DSTARB). The trigger decision sends a trigger signal to internal FPGA for acquisition operation, as well as one of the PXI Trigger Bus bit for multi-module synchronization operations.

3.3.1 Software Trigger

The software trigger, generated by software command, is asserted immediately following execution of specified function calls to begin the operation.

3.3.2 External Digital Trigger

An external digital trigger is generated when a TTL signal rising edge or falling edge is detected at the SMA connector TRG IN on the front panel. As shown, trigger polarity can be selected by software. Note that the signal level of the external digital trigger signal should be TTL compatible, and the minimum pulse width 20 ns.

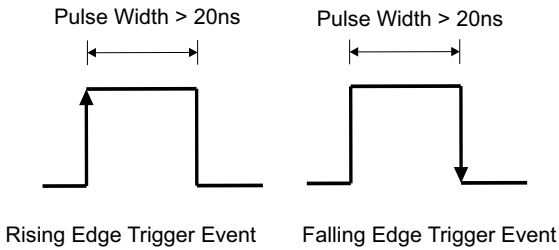


Figure 3-5: External Digital Trigger

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3.3.3 Analog Trigger

An analog trigger is generated when one of AI input signal CH0 to CH3 meets the trigger condition. The trigger conditions for analog triggers as shown in Figure 3-6.

Rising Edge Trigger

This trigger event occurs when the analog input signal changes from a voltage lower than the specified trigger level to one higher than the specified trigger level.

Falling Edge Trigger

This trigger event occurs when the analog input signal changes from a voltage higher than the specified trigger level to one lower than the specified trigger level.

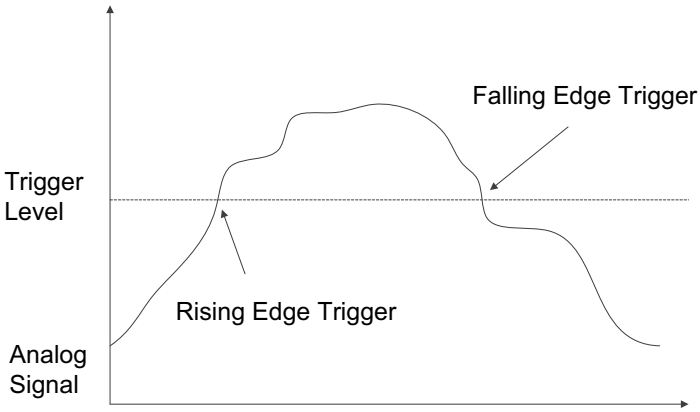


Figure 3-6: Analog Trigger Conditions

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3.3.4 PXI Trigger Bus

The PXIe-9834 utilizes PXI Trigger Bus[0..7] as multi-module synchronization interface. The interconnected bus provided by PXI Trigger Bus supports easy synchronization of multiple modules.

When configured as input, the PXIe-9834 serves as a slave module and will wait to commence signal acquisition until receiving a trigger from the PXI Trigger Bus. When configured as output, the PXIe-9834 serves as a master module and can output trigger to one of the PXI Trigger Bus. Each signal can be routed from one of the PXI Trigger Bus[0..7] by software programming.

3.3.5 PXI Star

When PXI STAR is selected as trigger source, the PXIe-9834 can accept a TTL-compatible digital signal as a trigger signal. The trigger occurs when a rising edge or falling edge is detected at PXI STAR. This utility can configure the trigger polarity. The minimum pulse width requirement of this digital trigger signal is 20ns.

3.3.6 PXIe Differential Trigger

PXIe-9834 also features a trigger source from PXIe differential trigger pin PXIe_DSTARB. The PXIe_DSTARB is a differential signal distributed from the PXIe system timing slot, with timing skew between any peripheral slots less than 150ps. This low slot-to-slot skew makes it ideal for transferring synchronization triggers. The trigger occurs when a rising edge or falling edge is detected at PXIe_DSTARB. Software can configure trigger polarity. Minimum pulse width requirement of this digital trigger signal is 20ns.

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3.4 Trigger Modes

Trigger modes applied to trigger sources initiate different data acquisition timings when a trigger event occurs. The following trigger mode descriptions are applied to analog input function.

3.4.1 Post Trigger Mode

Post-trigger acquisition is applicable when data is to be collected after the trigger event, as shown. When the operation starts, PXIe-9834 waits for a trigger event. Once the trigger signal is received, acquisition begins. Data is generated from ADC and transferred to system memory continuously. The acquisition stops once the total data amount reaches a predefined value.

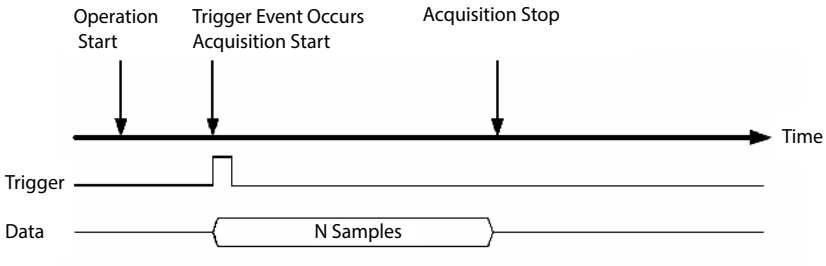


Figure 3-7: Post-Trigger Acquisition

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3.4.2 Delayed Trigger Mode

Delayed-trigger acquisition is utilized to postpone data collection after the trigger event, as shown. When the PXIe-9834 receives a trigger event, a time delay is implemented before commencing acquisition. The delay is specified by a 16-bit counter value such that a maximum thereof is the period of TIMEBASE X (2^{16}), and the minimum is the timebase period.

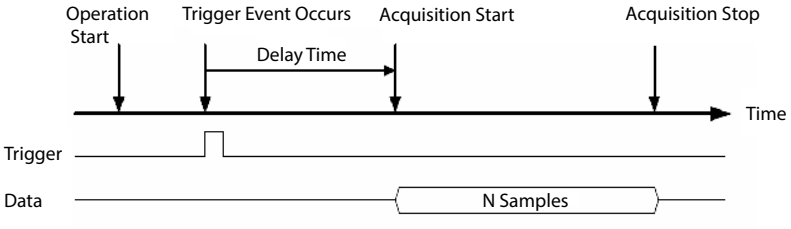


Figure 3-8: Delayed Trigger Mode Acquisition

3.4.3 Pre-Trigger Mode

Collects data before the trigger event, starting once specified function calls are executed to begin the pre-trigger operation, and stopping when the trigger event occurs. If the trigger event occurs after the specified amount of data has been acquired, the system stores only data preceding the trigger event by a specified amount, as follows.

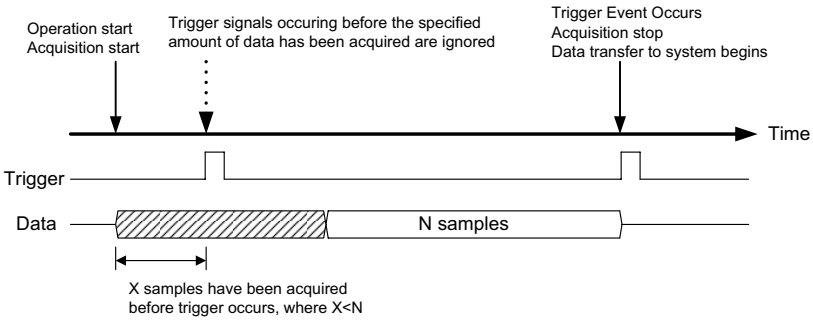


Figure 3-9: Pre-Trigger Mode Acquisition

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3.4.4 Middle Trigger Mode

Collects data before and after the trigger event, with the amount to be collected set individually (M and N samples), as follows

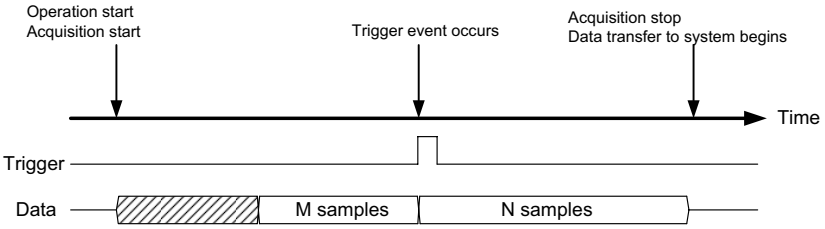


Figure 3-10: Middle Trigger Mode Acquisition

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3.4.5 Acquisition with Re-Triggering

A digitizer acquires a trace of N samples/channel for a single acquisition. Re-Trigger mode can also be set to automatically acquire R traces, containing N*R samples/channel of data, without additional software intervention.

The Re-Trigger setting can be used for Post-Trigger and Delayed-Trigger modes, with different limitations on the spacing between trigger events in each mode. Trigger events arriving too close to the previous instance will be ignored by the digitizer.

- In Post-Trigger mode, the minimum spacing between trigger events is N+1
- In Delayed-Trigger mode, the minimum spacing between trigger events is (N+D)+1, where D is the number of the delayed setting
- If R is set to zero, it means infinite re-trigger.

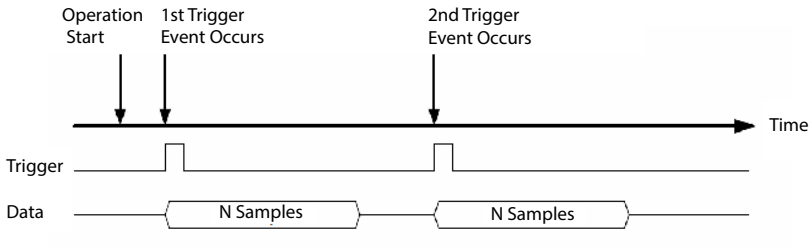


Figure 3-11: Re-Trigger Mode Acquisition

3.5 Timebase

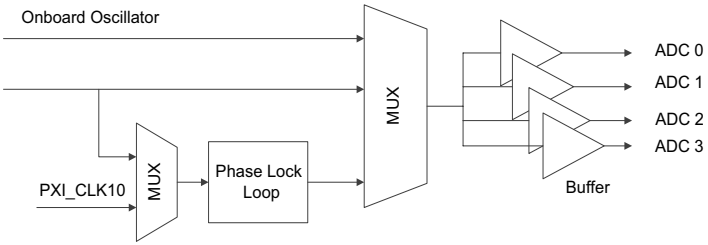


Figure 3-12: Timebase Architecture

3.5.1 Internal Sampling Clock

The PXIe-9834 internal 80MHz crystal oscillator acts as a sampling clock for ADC.

3.5.2 External Sampling Clock

For different frequency sampling clock settings, the PXIe-9834 provides external clock input from front panel SMA connector (CLK IN). When an external sampling clock is selected, the ADC sampling frequency switches to external clock source, with clock source frequency available from 10MHz to 20MHz. IT should be noted that if the frequency of the external sample clock is changed, the ADC needs to be re-configured synchronously. AI configuration via software API is thus necessary. For example, in C/C++ API, API function WD_AI_Config() must be called.

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3.5.3 External Reference Clock

The onboard phase-lock loop (PLL) circuit allows the PXIe-9834 to synch to an external 10MHz reference, in situation where multi-module synchronization in the timebase is needed. By software command, the CLK IN will route external 10MHz clock to the PLL synthesizer and generate a precise 80MHz clock for ADC.

As an added benefit from the PXIe platform, the chassis also provides reference 10MHz clock to each peripheral PXIe slot. The PXIe-9834 also routes this 10MHz to internal PLL circuit, enabling synchronization of multiple PXIe-9834 modules in a single chassis with no external cabling requirement.

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3.6 Acquisition Timing Control

The PXIe-9834 commences acquisition upon receipt of a trigger event originating with software command, external digital trigger, analog trigger, PXI_STAR, PXI Trigger Bus, or PXIe_DSTARB. Trigger mode allows collection of data when the trigger event occurs, depending trigger mode type. timebase provides an essential timing clock for ADC operation. To achieve different acquisition timing, more configurations may be required.

Using Post-Trigger mode as an example, as shown in the following figure, when a trigger is accepted by the digitizer, the acquisition engine commences acquisition of data from ADC and stores the sampled data to onboard memory. When onboard memory is not empty, data will be transferred to system memory automatically via the DMA (Direct Memory Access) engine. The sampled data is generated continuously at the rising edge of timebase according to the scan interval counter (ScanIntrv) setting. When sampled data reaches a specified value (DataCnt), acquisition is complete.

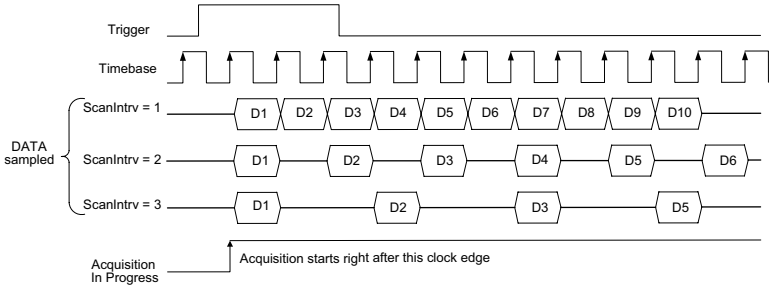


Figure 3-13: Varying Sampling Rates via Scan Interval Counter

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To achieve sampling rates other than 80MS/s, the scan interval counter (ScanIntrv) needs to be specified. For example, if the scan interval counter is set to 2, the equivalent sampling rate is 80MS/s/2=40MS/s. If 3, the equivalent sampling rate is 80MS/s/3= 26.66MS/s, and vice versa. The scan interval counter is 16 bits in width, therefore the lowest sampling rate is 1.121KS/s (80MS/s/ 65535).

Counter	Function	Length	Valid Value	Comment
ScanIntrv	Scan Interval Counter	16-bit	1-65535	Timebase divider to achieve equivalent sampling rate of the digitizer, when sampling rate=timebase/ ScanIntrv
DataCnt	Data Counter	31-bit	1-2147483647	Specifies the amount of data to be acquired; invalid when double buffer mode (infinite data number) is selected for continuous data sampling
trigDelayTicks	Delay Trigger Counter	16-bit	1-65535	Indicates time between a trigger event and commencement of acquisition, where unit of a delay counter is the period of the timebase (See “Delayed Trigger Mode” on page 32.)
ReTrgCnt	Re-Trigger Counter	31-bit	1-2147483647	Enables re-trigger to accept multiple triggers (See “Acquisition with Re-Triggering” on page 34.)

Table 3-4: Counter Parameters and Description

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3.7 Synchronizing Multiple Modules

Analog input channels on a single module, sharing the same timebase and trigger signals, are automatically synchronized. When synchronizing analog input channels between modules, however, correct module configuration and timebase and trigger signal wiring are critical for optimum synchronization.

Digitizer modules such as the PXIe-9834 support trigger synchronization and timebase synchronization.

Trigger synchronization implements a signal that initiates acquisition, and timebase synchronization provides the fundamental clock for AD operation.

As shown in the following, two digitizer modules operating at diverse onboard clock and trigger signals (free run) result in not only trigger time difference, but also clock phase error.

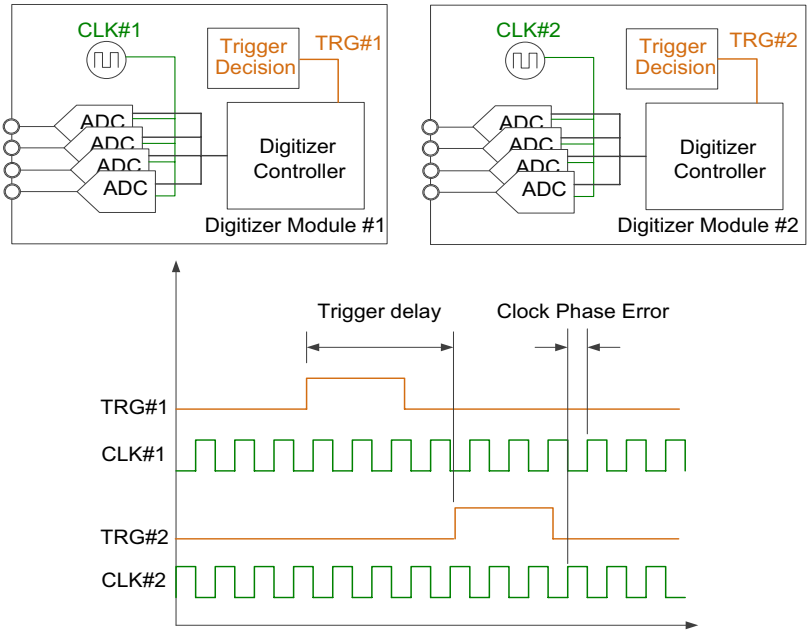


Figure 3-14: Non-synched Digitizer Modules

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With appropriate configuration of digitizer modules and effective instrument support, however, trigger or timebase synchronization, or both can be achieved, commensurate with application requirements.

As shown in the following, in a simple synchronization architecture, two digitizer modules receive trigger and timebase from a function generator. With required buffering of trigger and timebase signals and equal wiring length between the function generator and digitizers, trigger and timebase synchronization are possible. In this scenario, the function generator is a master device that outputs trigger and timebase, and the two digitizers are slave devices sharing the same trigger and timebase.

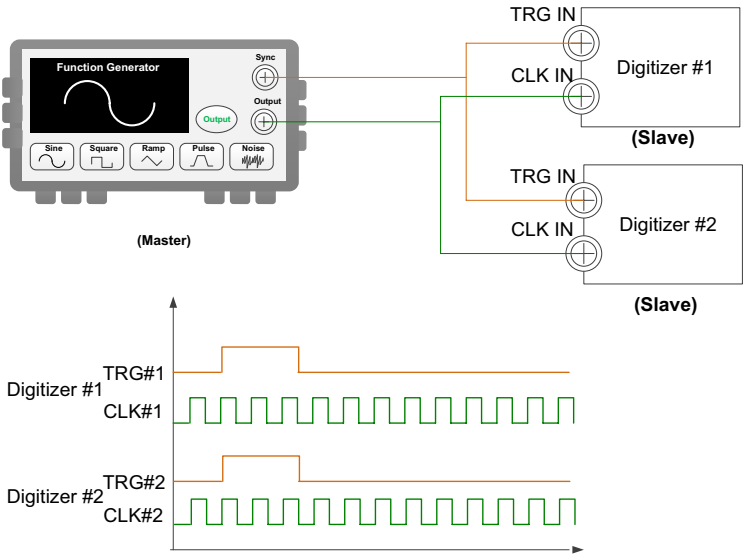


Figure 3-15: External Instrument Synchronization

Some digitizer modules provide advanced features that can output trigger or timebase to external devices, enabling multi-module synchronization as well. As shown in the following, digitizer #1 acts as a master device and transmits trigger/timebase to the two slave digitizers.

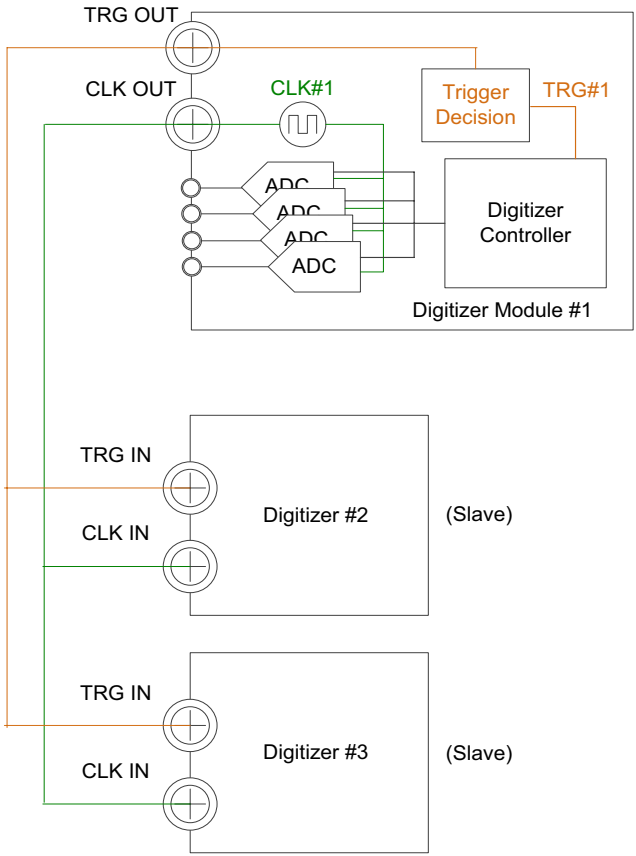


Figure 3-16: Module-based Synchronization

In the scenarios described, trigger and timebase signal buffering is required, with one or multiple signal buffering modules necessary

to maximize signal quality. Moreover, signal wiring must be precisely deployed to minimize timing skew.

The PXIe-9834, based on PXI Express HW & SW specifications, enables trigger and clock signals to be fully leveraged and benefits from the routing architecture of the PXI Express chassis. The PXI Express chassis provides additional timing and synchronization capabilities for more accurate measurement and improved new application management. Overall PXI Express chassis instrumentation signals are as follows.

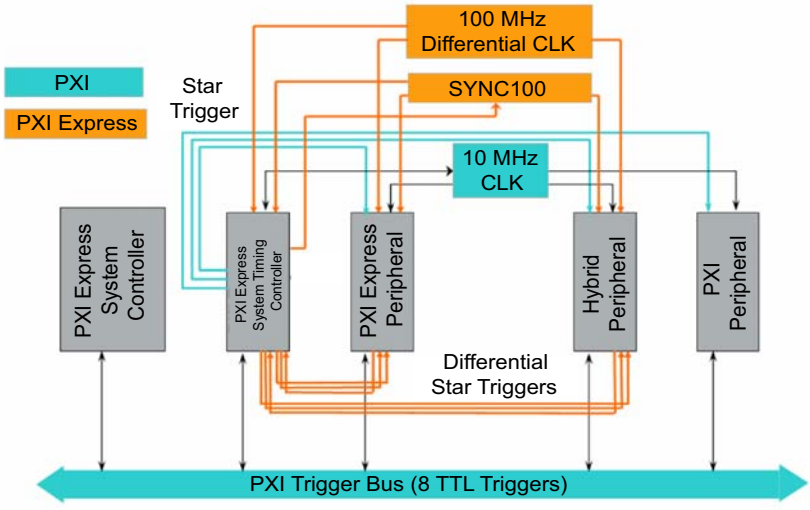


Figure reprinted courtesy of PXI Express Specification Tutorial.pdf from PXI System Alliance website (www.pxisa.org).

Figure 3-17: PXIe Instrumentation Signals

In the PXIe chassis, a system timing slot distributes trigger signals through PXI_STAR and PXIe differential star triggers. The 8-bit parallel PXI Trigger Bus provides additional channels for transmitting and receiving triggers between peripheral slots. The PXIe chassis further provides 10MHz (PXI_CLK10) clock options distributed to each peripheral slot with minimal clock skew.

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3.7.1 Multi-module Synchronization Interfaces

As shown in the following, four trigger input channels on the PXIe-9834 can receive triggers from a master device. The external digital trigger input is on the front panel, and the PXI Trigger Bus, PXI_STAR, and PXIe_DSTARB are from the PXIe chassis. When the PXIe-9834 acts as a master device, its trigger signal is output to one bit of the PXI Trigger Bus, as determined by software selection.

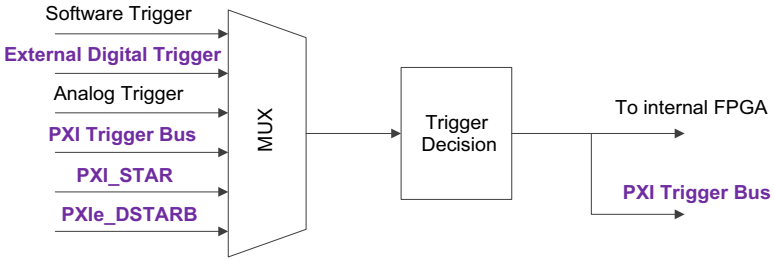


Figure 3-18: Trigger Architecture

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For timebase synchronization, the PXIe-9834 acts as a slave device, receiving external sampling clock or 10MHz reference clock from the front panel CLK IN or PXI_CLK10 from the PXIe chassis.

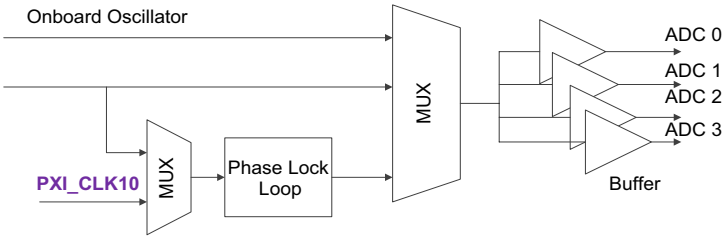


Figure 3-19: PXI_CLK10 as 10MHz Reference

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Appendix A Calibration

This chapter introduces the calibration process to minimize analog input measurement errors.

A.1 Calibration Constant

The PXIe-9834 is factory calibrated before shipment, with associated calibration constants written to the onboard EEPROM. At system boot, the PXIe-9834 driver loads these calibration constants, such that analog input path errors are minimized. ADLINK provides a software API for calibrating the PXIe-9834.

The onboard EEPROM provides two banks for calibration constant storage. Bank 0, the default bank, records the factory calibrated constants, providing written protection preventing erroneous auto-calibration. Bank 1 is user-defined space, provided for storage of self-calibration constants. Upon execution of auto-calibration, the calibration constants are recorded to Bank 1.

When PXIe-9834 boots, the driver accesses the calibration constants and is automatically set to hardware. In the absence of user assignment, the driver loads constants stored in bank 0. If constants from Bank 1 are to be loaded, the preferred bank can be designated as boot bank by software. Following re-assignment of the bank, the driver will load the desired constants on system reboot. This setting is recorded to EEPROM and is retained until reconfiguration.

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A.2 Auto-Calibration

Because errors in measurement and outputs will vary with time and temperature, re-calibration is recommended when the module is installed. Auto-calibration can measure and minimize errors without external signal connections, reference voltages, or measurement devices.

The PXIe-9834 has an on-board calibration reference to ensure the accuracy of auto-calibration. The reference voltage is measured on the production line and recorded in the on-board EEPROM.

Before initializing auto-calibration, it is recommended to warm up the PXIe-9834 for at least 20 minutes and remove connected cables.

NOTE:

It is not necessary to manually factor delay into applications, as the PXIe-9834 driver automatically adds the compensation time.

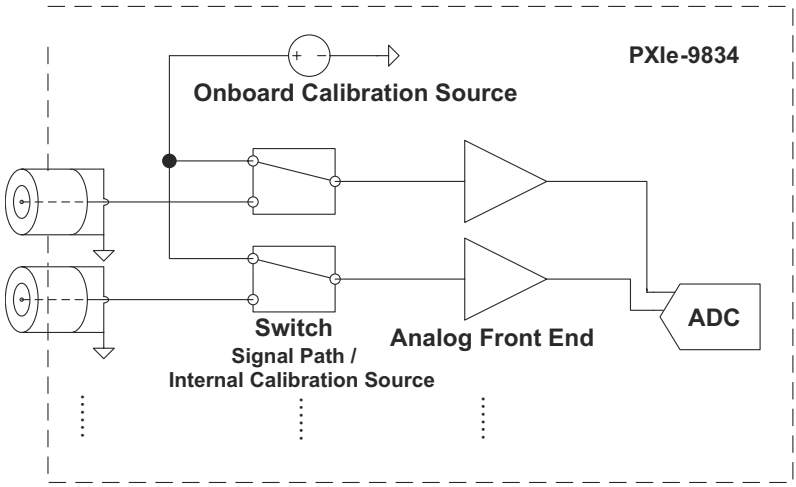


Figure A-1: Auto-Calibration Block Diagram

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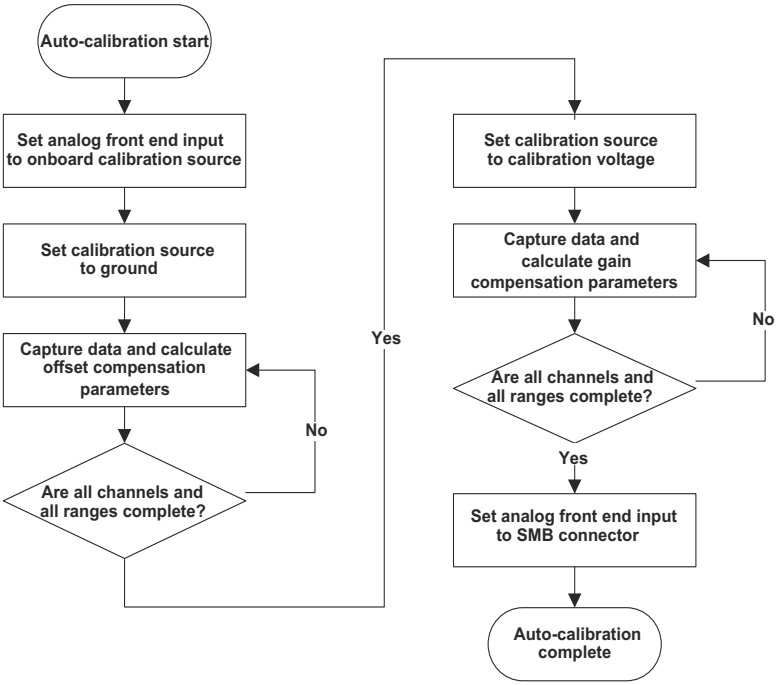


Figure A-2: Auto-Calibration Flow

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Important Safety Instructions

For user safety, please read and follow all instructions, Warnings, Cautions, and Notes marked in this manual and on the associated device before handling/operating the device, to avoid injury or damage.

S'il vous plaît prêter attention stricte à tous les avertissements et mises en garde figurant sur l'appareil , pour éviter des blessures ou des dommages.

- Read these safety instructions carefully
- Keep the User's Manual for future reference
- Read the Specifications section of this manual for detailed information on the recommended operating environment
- The device can be operated at an ambient temperature of 50ºC
- When installing/mounting or uninstalling/removing device; or when removal of a chassis cover is required for user servicing:
  - Turn off power and unplug any power cords/cables
  - Reinstall all chassis covers before restoring power
- To avoid electrical shock and/or damage to device:
  - Keep device away from water or liquid sources
  - Keep device away from high heat or humidity
  - Keep device properly ventilated (do not block or cover ventilation openings)
  - Always use recommended voltage and power source settings
  - Always install and operate device near an easily accessible electrical outlet
  - Secure the power cord (do not place any object on/over the power cord)
  - Only install/attach and operate device on stable surfaces and/or recommended mountings
- If the device will not be used for long periods of time, turn off and unplug from its power source

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- Never attempt to repair the device, which should only be serviced by qualified technical personnel using suitable tools
- A Lithium-type battery may be provided for uninterrupted backup or emergency power.



Risk of explosion if battery is replaced with one of an incorrect type; please dispose of used batteries appropriately.
Risque d'explosion si la pile est remplacée par une autre de type incorrect. Veuillez jeter les piles usagées de façon appropriée.

- The device must be serviced by authorized technicians when:
  - The power cord or plug is damaged
  - Liquid has entered the device interior
  - The device has been exposed to high humidity and/or moisture
  - The device is not functioning or does not function according to the User's Manual
  - The device has been dropped and/or damaged and/or shows obvious signs of breakage
- Disconnect the power supply cord before loosening the thumbscrews and always fasten the thumbscrews with a screwdriver before starting the system up
- It is recommended that the device be installed only in a server room or computer room where access is:
  - Restricted to qualified service personnel or users familiar with restrictions applied to the location, reasons therefor, and any precautions required
  - Only afforded by the use of a tool or lock and key, or other means of security, and controlled by the authority responsible for the location

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	**BURN HAZARD** Touching this surface could result in bodily injury. To reduce risk, allow the surface to cool before touching. ***RISQUE DE BRÛLURES*** *Ne touchez pas cette surface, cela pourrait entraîner des blessures.* *Pour éviter tout danger, laissez la surface refroidir avant de la toucher.*

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Getting Service

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