PXIe-9842

1-CH 14-Bit 200 MS/s
High-Speed PXI Express Digitizer

User's Manual



Manual Rev.:	2.00
Revision Date:	Feb. 24, 2012
Part No:	50-17039-1000

Recycled Paper

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Revision History

Revision	Release Date	Description of Change(s)
2.00	2012/02/24	Initial Release

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Preface

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Additional information, aids, and tips that help users perform tasks.



Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.



Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

The PXIe-9842 is a high-speed 1-CH 14-bit 200 MS/s digitizer, specifically designed for applications such as LIDAR testing, optical fiber testing and radar signal acquisition. Analog input with 100 MHz bandwidth receives ±1V high-speed signals with 50Ω impedance. With a simplified front-end design and highly stable onboard reference, the PXIe-9842 provides both highly accurate measurement results and high dynamic performance.

Ideal for environments requiring real-time acquisition and transfer of data, the PXIe-9842 is designed on the PXI Express x4 bus as interface. When signals are converted from analog to digital, data is continually transferred to host system memory due to PCI Express high bandwidth features.

The PXIe-9842 is auto-calibrated with an onboard reference circuit that calibrates the offset and acquires errors of analog input. Once auto-calibration is complete, the calibration constant is stored in EEPROM, such that these values can be loaded and used as needed by the board. Because all the calibration is conducted automatically, there remains no requirement to calibrate the module manually.

1.1 Features

- PXI Express hardware specification Rev. 1.0 compliant
- Up to 200 MS/s sampling rate
- High resolution 14-Bit ADC
- 100 MHz bandwidth for analog input
- High dynamic performance, up to 70 dB SNR with 10 MHz sine wave input
- Scatter-Gather DMA data transfer for high-speed data streaming
- Support for:
  - one external digital trigger input
  - one digital trigger output to external instrument
  - auto-calibration

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1.2 Applications

- Radar signal acquisition
- IF signal spectrum monitoring
- Optical fiber testing
- Physics laboratory and research environments
- Cable fault location and partial discharge monitoring for power applications

1.3 Specifications

1.3.1 Analog Input

Channel Characteristics	
Channels	1 single-ended channel
Connector type	SMA screw type
Input coupling	DC
ADC resolution	14-Bit
Input signal range	±1.0 V
Overvoltage	±5 V
Input impedance	50 Ω ± 2%
Offset error	±1 mV
Gain error	±0.5%

Table 1-1: Channel Characteristics

Analog Input Bandwidth (-3 dB)	
±1.0 V input	100 MHz

Table 1-2: Analog Input Bandwidth

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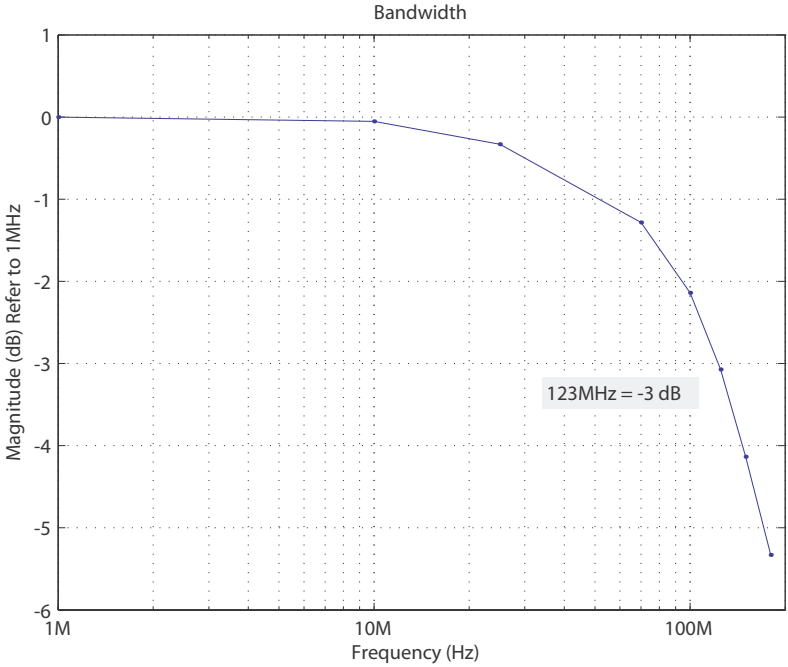


Figure 1-1: Analog Input Channel Bandwidth, ±1 V Input Range

1.3.2 Timebase

Sample clock source	Internal: onboard clock (oscillator)
Timebase frequency	200 MHz
Sampling rate	200 MS/s ~ 3051.75 S/s
Internal Timebase Accuracy	< ±25 ppm

Table 1-3: Timebase

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1.3.3 Triggers

Trigger Source & Mode	
Trigger source	Software command, external digital trigger, PXI star trigger, and PXI trigger bus [0..7]
Trigger mode	Post trigger, delay trigger, re-trigger for all trigger modes

Table 1-4: Trigger Source & Mode

Digital Trigger Input	
Sources	Front panel SMA connector
Compatibility	3.3 V TTL, 5 V tolerant
Input high threshold	2.0 V
Input low threshold (VIL)	0.8 V
Maximum input overload	-0.5 V ~ +5.5 V
Trigger polarity	Rising or falling edge
Pulse width	20 ns minimum

Table 1-5: Digital Trigger Input

Digital Trigger Output	
Compatibility	5 V TTL
Output high threshold (VOH)	2.4 V
Output low threshold (VOL)	0.2 V
Trigger polarity	Positive or negative
Pulse width	50 ns, 100 ns, 150 ns, 200 ns, 500 ns, 1 µs, 2 µs, 7.5 µs, and 10 µs
Trigger output driving capacity	Capable of driving 50Ω load

Table 1-6: Digital Trigger Output

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1.3.4 General Specifications

Specifications	
Physical dimensions	160 W x 100 H mm (6.3 x 3.94 in.)
Bus	
Bus interface	PXI Express, PXI hybrid compatible
PCIe signaling	PCI Express x 4, Gen 1
Environmental toleance	
Operating	Temperature: 0°C - 50°C Relative humidity: 5% - 95%, non-condensing
Storage	Temperature: -20°C - +80°C Relative humidity: 5% - 95%, non-condensing

Calibration	
Onboard reference	+5 V
Temperature coefficient	≤ ±5 ppm/°C
Warm-up time	15 minutes

Power Consumption		
Power Rail	**Standby Current (mA)**	**Full Load (mA)**
+3.3 V	1275	1276
+12 V	306	308

1.4 Software Support

ADLINK provides versatile software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environments such as LabVIEW®.

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All software options are included in the ADLINK All-in-One CD. Commercial software drivers are protected with licensing codes. Without the code, you may install and run the demo version for trial/demonstration purposes for only up to two hours. Contact your ADLINK dealer to purchase the software license.

1.4.1 SDK

For customers who want to write their own programs, ADLINK provides the following software development kits.

- ▷ DAQPilot for Windows, compatible with various application environments, such as VB.NET, VC.NET, VB/VC++, BCB, and Delphi
- ▷ DAQPilot for LabVIEW
- ▷ Toolbox adapter for MATLAB

1.4.2 WD-DASK

WD-DASK includes device drivers and DLL for Windows 2000/ XP/Vista/7. DLL is binary compatible across Windows 2000/ XP/ Vista/7. This means all applications developed with WD-DASK are compatible with these Windows operating systems. The devel- opment environment may be VB, VB.NET, VC++, BCB, and Delphi, or any Windows programming language that allows calls to a DLL. The WD-DASK user and function reference manuals are on the ADLINK All-in-One CD.

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2 Getting Started

This chapter describes proper installation environment, installation procedures, package contents and basic information users should be aware of regarding the PXIe-9842.


NOTE:

Diagrams and illustrated equipment are for reference only. Actual system configuration and specifications may vary.

2.1 Installation Environment

When unpacking and preparing to install, please refer to Important Safety Instructions.

Only install equipment in well-lit areas on flat, sturdy surfaces with access to basic tools such as flat- and cross-head screwdrivers, preferably with magnetic heads as screws and standoffs are small and easily misplaced.

Recommended Installation Tools

- Phillips (cross-head) screwdriver
- Flat-head screwdriver
- Anti-static wrist strap
- Antistatic mat

ADLINK PXIe-9842 DAQ modules are electrostatically sensitive and can be easily damaged by static electricity. The module must be handled on a grounded anti-static mat. The operator must wear an anti-static wristband, grounded at the same point as the anti-static mat.

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Inspect the carton and packaging for damage. Shipping and handling could cause damage to the equipment inside. Make sure that the equipment and its associated components have no damage before installation.



The equipment must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the equipment and wear a grounded wrist strap when servicing.

- **Package Contents**
- PXIe-9842 high-speed digitizer
- ADLINK All-in-one compact disc
- PXIe-9842 User's Manual

If any of these items are missing or damaged, contact the dealer



Do not install or apply power to equipment that is damaged or missing components. Retain the shipping carton and packing materials for inspection. Please contact your ADLINK dealer/ vendor immediately for assistance and obtain authorization before returning any product.

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2.2 Device Layout and I/O Array

NOTE:

All dimensions are in mm

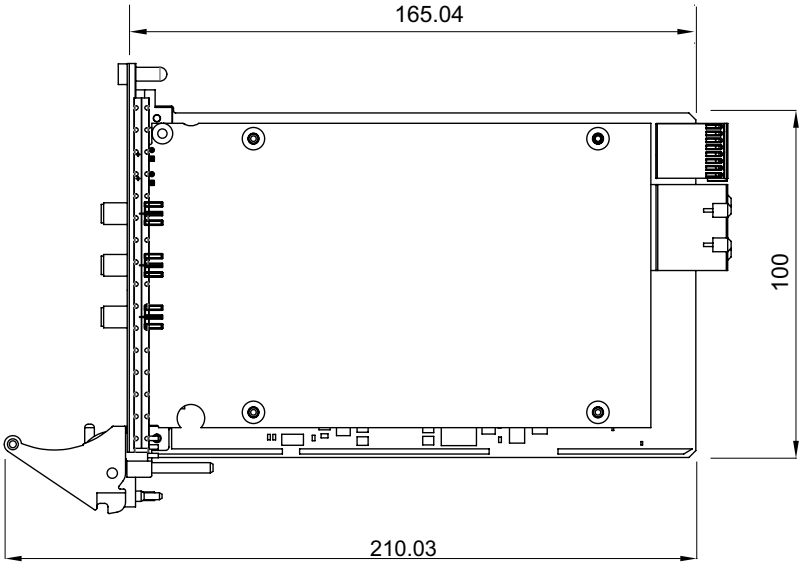


Figure 2-1: PXIe-9842 Schematic

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The PXIe-9842 I/O array is labeled to indicate connectivity, as shown.



Figure 2-2: PXIe-9842 I/O array

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Name	Faceplate Legend	Type	Remark
LED1	N/A	Green	ON status indicates card registered to system OFF status indicates card withdrawn
LED2	N/A	Blue	BLINK indicates ongoing acquisition OFF indicates acquisition stopped
Analog Input Channel	CH0	SMA Screw Type	Analog input channel
Ext. Digital Trigger Input	TRG IN		External digital trigger input, receiving trigger signal from external instrument and initiating acquisition
Trigger Output	TRG OUT		Trigger output, in which every time acquisition begins, a pulse synchronized with Timebase clock asserts and is output through this connector, at pulse width programmable from 50ns to 10µs via software

Table 2-1: PXIe-9842 I/O Array

2.3 Installing the module

1. Turn off the PXI system/chassis and disconnect the power cable from the power source.
2. Align the module's edge with the module guide in the PXI chassis.
3. Slide the module into the chassis until resistance is felt from the PXI connector.
4. Push the ejector latch upwards and fully insert the module into the chassis.

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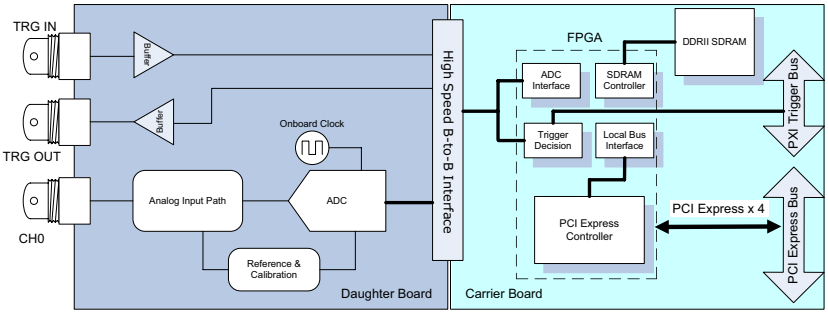
5. Once the module is fully seated, a “click” can be heard from the ejector latch.
6. Tighten the screw on the front panel.
7. Connect the power plug to a power source and power up the PXI system/chassis.

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3 Operations

This chapter contains information regarding analog input, analog output, triggering and timing for the PXIe-9842.

3.1 Functional Block Diagram



3.2 Analog Input Channel

3.2.1 Analog Input Front-End Configuration

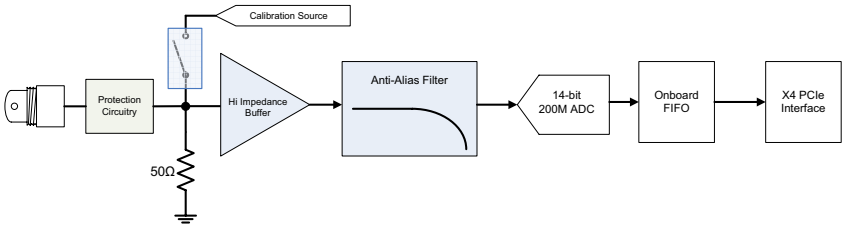


Figure 3-1: Analog Input Architecture of the PXIe-9842

Input Configuration

The input channel terminates with equivalent 50 Ω input impedance. An anti-aliasing filter is adopted to eliminate high frequency noise exceeding 100MHz. The 14-bit ADC provides not only accurate DC performance but also high signal-to-noise ratio, and high spurious-free dynamic range in AC perfor-

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mance. The ADC transfers data to system memory via the high speed PCI Express X 4 interface.

For auto-calibration, internal calibration provides stable and accurate reference voltage to the AI.

3.2.2 Input Range and Data Format

Data format of the PXIe-9842 is 2's complement. The ADC data of PXIe-9842 is on the 14 MSB of the 16-bit A/D data. The 2 LSB of the 16-bit A/D data should be truncated by software. A/D data structure is as follows.

D15	D14	D13	D12	….	D3	D2	D1	D0
D15 ~ D2 bits represent the data from ADC (2's complement) D1, D0 bits are identical to D2 bit and should be truncated.								

Table 3-1: Input Range and Data Format

Description	Full-scale range	Least significant bit	FSR-1LSB	-FSR
Bipolar Analog Input	±1V	122.07 μV	0.999940 V	-1.000 V
Digital Code	N/A	N/A	7FFC	8000

Table 3-2: Input Range FSR and –FSR Values

Description	Midscale +1LSB	Midscale	Midscale –1LSB
Bipolar Analog Input	0.000122 V	0 V	-0.000122 V
Digital Code	0001	0000	FFFC

Table 3-3: Input Range Midscale Values

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3.2.3 DMA Data Transfer

PCI Express offers dedicated bandwidth of up to 250MB/s. Unlike the PCI bus, having parallel bus architecture dividing bandwidth among all devices on the bus, PCI Express features peer-to-peer architecture with dedicated data pipelining. Data can be transferred at 2.5Gb/s, which enables a theoretical 250MB/s bandwidth per lane. With PCI Express, data bandwidth is dramatically improved compared to the PCI bus, allowing data to be streamed to the system faster with minimum onboard memory required.

One of the most important features of the PXIe-9842 is its PCI Express X 4 interface. PXIe-9842 is equipped with a 200MS/s high sampling rate ADC, generating a 400 MByte/second rate, making it useful to have a high bandwidth bus interface when streaming data from ADC to system memory.

The actual data throughput for a PC system depends on system topology, data transfer between other devices in the system, and other components in the system. For example, data transfer between digitizers and host memory usually travels through a PCIe switch before transfer to the host system. All digitizers share the bandwidth available on the link between PCIe switch and the host system.

To provide efficient data transfer, a PCI bus-mastering DMA is essential for continuous data streaming, as it helps to achieve full potential PCI Express bus bandwidth. The bus-mastering controller releases the burden on the host CPU since data is directly transferred to the host memory without intervention. Once analog input operation begins, the DMA returns control of the program. During DMA transfer, the hardware temporarily stores acquired data in the onboard AD Data FIFO, and then transfers the data to a user-defined DMA buffer in the computer.

Using a high-level programming library for high speed DMA data acquisition, the sampling period and the number of conversions needs simply to be assigned into specified counters. After the AD trigger condition is met, the data will be transferred to the system memory by the bus-mastering DMA.

In a multi-user or multi-tasking OS, such as Microsoft Windows, Linux, or other, it is difficult to allocate a large continuous memory

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block. Therefore, the bus controller provides DMA transfer with scatter-gather function to link non-contiguous memory blocks into a linked list so users can transfer large amounts of data without being limited by memory limitations. In non-scatter-gather mode, the maximum DMA data transfer size is 2 MB double words (8 MB bytes); in scatter-gather mode, there is no limitation on DMA data transfer size except the physical storage capacity of the system.

Users can also link descriptor nodes circularly to achieve a multi-buffered DMA. Figure 3-2 illustrates a linked list comprising three DMA descriptors. Each descriptor contains a PCI address, PCI dual address, a transfer size, and the pointer to the next descriptor. PCI address and PCI dual address support 64-bit addresses which can be mapped into more than 4 GB of address space.

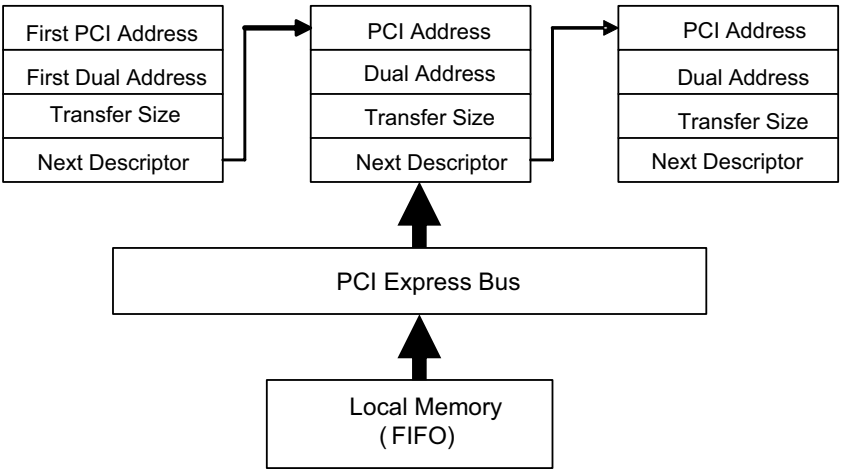


Figure 3-2: Linked List of PCI Address DMA Descriptors

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3.3 Trigger Source and Trigger Modes

This section details PXIe-9842 triggering operations.

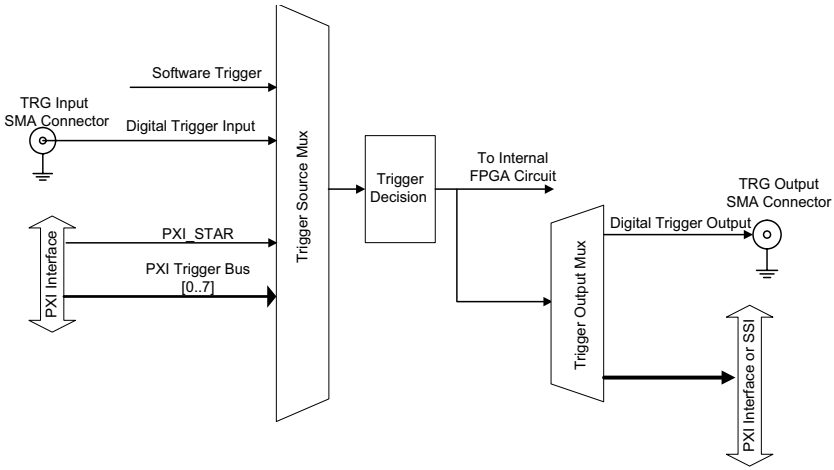


Figure 3-3: Trigger Architecture of the PXIe-9842

The PXIe-9842 requires a trigger to implement acquisition of data. Configuration of triggers requires identification of trigger source. The PXIe-9842 supports internal software trigger, external digital trigger, PXI_STAR trigger and PXI Trigger Bus [0.7].

3.3.1 Software Trigger

The software trigger, generated by software command, is asserted immediately following execution of specified function calls to begin the operation.

3.3.2 External Digital Trigger

An external digital trigger is generated when a TTL rising edge or falling edge is detected at the SMA connector TRG IN on the front panel. As shown, trigger polarity can be selected by software. Note that the signal level of the external digital trigger signal should be TTL compatible, and the minimum pulse width 20 ns.

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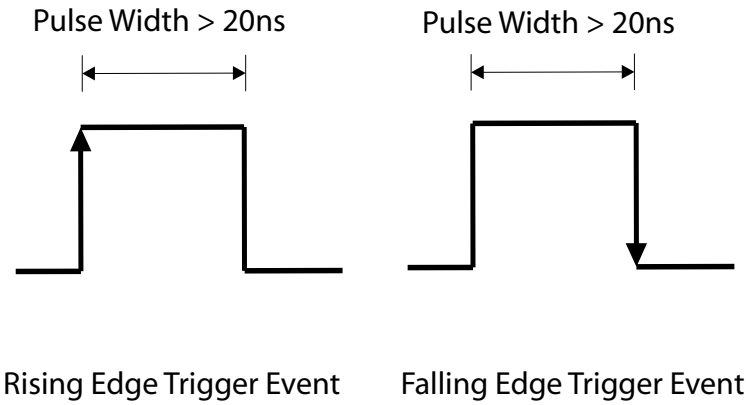


Figure 3-4: External Digital Trigger

3.3.3 PXI STAR Trigger

When PXI STAR is selected as the trigger source, the PXIe-9842 accepts a TTL-compatible digital signal as a trigger signal. Triggering occurs when a rising edge or falling edge is detected at PXI STAR, with trigger polarity configurable by software. The minimum pulse width requirement of this digital trigger signal is 20 ns.

3.3.4 PXI Trigger Bus

The PXIe-9842 utilizes PXI Trigger Bus Numbers 0 through 7 to act as a System Synchronization Interface (SSI). With the inter-connected bus provided by PXI Trigger Bus, multiple modules are easily synched. When configured as input, the PXIe-9842 serves as a slave module and can accept trigger signals from one of buses 0 through 7. When configured as output, the PXIe-9842 serves as a master module and can output trigger signals to the PXI Trigger Bus Numbers 0 through 7.

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3.3.5 Trigger Export

The PXIe-9842 can export trigger signals to the SMA TRG OUT on the front panel, and PXI Trigger Bus Numbers 0 through 7. The TRG OUT on the front panel can also be programmed to output the trigger signal when the trigger source is generated by software, PXI STAR, or PXI Trigger Bus Numbers 0 through 7. The PXIe-9842 utilizes PXI Trigger Bus Numbers 0 through 7 to act as the System Synchronization Interface. When configured as the output, the PXIe-9842 serves as a master module and can output trigger signals to synchronize the slave modules. The trigger signal can be routed to any of the seven PXI Trigger Bus Numbers via software.

3.4 Trigger Modes

Two trigger modes applied to trigger sources initiate different data acquisition timings when a trigger event occurs. The following trigger mode descriptions are applied to analog input and analog output functions.

3.4.1 Post Trigger Mode

Post-trigger acquisition is applicable when data is to be collected after the trigger event, as shown. When the operation starts, PXIe-9842 waits for a trigger event. Once the trigger signal is received, acquisition begins. Data is generated from ADC and transferred to system memory continuously. The acquisition stops once the total data amount reaches a predefined value.

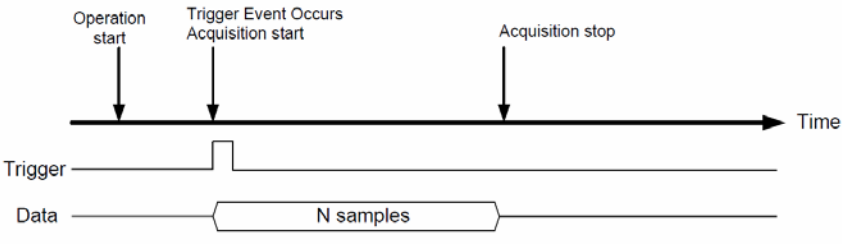


Figure 3-5: Post-Trigger Acquisition

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3.4.2 Delayed Trigger Mode

Delayed-trigger acquisition is utilized to postpone data collection after the trigger event, as shown. When PXIe-9842 receives a trigger event, a time delay is implemented before commencing acquisition. The delay is specified by a 32-bit counter value such that a maximum thereof is the period of TIMEBASE X (2^{32}), and the minimum is the Timebase period.

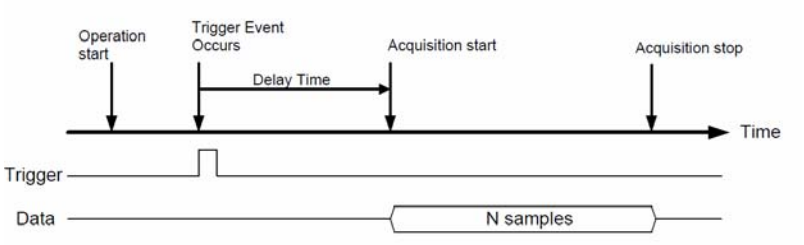


Figure 3-6: Delayed Trigger Mode Acquisition

3.4.3 Post-Trigger or Delayed-Trigger Acquisition with Re-Triggering

Post-trigger or delayed trigger acquisition with re-triggering are applicable to collect data after several trigger events, as shown. Once the number of triggers has been programmed, the digitizer acquires a specific data sample each time a trigger is accepted. The time between a previous sample and subsequent trigger event can only be one Timebase clock period. Following initial setup, the process requires no additional software intervention.

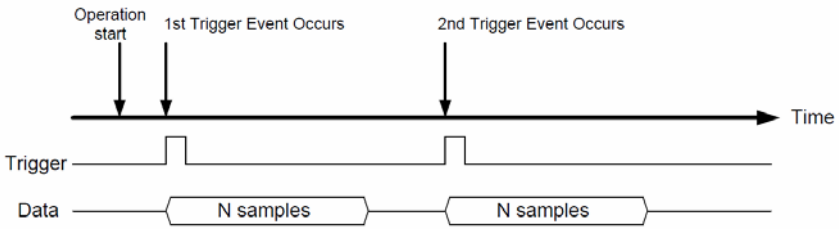


Figure 3-7: Re-Trigger Mode Acquisition

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3.5 ADC Timing Control

3.5.1 Timebase Architecture

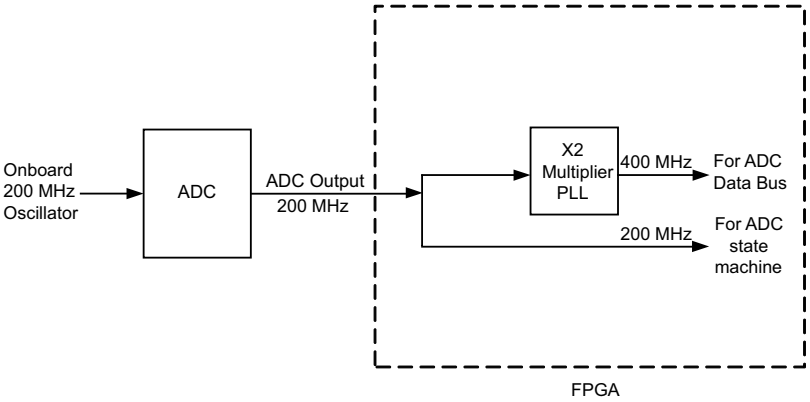


Figure 3-8: PXIe-9842 Timebase Architecture

3.5.2 Basic Acquisition Timing

The PXIe-9842 commences acquisition upon receipt of a trigger event originating with software command, external digital trigger, or the PXI Trigger Bus. The Timebase is a clock provided to the ADC and acquisition engine for essential timing. The Timebase is from an onboard 200MHz oscillator. To achieve different sampling rates, a scan interval counter is used.

Using the post-trigger mode as an example, as shown, when a trigger is accepted by the digitizer, the acquisition engine commences acquisition of data from ADC, and stores the sampled data to the onboard FIFO. When FIFO is not empty, data will be transferred to system memory immediately through the DMA engine. The sampled data is generated continuously at the rising edge of Timebase according to the scan interval counter setting. When sampled data reaches a specified value, in this example 256, acquisition ends.

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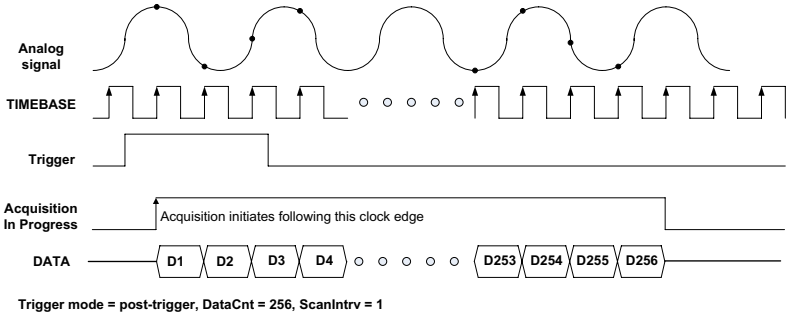


Figure 3-9: Basic Digitizer Acquisition Timing

To achieve sampling rates other than 200MS/s, a number for scan interval counter needs only be specified. For example, if the scan interval counter is set as 2, the equivalent sampling rate is 200MS/s / 2 = 100MS/s. If as 3, the equivalent sampling rate is 200MS/s / 3 = 66.66MS/s, and vice versa. The scan interval counter is 16 bits in width, therefore the lowest sampling rate is 3.051KS/s (200MS/s / 65535).

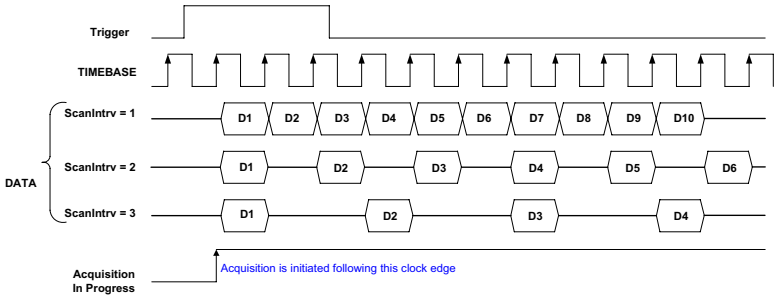


Figure 3-10: Varying Sampling Rates by Adjusting Scan Interval Counter

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Counter Name	Length	Valid Value	Description
ScanIntrv	16-bit	1 - 65535	Timebase divider to achieve equivalent sampling rate of the digitizer, where Sampling rate = Timebase / ScanIntrv
DataCnt	32-bit	1 - 536870911	Specifies the amount of data to be acquired
trigDelayTicks	32-bit	1 -536870911	Indicates time between a trigger event and commencement of acquisition. The unit of a delay count is the period of the Timebase.
ReTrgCnt	24-bit	1 -16777215	Enables re-trigger to accept multiple triggers. Please see Section 3.4.3: Post-Trigger or Delayed-Trigger Acquisition with Re-Triggering for more details.

Table 3-4: Counter Parameters and Description

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4 Calibration

This chapter introduces the calibration process to minimize analog input measurement errors and analog output errors.

4.1 Calibration Constant

The PXIe-9842 is factory calibrated before shipment, with associated calibration constants written to the onboard EEPROM. At system boot, the PXIe-9842 driver loads these calibration constants, such that analog input path and analog output circuit errors are minimized. ADLINK provides a software API for calibrating the PXIe-9842.

The onboard EEPROM provides three banks for calibration constant storage. Bank 0, the default bank, records the factory calibrated constants, providing written protection preventing erroneous auto-calibration. Banks 1 and 2, user-defined space, are provided for storage of self-calibration constants. Upon execution of auto-calibration, the calibration constants are recorded to bank 1 or 2 based on user assignment.

When PXIe-9842 boots, the driver accesses the calibration constants and is automatically set to hardware. In the absence of user assignment, the driver loads constants stored in bank 0. If constants from bank 1 or 2 are to be loaded, the preferred bank can be designated as boot bank by software. Following re-assignment of the bank, the driver will load the desired constants on system re-boot. This setting is recorded to EEPROM and is retained until re-configuration.

4.2 Auto-Calibration

Because errors in measurement and outputs will vary with time and temperature, re-calibration is recommended when the module is installed. Auto-calibration can measure and minimize errors without external signal connections, reference voltages, or measurement devices.

The PXIe-9842 has an on-board calibration reference to ensure the accuracy of auto-calibration. The reference voltage is mea-

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sured on the production line and recorded in the on-board EEPROM.

Before initializing auto-calibration, it is recommended to warm up the PXIe-9842 for at least 20 minutes and remove connected cables.



NOTE:

It is not necessary to manually factor delay into applications, as the PXIe-9842 driver automatically adds the compensation time.

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

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- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.
- A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced with an incorrect type; please dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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Getting Service

Contact us should you require any service or assistance.

ADLINK Technology, Inc.
Address: 9F, No.166 Jian Yi Road, Zhonghe District
New Taipei City 235, Taiwan
新北市中和區建一路 166 號 9 樓
Tel: +886-2-8226-5877
Fax: +886-2-8226-5717
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-360-0222
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203)
300 Fang Chun Rd., Zhangjiang Hi-Tech Park,
Pudong New Area, Shanghai, 201203 China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1, B/D
Shang Di East Rd., Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8625
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园
A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7,
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

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ADLINK Technology, Inc. (French Liaison Office)
Address: 15 rue Emile Baudot, 91300 Massy CEDEX, France
Tel: +33 (0) 1 60 12 35 66
Fax: +33 (0) 1 60 12 35 66
Email: france@adlinktech.com

ADLINK Technology Japan Corporation
Address: 〒101-0045 東京都千代田区神田鍛冶町 3-7-4
神田 374 ビル 4F
KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
Chiyoda-ku, Tokyo 101-0045, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5209-6013
Email: japan@adlinktech.com

ADLINK Technology, Inc. (Korean Liaison Office)
Address: 서울시 서초구 서초동 1675-12 모인터빌딩 8 층
8F Mointer B/D,1675-12, Seocho-Dong, Seocho-Gu,
Seoul 137-070, Korea
Tel: +82-2-2057-0565
Fax: +82-2-2057-0563
Email: korea@adlinktech.com

ADLINK Technology Singapore Pte. Ltd.
Address: 84 Genting Lane #07-02A, Cityneon Design Centre,
Singapore 349584
Tel: +65-6844-2261
Fax: +65-6844-2263
Email: singapore@adlinktech.com

ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)
Address: 1st Floor, #50-56 (Between 16th/17th Cross) Margosa Plaza,
Margosa Main Road, Malleswaram, Bangalore-560055, India
Tel: +91-80-65605817, +91-80-42246107
Fax: +91-80-23464606
Email: india@adlinktech.com

ADLINK Technology, Inc. (Israeli Liaison Office)
Address: 6 Hasadna St., Kfar Saba 44424, Israel
Tel: +972-9-7446541
Fax: +972-9-7446542
Email: israel@adlinktech.com

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