Q7-AL

User's Manual

Qseven Computer On Module (COM) with
Embedded Intel® Atom™, Pentium®, and Celeron® Processors





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Preface

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Revision History

Revision	Description	Date	By
1.0	Initial release	2018-03-02	DA

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1. Introduction

The Q7-AL Computer-On-Module (COM) combines the QSeven® 2.1 standard with the Intel® (“Apollo Lake”) Atom E-series and Pentium® and Celeron® N-series System-on-Chips (SoCs), providing ideal solutions for low power consumption and high pin/area density requirements. The module provides the high integration, high performance, low power, and ruggedness favored by Internet-of-Things (IoT) applications such as retail transactional clients, digital signage, and in-vehicle infotainment systems.

The QSeven form factor affords a more compact profile and footprint than the other COM platforms. With mechanical dimensions of 70mm width, 70mm length, and 2.3mm of overall height, Qseven ranks as one of the smallest COM standards currently available.

The Q7-AL utilizes the upgrades in Intel’s latest (“Apollo Lake”) N-series and E-series SoCs such as the Intel 64 Architecture (“Goldmont”), the new HD graphics 500/505 engine (Gen-9), and a faster, 4-vector image processing unit. The SoCs are manufactured on Intel’s industry-leading, tri-gate 14nm process, improving system performance by supporting up to 8GB of system memory. Compared to the previous generation (“Braswell”), the Apollo Lake SoC comes with a larger package size (24x31mm^2) and pin count (1296 pins) and has updated the OS support by adding Windows 10 IOT and removing support for Windows7/8.1 and WEC7/2013. Because Apollo Lake has more I/O interfaces than Braswell, no pin compatibility exists between these two generations of SoCs.

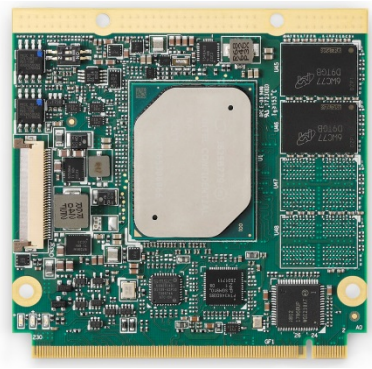
New Intel SoC features:

- Integrated heat spreader on Atom E3950, E3940 and E3930
- Extended temperature SKUs (-40°C to +85°C)
- Windows 10 IOT support
- Gen-9 graphics engine with 18 execution units
- Up to 4-vector-unit image processing unit
- Up to 15 simultaneous 1080p30 decode streams
- Memory bandwidth increase to 38.4 GB/s
- 4K display resolution with 60Hz
- 4K video encode
- Embedded Apollo Lake-I and Apollo Lake have 15-year Intel support lifecycle

The Qseven module primarily targets embedded intelligent systems used in several vertical market segments such as healthcare, industrial controllers and real-time systems, gaming devices, retail systems, edge IoT gateways, in-vehicle infotainment systems, printers, thin clients, industrial and ruggedized tablets, and many others. The Q7-AL supports contemporary, high-bandwidth interfaces such as Ultra HD HDMI, dual-channel LVDS, PCI Express Gen2, Gigabit Ethernet, USB 2.0/3.0, SATA Gen3, two MIPI CSI cameras, and a state-of-the-art HD audio interface. The module generates its own LVDS (18/24bit), TMDS, and DisplayPort++ video signals using eDP and DDI output from the SoC.

Two SPI Flash chips implement a fail-safe BIOS, allowing the user to boot the module even if current BIOS settings have corrupted the system. Other storage devices on the board include an optional eMMC NAND Flash device and an optional SATA SSD.

Under the management of the BMC (Board Management Controller), the SEMA (Smart Embedded Management Agent) utility provides system control, security, and failure protection—counting, monitoring, and measuring hardware and software events, and using the SMBus to send corrective commands to the SoC.





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2. Specifications

2.1. Core System

CPU	**Intel® Atom™ E39xx, Pentium® N4200, and Celeron® N3350, x86 dual-core or quad-core SoCs (System on Chips) with integrated memory, graphics, and I/O (formerly 'Apollo Lake')** • Atom E3950 Quad-Core; 12W TDP; 1.6 GHz base freq; 2.0 GHz burst freq; up to 2400 MT/s; 500MHz graphics base freq; 650MHz graphics burst freq • Atom E3940 Quad-Core; 9.5W TDP; 1.6 GHz base freq; 1.8 GHz burst freq; up to 2133 MT/s; 400MHz graphics base freq; 600MHz graphics burst freq • Atom E3930 Dual-Core; 6.5W TDP; 1.3 GHz base freq; 1.8 GHz burst freq; up to 2133 MT/s; 400MHz graphics base freq; 550MHz graphics burst freq • Pentium N4200 Quad-Core; 6W TDP; 1.1 GHz base freq; 2.5 GHz burst freq; up to 2400 MT/s; 200MHz graphics base freq; 750MHz graphics burst freq • Celeron N3350 Dual-Core; 6W TDP; 1.1 GHz base freq; 2.4 GHz burst freq; up to 2400 MT/s; 200MHz graphics base freq; 650MHz graphics burst freq **Support**: Intel VT-x, VT-d, Intel TXT, Intel SSE4.2, Intel 64 Architecture, Intel Turbo Boost Technology 2.0, Intel AES-NI, and PCLMULQDQ Instruction DRNG **Note:** Availability of features may vary between processor SKUs. Only Atom SKUs can support extreme temperature operating range.
Cache	2MB L2 for all SKUs
Memory	Dual channel non-ECC 2133/2400 MHz LPDDR4 memory; up to 8 GB soldered SDRAM
BIOS	AMI EFI, 16MB SPI BIOS with CMOS backup

2.2. Expansion Busses

PCI Express	4x PCI Express x1 Gen2 : Lanes 0/1/2/3, support up to 5 GT/s signal rate
Other	• LPC bus • SMBus (system) • I^2C (user)

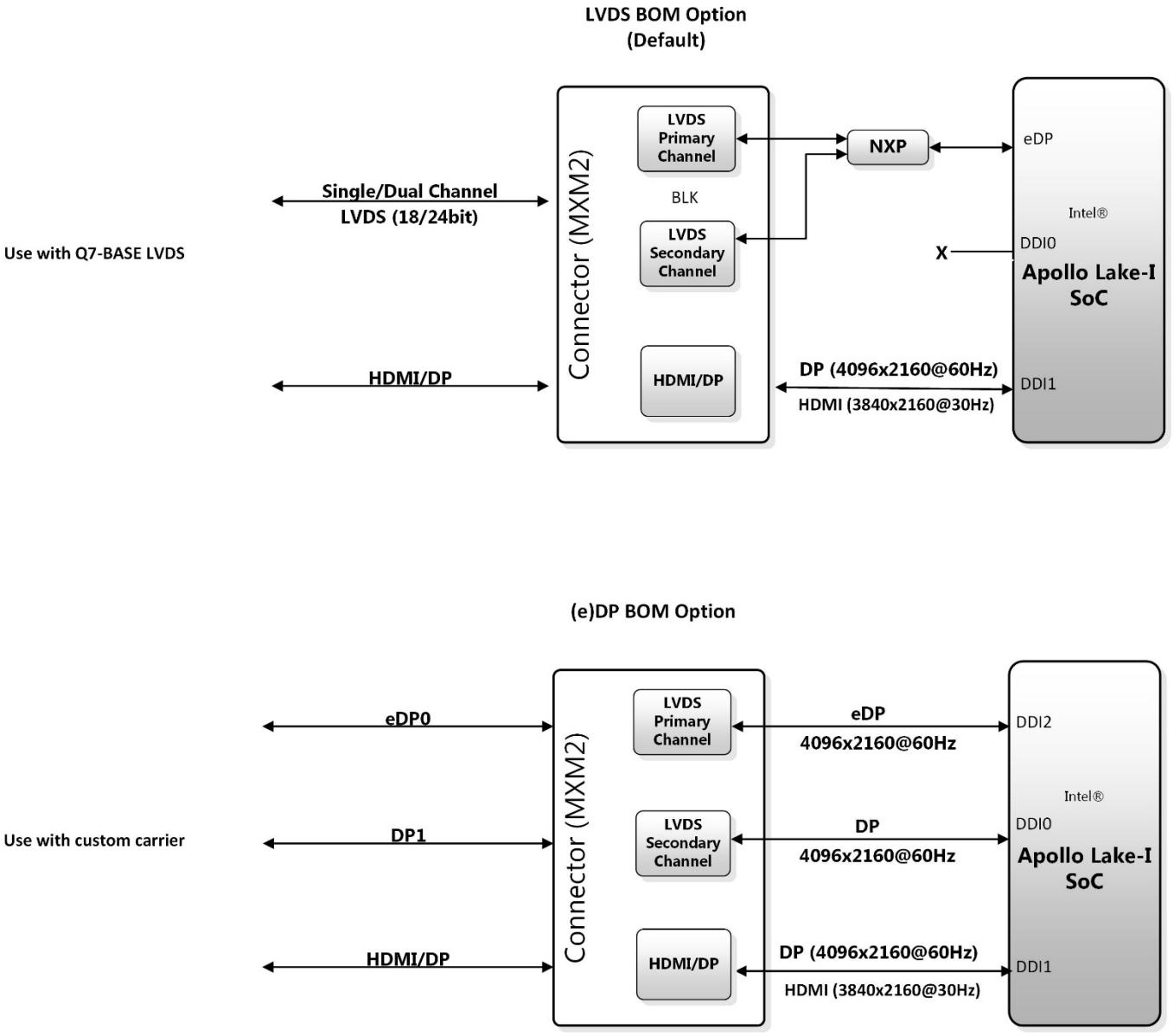
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2.3. Video

Integrated on Processor	Intel 9th Generation Low Power Graphics core architecture (Intel HD Graphics 500/505)
GPU Feature Support	• 2 to 3 independent and simultaneous display combinations of DisplayPort, HDMI, LVDS and eDP • Encode/transcode HD content • Playback of high definition content including Blu-ray Disc • Playback of Blu-ray disc S3D content using HDMI (1.4a spec compliant with 3D) • DirectX Video Acceleration (DXVA2) support for accelerated video processing • AVC/VC1/MPEG2/HEVC/VP8/JPEG HW decode • AVC/MPEG2/HEVC/VP8/JPEG HW encode • Advanced Scheduler 2.0, 1.0, XPDM support • DirectX 12, OpenGL 4.3, OpenGL ES 3.0 and OpenCL 2.0 • Multi Display Support: 3 independent displays **Note:** Availability of features may vary between processor SKUs.
Display Types	• Single/dual channel 18/24-bit LVDS via eDP-to-LVDS chip from DDI2, supporting DE mode and H/V-Sync mode display. Resolutions up to 1920x1200 with dual channel LVDS. • With eDP-to-LVDS chip removed (build option): eDP (4096x2160@60Hz) at LVDS primary channel pins from DDI2 and DP (4096x2160@60Hz) at LVDS secondary channel pins from DDI0. Requires compatible carrier board. • DisplayPort (4096x2160@60Hz)/HDMI (3840x2160@30Hz) from DDI1 **Note:** Supports HDMI 1.4b, DP 1.2a and eDP 1.3.

The figure below illustrates the default (LVDS) build configuration and the alternative (e)DP configuration:

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2.4. Audio

Integrated	Intel® HD Audio integrated on SoC
Codec	Located on carrier Q7-BASE (ALC886 standard support)

2.5. LAN

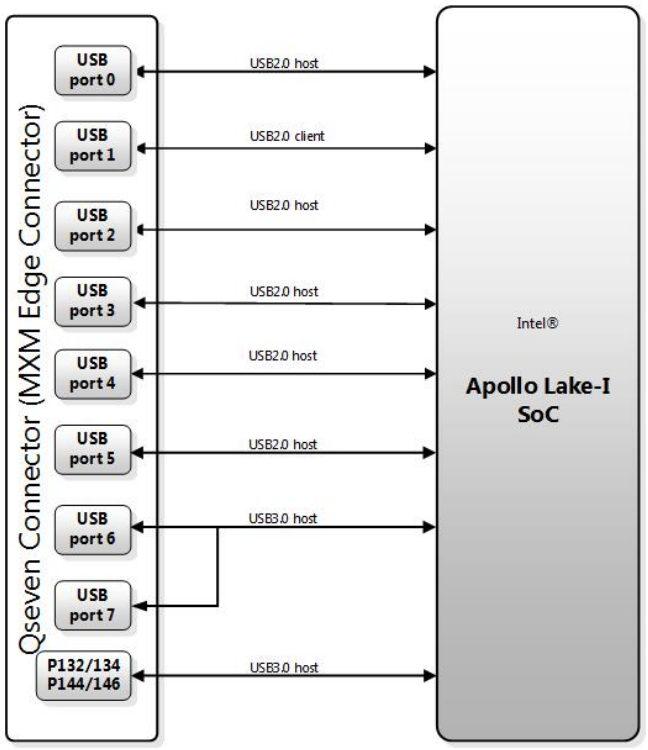
Integrated	MAC integrated on SoC
Intel PHY	Intel® Ethernet Controller I210-IT or I211-IT
Interface	10/100/1000 Mbit/s connection

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2.6. Multi I/O and Storage

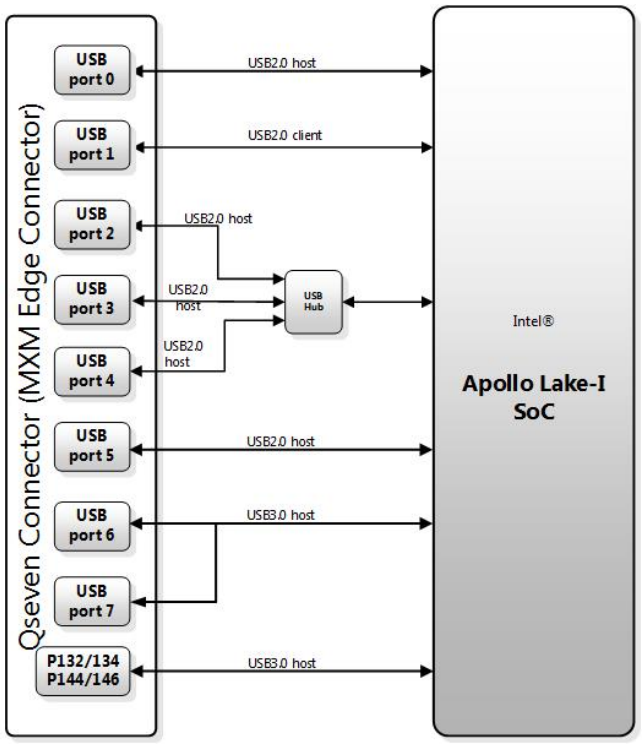
I/O Hub	Integrated on SoC
USB	2x USB 3.0 hosts (USB 6,7) and 6x USB 2.0 ports (USB 0,1,2,3,4,5 [1x client and 5x Host]) All USBs supported by XHCI controller
SATA	2x SATA 6Gb/s ports (1x used for optional SATA SSD)
GPIO	8 GPIO from BMC multiplexed with LPC from SoC (build option)

Q7-AL supports a standard USB topology as shown in the figure below:



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As a build option it can also be provided including a USB hub:



2.7. Serial I/O on Module

- **Chipset:** Embedded in SoC
- **Ports:** 1x UART Rx/Tx only, the bit rate can support up to 115.2k bps
- **Console Redirection:** selectable in BIOS, supported during BIOS POST

2.8. SEMA Board Controller

- **Type:** ADLINK Smart Embedded Management Agent (SEMA)
- **Functions:**
  - Voltage/Current monitoring
  - Power sequence debug support
  - AT/ATX mode control
  - Logistics and forensic information
  - Flat panel control
  - General purpose I2C
  - Failsafe BIOS (dual BIOS)
  - Watchdog timer and fan control

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2.9. Debug

- 40-pin flat cable connector to be used with DB-40 debug module
  Supports: BIOS POST code LED, BMC access, SPI BIOS flashing, power testpoints, debug LEDs

2.10. Power Specifications

Power Modes	AT and ATX mode (AT mode startup controlled by SEMA Board Controller)
Standard Voltage Input	+5V±5% / 5Vsb ±5%
Wide Voltage Input	ATX: 5V / 5Vsb ±5% or AT: 5V ±5%
Power Management	ACPI 5.0 compliant; Smart Battery support
Power States	Supports C1-C2, S0, S3, S4, S5 (Wake-on-USB S3/S4, WoL S3/S4/S5)
ECO Mode	Supports deep S5 for 5Vsb power saving

2.11. Power Consumption

Parameter	**12W, E3950 Atom SoC**	**9W, E3940 Atom SoC**	**6W, E3930 Atom SoC**	**6W, N4200 Pentium SoC**	**6W, N3350 Celeron SoC**
Input Type	Regulated DC Voltage	Regulated DC Voltage	Regulated DC Voltage	Regulated DC Voltage	Regulated DC Voltage
Typical Idle Mode Current and Power (EIST enabled; 240GB SSD; under Windows 10 Enterprise)	0.33A (1.65W) @ 5V	N/A on DVT Report	0.32A (1.60W) @ 5V	N/A on DVT Report	0.34A (1.70W) @ 5V
Typical Operating Mode Current and Power (EIST enabled; 240GB SSD; under Windows 10 Enterprise)	2.4A (12.00W) @ 5V	N/A on DVT Report	1.70A (8.50W) @ 5V	N/A on DVT Report	2.30A (11.50W) @ 5V
Maximum Operating Mode Current and Power (EIST enabled; 240GB SSD; under Windows 10 Enterprise; Intel TAT tool v6.10.13)	3.4A (17.00W) @ 5V	N/A on DVT Report	2.10A (10.50W) @ 5V	N/A on DVT Report	3.20A (16.00W) @ 5V
System S3 mode (240 GB SSD; under Windows 10 Enterprise	0.08A (0.40W) @ 5VSB	N/A on DVT Report	0.08A (0.40W) @ 5VSB	N/A on DVT Report	0.09A (0.45W) @ 5VSB

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Parameter	12W, E3950 Atom SoC	9W, E3940 Atom SoC	6W, E3930 Atom SoC	6W, N4200 Pentium SoC	6W, N3350 Celeron SoC
System S4 mode (240 GB SSD; under Windows 10 Enterprise	0.04A (0.20W) @ 5VSB	N/A on DVT Report	0.04A (0.20W) @ 5VSB	N/A on DVT Report	0.05A (0.25W) @ 5VSB
System S5 mode with ECO enabled (240 GB SSD; under Windows 10 Enterprise	0.01A (0.05W) @ 5VSB	N/A on DVT Report	0.01A (0.05W) @ 5VSB	N/A on DVT Report	0.01A (0.05W) @ 5VSB

2.12. Operating Temperatures

Standard Operating Temperature	0°C to +60°C Storage: -20°C to +70°C
Extreme Rugged Operating Temperature (optional)	-40°C to +85°C Storage: -40°C to +85°C

2.13. Environmental

Humidity	**Operating: 5-90% RH, non-condensing** **Storage: 5-95% RH (and operating with conformal coating)**
Shock and Vibration	IEC 60068-2-64 and IEC-60068-2-27 MIL-STD-202F, Method 213B, Table 213-I, Condition A and Method 214A, Table 214-I, Condition D
HALT	Thermal Stress, Vibration Stress, Thermal Shock and Combined Test
MTBF	• Mean Time Between Failures: 346,394 hours @ 40°C ambient (according to MIL calculation) based on actual calculated derating • Mean Time Between Failures: 89,314 hours @ 85°C ambient (according to MIL calculation) based on actual calculated derating

2.14. Specification Compliance

- SGET (Standardization Group for Embedded Technologies) Qseven: Rev 2.1; Small size 70 x 70 mm

2.15. Operating Systems

Standard Support	**Windows 10 IOT Enterprise (64-bit)** **Windows 10 IOT Core (32/64-bit)** **Yocto Linux (64-bit)**
Extended Support (BSP)	VxWorks 7.0

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2.16. Functional Diagram

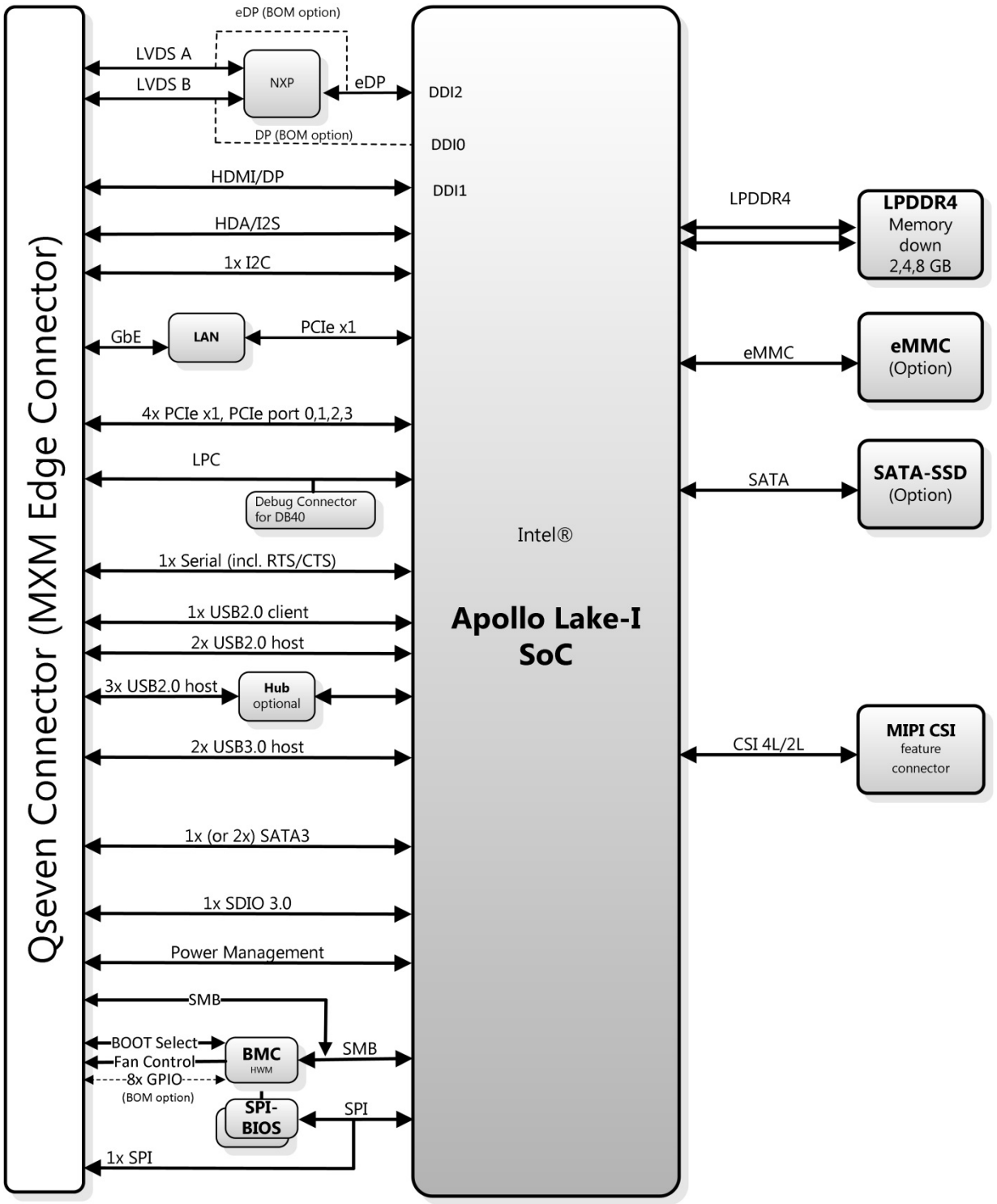
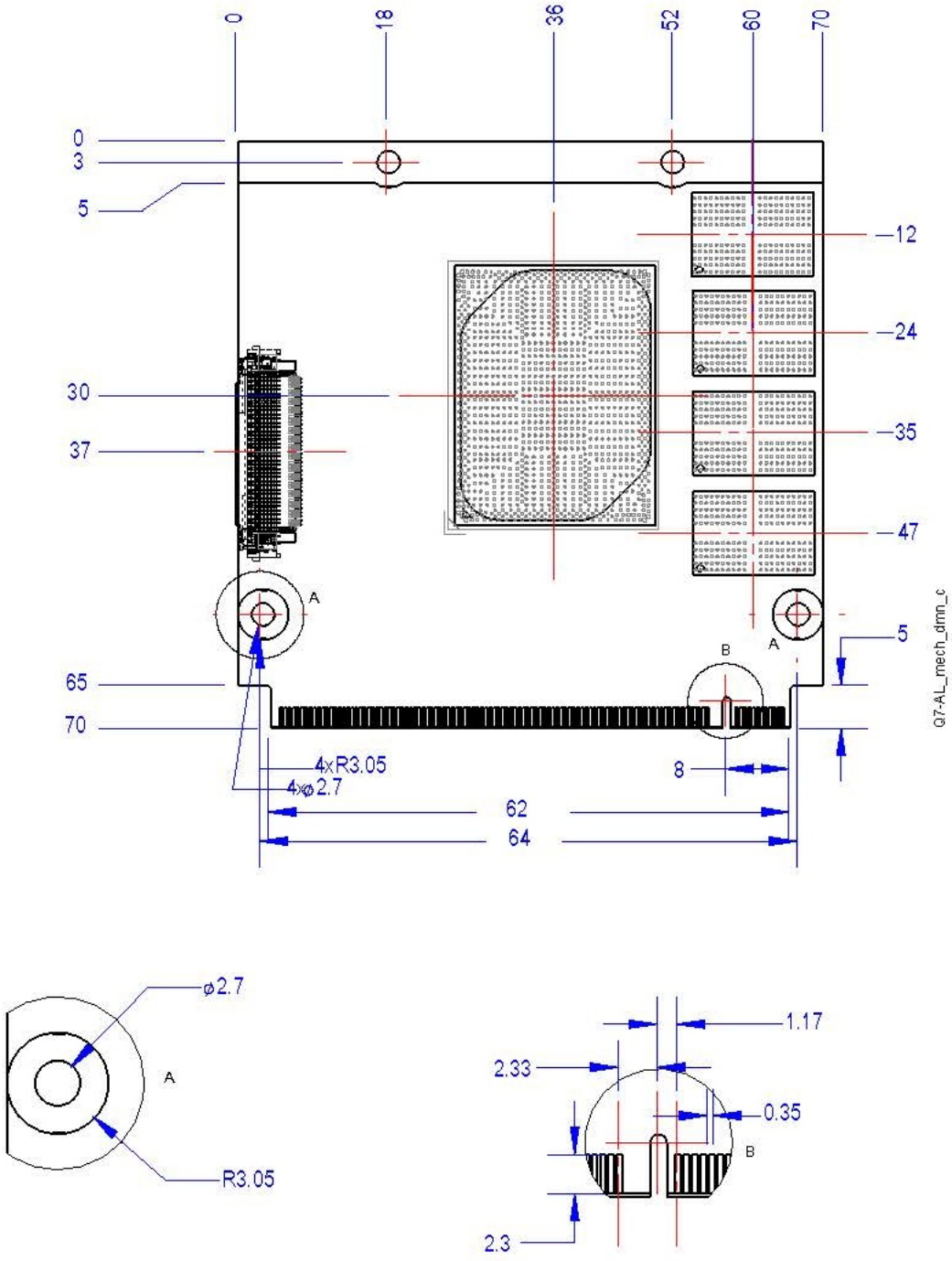


Figure 1: Q7-AL Functional Block Diagram

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2.17. Mechanical Drawing



All are dimensions shown in millimeters.

Tolerances should be ± 0.25mm, unless otherwise noted.

Figure 2: Q7-AL Mechanical Drawing

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2.18. Q7-AL Heatspreaders

The Q7-AL is designed to operate at its maximum CPU speed and requires a thermal solution to cool the CPU. ADLINK offers two passive heatsinks, one active heatsink, and two heat spreaders for cooling. Each Q7-AL module requires one of the three heatsinks (either the Q7-AL-HS3, Q7-AL-HS4, or the Q7-AL-HS5) or one of two heat spreaders (either the Q7-AL-HS1 or the Q7-AL-HS2) depending on the featured CPU (HS1 for E-series or HS2 for N-series). The heat spreaders must be combined with additional forms of cooling such as active heatsinks. The Q7-AL-HS3 active heatsink must be combined with one of the two heat spreaders (Q7-AL-HS1 or Q7-AL-HS2).

2.18.1. The Q7-AL-HS1 heat spreader must be used for the Q7-AL-E3950/40/30 modules. As can be seen in Figure-1, the Intel Atom E39xx SoCs come with mounted Intel heat spreaders, which look like metallic lids and add 2mm to the heights of the SoCs. The Q7-AL-HS1 heat spreader is designed for the extra heights of these SoCs. See the following diagram for a mechanical overview of the Q7-AL-HS1 heat spreader.

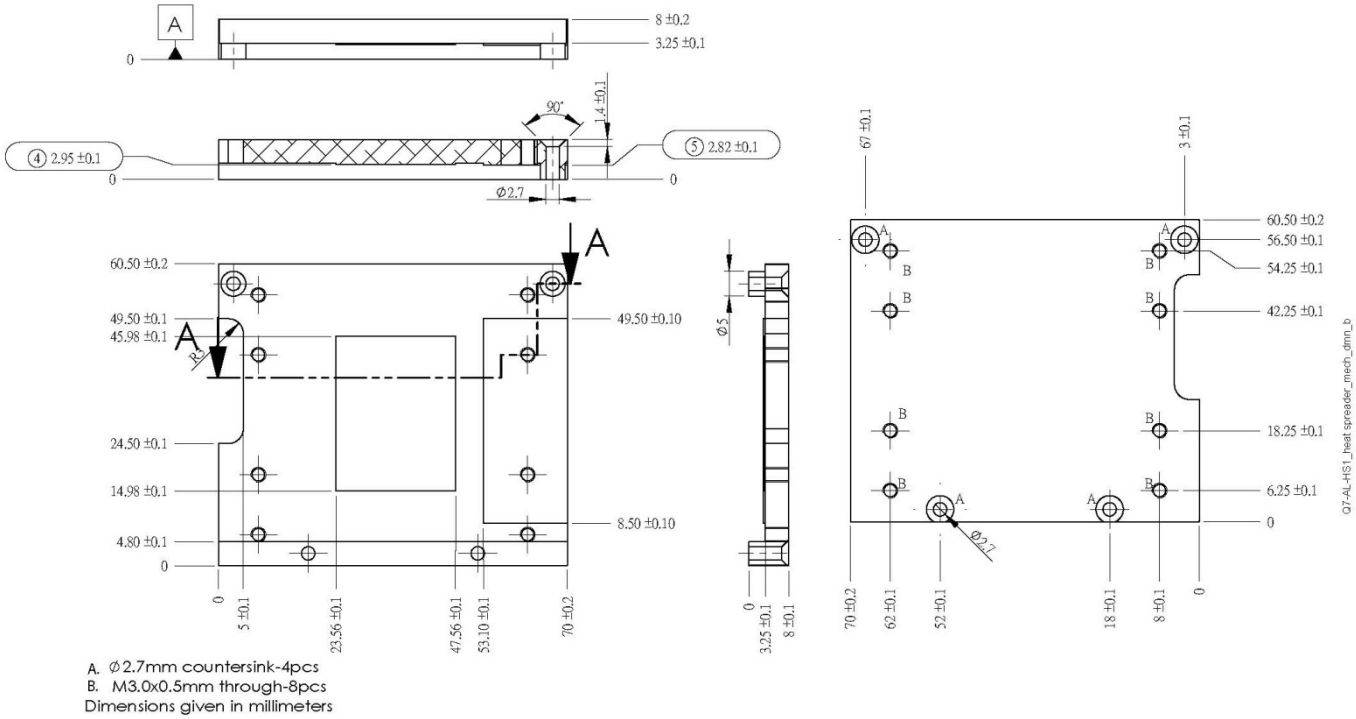


Figure 3: Q7-AL-HS1 Heat Spreader Mechanical Drawing

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2.18.2. The Q7-AL-HS2 heat spreader is designed for the Q7-AL-N4200/N3350 modules and must be used for these lower profile SoCs. As can be seen in Figure-1, the Intel Pentium and Celeron N4200/N3350 SoCs come without mounted Intel heat spreaders, and their profiles are 2mm lower than the Atom E39xx SoCs. See the following diagram for a mechanical overview of the Q7-AL-HS2 heat spreader.

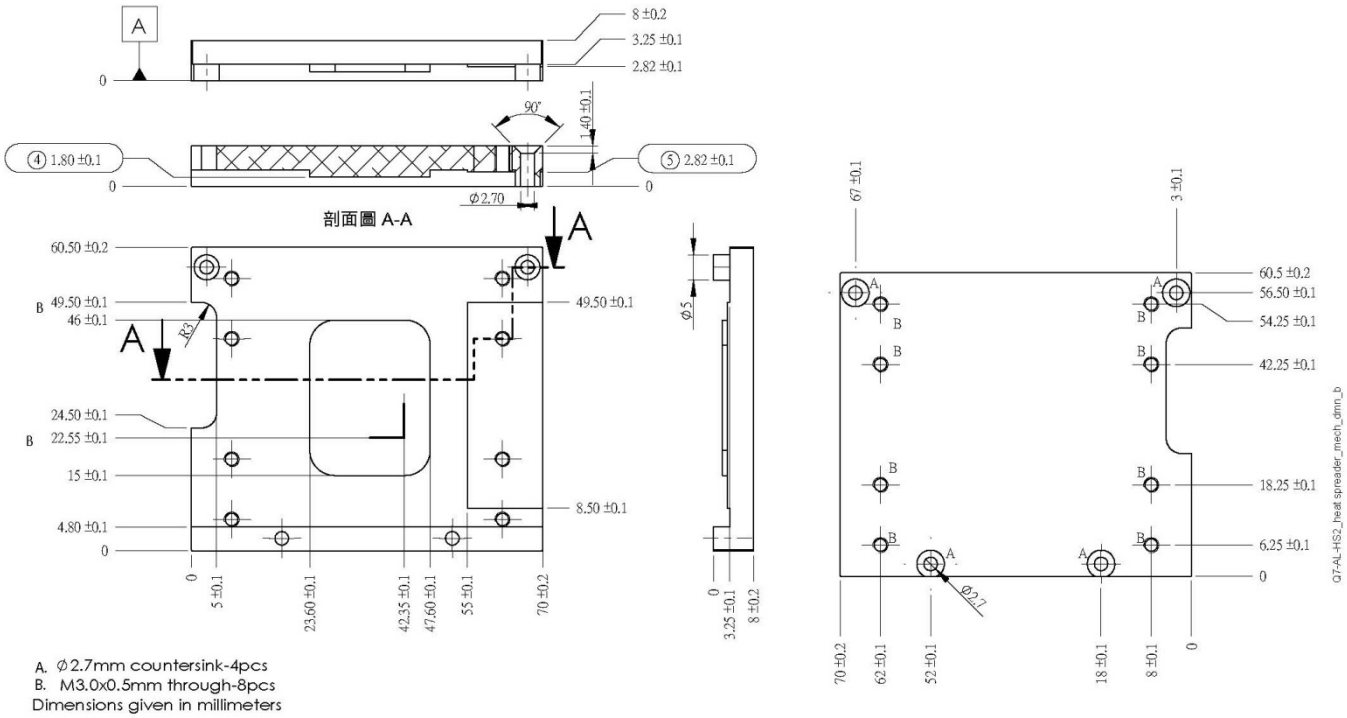


Figure 4: Q7-AL-HS2 Heat Spreader Mechanical Drawing

2.18.3. The Q7-AL-HS-4 passive heatsink must be used for the Q7-AL-E3950/40/30 modules. As can be seen in Figure-1, the Intel Atom E39xx SoCs come with mounted Intel heat spreaders, which look like metallic lids and add 2mm to the heights of the SoCs. The Q7-AL-HS-4 passive heatsink is designed for the extra heights of these SoCs. See the following diagram for a mechanical overview of the Q7-AL-HS-4 passive heatsink.

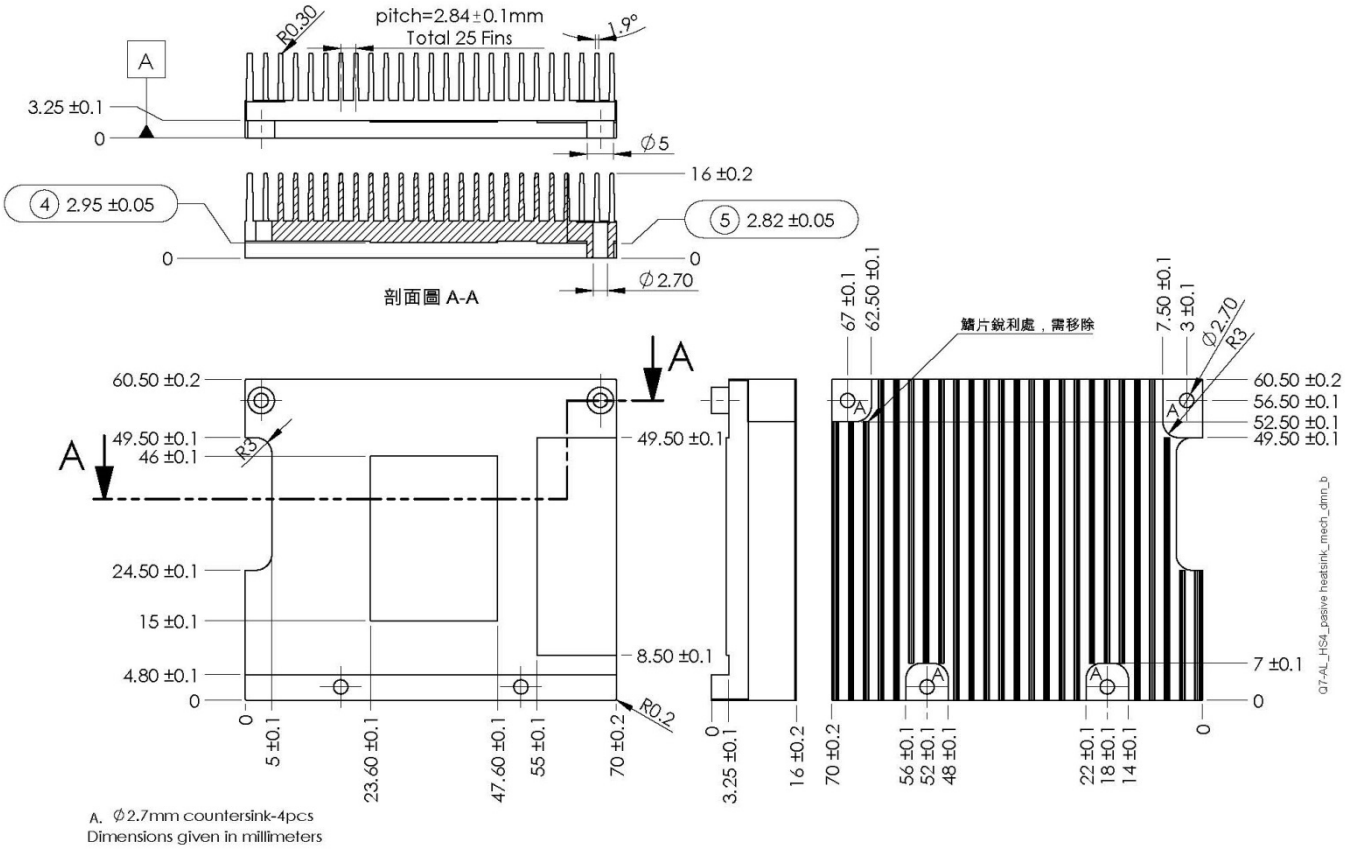


Figure 5: Q7-AL-HS4 Passive Heatsink Mechanical Drawing

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2.18.4. The Q7-AL-HS-5 passive heatsink is designed for the Q7-AL-N4200/N3350 modules and must be used for these lower profile SoCs. As can be seen in Figure-1, the Intel Pentium and Celeron N4200/N3350 SoCs come without mounted Intel heat spreaders, and their profiles are 2mm lower than the Atom E39xx SoCs. See the following diagram for a mechanical overview of the Q7-AL-HS-5 passive heatsink.

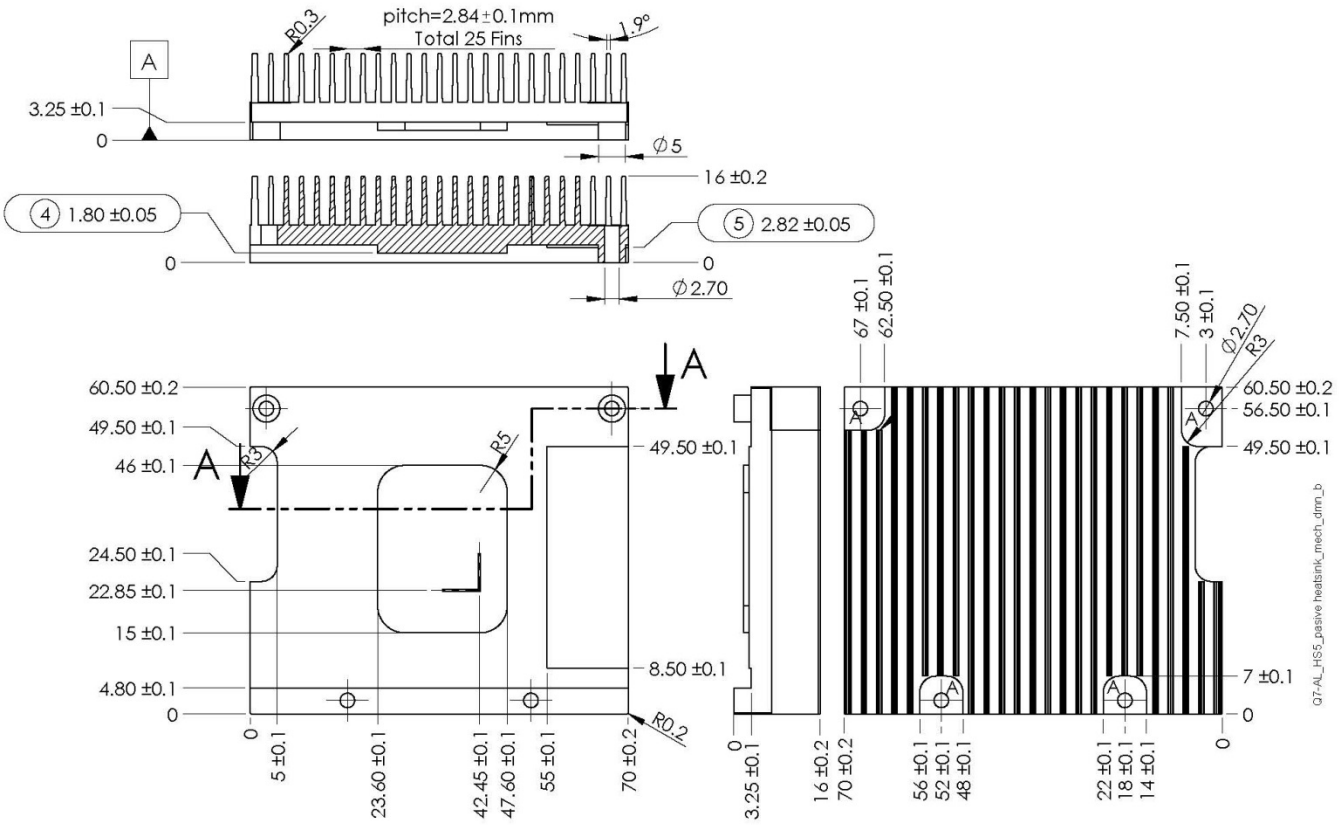
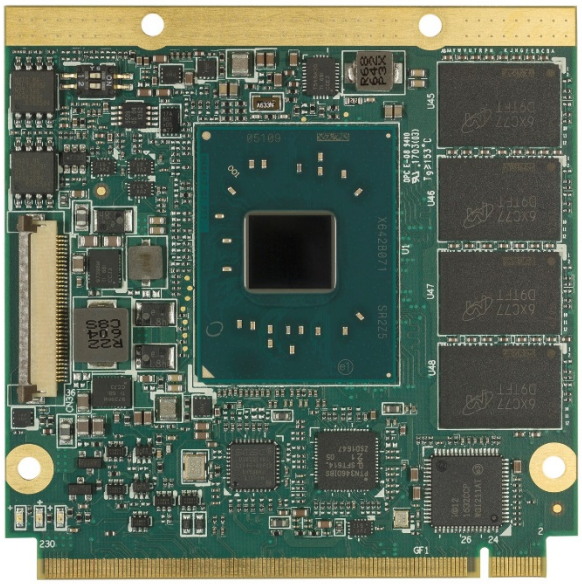
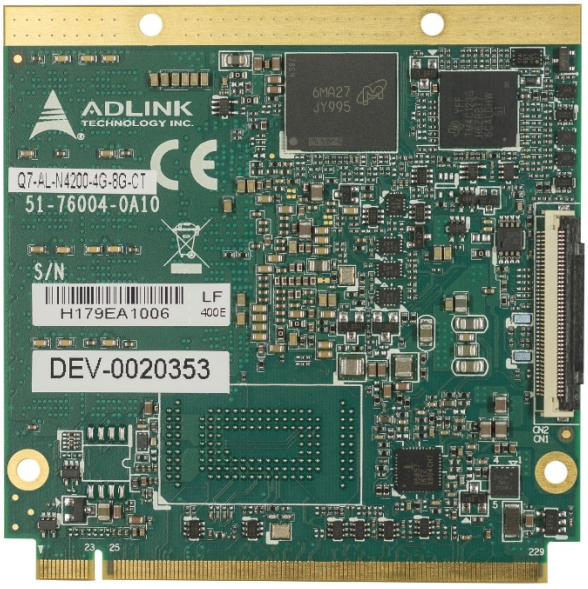


Figure 6: Q7-AL-HS5 Passive Heatsink Mechanical Drawing

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2.19. Q7-AL Top View and Bottom View





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3. Pinouts and Signal Descriptions

3.1. Primary/Secondary Pin Definitions

The Q7-AL is a Qseven 2.1 compliant module supporting some of the options of the specification. All pins in the Qseven 2.1 specification are described, including those not supported on the Q7-AL. Those not supported on the Q7-AL module are ~~crossed out~~.

Table 1: Q7-AL Primary/Secondary Pin Definitions

Primary side (BOTTOM)			**Secondary side (TOP)**		
Pin#	Signal	PU/PD	Pin#	Signal	PU/PD
1	GND		2	GND	
3	GBE_MDI3-		4	GBE_MDI2-	
5	GBE_MDI3+		6	GBE_MDI2+	
7	GBE_LINK100#		8	GBE_LINK1000#	
9	GBE_MDI1-		10	GBE_MDI0-	
11	GBE_MDI1+		12	GBE_MDI0+	
13	GBE_LINK#		14	GBE_ACT#	
15	GBE_CTREF		16	SUS_S5#	
17	WAKE#		18	SUS_S3#	
19	GPO0		20	PWRBTN#	
21	SLP_BTN# ~~/GPII1~~		22	LID_BTN# ~~/ GPII0~~	
23	GND		24	GND	
Key			Key		
25	GND		26	PWGIN	
27	BATLOW#~~/GPII2~~		28	RSTBTN#	
29	SATA0_TX+		30	SATA1_TX+	
31	SATA0_TX-		32	SATA1_TX+	
33	SATA_ACT#		34	GND	
35	SATA0_RX+		36	SATA1_RX+	
37	SATA0_RX-		38	SATA1_RX-	
39	GND		40	GND	
41	BIOS_DISABLE#~~/BOOT_ALT#~~		42	SDIO_CLK#	
43	SDIO_CD#		44	Reserved	
45	SDIO_CMD		46	SDIO_WP	
47	SDIO_PWR#		48	SDIO_DAT1	
49	SDIO_DAT0		50	SDIO_DAT3	
51	SDIO_DAT2		52	Reserved	
53	Reserved		54	Reserved	

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Primary side (BOTTOM)			Secondary side (TOP)		
55	Reserved		56	USB_OTG_VBUS	
57	GND		58	GND	
59	HDA_SYNC /I2S_WS		60	SMB_CLK ~~/GP1_I2C_CLK~~	
61	HDA_RST# /I2S_RST#		62	SMB_DAT ~~/GP1_I2C_DAT~~	
63	HDA_BITCLK /I2S_CLK		64	SMB_ALERT#	
65	HDA_SDI /I2S_SDI		66	GP0_I2C_CLK	
67	HDA_SDO /I2S_SDO		68	GP0_I2C_DAT	
69	THRM#		70	WDTRIG#	
71	THRMTRIP#		72	WDOUT	
73	GND		74	GND	
75	U3_USB1_TX_N ~~USB_P7-~~ ~~/USB_SSTX0-~~		76	U3_USB1_RX_N ~~USB_P6-~~ ~~/USB_SSRX0-~~	
77	U3_USB1_TX_P ~~USB_P7+/USB_SSTX0+~~		78	U3_USB1_RX_P ~~USB_P6+/USB_SSRX0+~~	
79	USB_OC1# ~~USB_6_7_OC#~~		80	USB_OC1# ~~USB_4_5_OC#~~	
81	U2_USB4_N ~~USB_P5-~~ ~~/USB_SSTX2-~~		82	U2_USB5_N ~~USB_P4-~~ / ~~USB_SSRX1-~~	
83	U2_USB4_P ~~USB_P5+/USB_SSTX2+~~		84	U2_USB5_P ~~USB_P4+~~ / ~~USB_SSRX1+~~	
85	USB_OC0# ~~USB_2_3_OC#~~		86	USB_OC0# ~~USB_0_1_OC#~~	
87	U2_USB3_N ~~USB_P3-~~		88	U2_USB2_N ~~USB_P2-~~	
89	U2_USB3_P ~~USB_P3+~~		90	U2_USB2_P ~~USB_P2+~~	
91	USB_VBUS		92	USB_OTG_ID ~~USB_ID~~	
93	U2_USB_OTG_N ~~USB_P1-~~		94	U2_USB1_N ~~USB_P0-~~	
95	U2_USB_OTG_P ~~USB_P1+~~		96	U2_USB1_P ~~USB_P0+~~	
97	GND		98	GND	
99	eDP0_TX0+ / LVDS_A0+ [LVDS Default]		100	DDI0_TX0+ ~~eDP1_TX0+~~ / LVDS_B0+ [LVDS Default]	
101	eDP0_TX0- / LVDS_A0-		102	DDI0_TX0- ~~eDP1_TX0-~~ / LVDS_B0-	

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Primary side (BOTTOM)			Secondary side (TOP)		
	[LVDS Default]			[LVDS Default]	
103	eDP0_TX1+ / LVDS_A1+ [LVDS Default]	PU, 470k, V1P8S	104	DDI0_TX1+ ~~eDP1_TX1+~~ / LVDS_B1+ [LVDS Default]	
105	eDP0_TX1- / LVDS_A1- [LVDS Default]	PU, 470k, V1P8S	106	DDI0_TX1- ~~eDP1_TX1-~~ / LVDS_B1- [LVDS Default]	
107	eDP0_TX2+ / LVDS_A2+ [LVDS Default]	PU, 470k, V1P8S	108	DDI0_TX2+ ~~eDP1_TX2+~~ / LVDS_B2+ [LVDS Default]	
109	eDP0_TX2- / LVDS_A2- [LVDS Default]	PU, 470k, V1P8S	110	DDI0_TX2- ~~eDP1_TX2-~~ / LVDS_B2- [LVDS Default]	
111	LVDS_3P3_VDD_EN ~~LVDS_PPEN~~	PU, 470k, V1P8S	112	LVDS_3P3_BKLT_EN ~~LVDS_BLEN~~	
113	eDP0_TX3+ / LVDS_A3+ [LVDS Default]	PU, 470k, V1P8S	114	DDI0_TX3+ ~~eDP1_TX3+~~ / LVDS_B3+ [LVDS Default]	
115	eDP0_TX3- / LVDS_A3- [LVDS Default]	PU, 470k, V1P8S	116	DDI0_TX3- ~~eDP1_TX3-~~ / LVDS_B3- [LVDS Default]	
117	GND		118	GND	
119	eDP0_AUX+ / LVDS_A_CLK+ [LVDS Default]		120	DDI0_AUX_P ~~eDP1_AUX+~~ / LVDS_B_CLK+ [LVDS Default]	
121	eDP0_AUX- / LVDS_A_CLK- [LVDS Default]		122	DDI0_AUX_N ~~eDP1_AUX-~~ / LVDS_B_CLK-	
123	LVDS_3P3 _BKLT_CTRL ~~/GP_PWM_OUT0~~		124	GP_1-Wire_Bus/ ~~HDMI_CEC~~	
125	3P3V_LVDS_DDC_DAT ~~GP2_I2C_DAT/LVDS_DID_DAT~~		126	eDP0_HPD# / ~~LVDS_BLC_DAT~~	
127	3P3V_LVDS_DDC_CLK ~~GP2_I2C_DAT/LVDS_DID_DAT~~		128	eDP1_HPD# / ~~LVDS_BLC_CLK~~	
129	~~CAN0_TX~~		130	~~CAN0_RX~~	
131	DP_LANE3+ / TMDS_CLK+		132	U3_USB0_TX_N ~~USB_SSTX1-~~	
133	DP_LANE3- / TMDS_CLK-		134	U3_USB0_TX_P ~~USB_SSTX1+~~	
135	GND		136	GND	

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Primary side (BOTTOM)			Secondary side (TOP)		
137	DP_LANE1+ / TMDS_LANE1+		138	DP_AUX+	
139	DP_LANE1- / TMDS_LANE1-		140	DP_AUX-	
141	GND		142	GND	
143	DP_LANE2+ / TMDS_LANE0+		144	U3_USB0_RX_N ~~USB_SSRX1-~~	
145	DP_LANE2- / TMDS_LANE0-		146	U3_USB0_RX_P ~~USB_SSRX1+~~	
147	GND		148	GND	
149	DP_LANE0+ / TMDS_LANE2+		150	HDMI_CTRL_DAT	
151	DP_LANE0- / TMDS_LANE2-		152	HDMI_CTRL_CLK	
153	DP_HDMI_HPD#		154	DP_HPD#	
155	PCIE_CLK_REF+		156	PCIE_WAKE#	
157	PCIE_CLK_REF-		158	PCIE_RST#	
159	GND		160	GND	
161	PCIE3_TX+		162	PCIE3_RX+	
163	PCIE3_TX-		164	PCIE3_RX-	
165	GND		166	GND	
167	PCIE2_TX+		168	PCIE2_RX+	
169	PCIE2_TX-		170	PCIE2_RX-	
171	UART0_TX		172	UART0_RTS#	
173	PCIE1_TX+		174	PCIE1_RX+	
175	PCIE1_TX-		176	PCIE1_RX-	
177	UART0_RX		178	UART0_CTS#	
179	PCIE0_TX+		180	PCIE0_RX+	
181	PCIE0_TX-		182	PCIE0_RX-	
183	GND		184	GND	
185	LPC_AD0/GPIO0		186	LPC_AD1 / GPIO1	
187	LPC_AD2/GPIO2		188	LPC_AD3 / GPIO3	
189	LPC_AD4 /GPIO4		190	LPC_FRAME# / GPIO5	
191	LPC_SERIRQ /GPIO6		192	LPC_LDRQ# / GPIO7	
193	VCC_RTC		194	SPKR ~~/ GP_PWM_OUT2~~	
195	BMC_TACHIN ~~/GP_TIMER_IN~~		196	~~FAN_PWMOUT /~~ BMC_PWM_OUT	
197	GND		198	GND	
199	SPI_MOSI		200	SPI_CS0#	

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Primary side (BOTTOM)			Secondary side (TOP)		
201	SPI_MISO		202	SPI_CS1#	
203	SPI_SCK		204	~~MFG_NC4~~	
205	VCC_5V_SB		206	VCC_5V_SB	
207	~~MFG_NC0~~		208	~~MFG_NC2~~	
209	~~MFG_NC1~~		210	~~MFG_NC3~~	
211	NC		212	NC	
213	NC		214	NC	
215	NC		216	NC	
217	NC		218	NC	
219	VCC		220	VCC	
221	VCC		222	VCC	
223	VCC		224	VCC	
225	VCC		226	VCC	
227	VCC		228	VCC	
229	VCC		230	VCC	

Notes:

(1) eDP is available as a build option in place of LVDS.

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3.2. Signal Description Terminology

The following terms are used in the Qseven Signal Descriptions below.

I	Input to the Module
O	Output from the Module
I/O	Bi-directional input/output signal
OD	Open drain output
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I/O 3.3Vsb	Input 3.3V tolerant active in standby state
P	Power Input/Output
REF	Reference voltage output that may be sourced from a module power plane.
PDS	Pull-down strap. This is an output pin on the module that is either tied to GND or not connected. The signal is used to indicate the PICMG module type to the Carrier Board.
PU	ADLINK implemented pull-up resistor on module
PD	ADLINK implemented pull-down resistor on module

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3.3. Qseven Signal Descriptions

3.3.1. Gigabit Ethernet

Gigabit Ethernet	Pin	Description	I/O	PU/PD	Comment
GBE0_MDI0+ GBE0_MDI0-	12 10	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Gb_LAN		Twisted pair signals for external transformer
GBE0_MDI1+ GBE0_MDI1-	11 9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	I/O Gb_LAN		Twisted pair signals for external transformer
GBE0_MDI2+ GBE0_MDI2-	6 4	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Gb_LAN		Twisted pair signals for external transformer
GBE0_MDI3+ GBE0_MDI3-	5 3	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	I/O Gb_LAN		Twisted pair signals for external transformer
GBE0_ACT#	14	Gigabit Ethernet Controller 0 activity indicator, active low.	O 3.3VSB		max 10 mA
GBE0_LINK#	13	Gigabit Ethernet Controller 0 link indicator, active low.	O 3.3VSB		max 10 mA
GBE0_LINK100#	7	Gigabit Ethernet Controller 0 100Mbit/sec link indicator, active low.	O 3.3VSB		max 10 mA
GBE0_LINK1000#	8	Gigabit Ethernet Controller 0 1000Mbit/sec link indicator, active low.	O 3.3VSB		max 10 mA
GBE0_CTREF	15	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be 250 mA or less.	REF		

3.3.2. Serial ATA

Signal	Pin	Description	I/O	PU/PD	Comment
SATA0_TX+ SATA0_TX-	29 31	Serial ATA channel 0, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA0_RX+ SATA0_RX-	35 37	Serial ATA channel 0, Receive Input differential pair.	I SATA		AC coupled on Module
SATA1_TX+ SATA1_TX-	30 32	Serial ATA channel 1, Transmit Output differential pair.	O SATA		AC coupled on Module
SATA1_RX+ SATA1_RX-	36 38	Serial ATA channel 1, Receive Input differential pair.	I SATA		AC coupled on Module
SATA_ACT#	33	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC 3.3V		Max. 10mA

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3.3.3. SDIO

Signal	Pin	Description	I/O	PU/PD	Comment
SDIO_CD#	43	SDIO Card Detect. This signal indicates when an SDIO/MMC card is present.	I/O CMOS 3.3V	PU 100K 3.3V	
SDIO_CLK	42	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs.	O CMOS 3.3V		
SDIO_CMD	45	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	I/O CMOS 3.3V OD/PP		
SDIO_WP	46	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	I/O CMOS 3.3V	PU 100K 3.3V	
SDIO_PWR#	47	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	O CMOS 3.3V	PU 100K 3.3V	
SDIO_DAT0-3	48 (DAT1); 49 (DAT0); 50 (DAT3); 51 (DAT2)	SDIO Data lines. These signals operate in push-pull mode.	I/O CMOS 3.3V PP		

3.3.4. Audio Signals

Signal	Pin	Description	I/O	PU/PD	Comment
HDA_RST# ~~I2S_RST#~~	61	HD Audio Codec Reset. Multiplexed with I2S Codec Reset.	O CMOS 3.3V		
HDA_SYNC ~~I2S_WS~~	59	Serial Bus Synchronization. Multiplexed with I2S Word Select from Codec.	O CMOS 3.3V		
HDA_BITCLK ~~I2S_CLK~~	63	HD Audio 24 MHz Serial Bit Clock from Codec. Multiplexed with I2S Serial Data Clock from Codec.	O CMOS 3.3V		
HDA_SDO ~~I2S_SDO~~	67	HD Audio Serial Data Output to Codec. Multiplexed with I2S Serial Data Output from Codec.	O CMOS 3.3V		
HDA_SDI ~~I2S_SDI~~	65	HD Audio Serial Data Input from Codec. Multiplexed with I2S Serial Data Input from Codec.	I CMOS 3.3V		

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3.3.5. Miscellaneous

Signal	Pin	Description	I/O	PU/PD	Comment
WDTRIG#	70	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse.	I CMOS 3.3V		
WDOUT	72	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be de-asserted by software, system reset or a system power down.	O CMOS 3.3V		
GP0_I2C_CLK	66	General Purpose I²C bus #0 clock line.	I/O CMOS 3.3V	PU 2.2K 3.3V suspend	
GP0_I2C_DAT	68	General Purpose I²C bus #0 data line.	I/O CMOS 3.3VSB	PU 2.2K 3.3V suspend	
SMB_CLK /~~GP1_I2C_CLK~~	60	Clock line of System Management Bus. ~~Multiplexed with General Purpose I²C bus #1 clock line.~~	I/O CMOS 3.3V OD Suspend	PU 4.7K 3.3V	
SMB_DAT /~~GP1_I2C_DAT~~	62	Fan tachometer input for a fan with a two pulse output.	I/O CMOS 3.3V OD Suspend	PU 4.7K 3.3V	
SMB_ALERT#	64	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	I/O CMOS 3.3V OD Suspend	PU 2.2K 3.3V	
SPKR /~~GP_PWM_OUT 2~~	194	Primary functionality is output for audio enunciator, the “speaker” in PC AT systems. ~~When not in use for this primary purpose it can be used as General Purpose PWM Output.~~	O CMOS 3.3V	PU 10K 3.3V	
BIOS_DISABLE # /~~BOOT_ALT#~~	41	Module BIOS disable input signal. Pull low to disable module's on-board BIOS. Allows off-module BIOS implementations. ~~This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a boot loader.~~	I CMOS 3.3V	PU 10K 3.3V suspend	
GP_1-Wire_Bus	124	General Purpose 1-Wire bus interface. Can be used for consumer electronics control bus (CEC) of HDMI	I/O CMOS 3.3V	PU 1K 3.3V	
LID_BTN# /~~GPII0~~	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. Open/Close state may be software configurable.	I CMOS 3.3V Suspend	PU 10K 3.3V	
SLP_BTN# /~~GPII1~~	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.	I CMOS 3.3V Suspend	PU 10K 3.3V	
BATLOW# /~~GPII2~~	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	I CMOS 3.3V Suspend	PU 10K 3.3V	

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Signal	Pin	Description	I/O	PU/PD	Comment
GPO0	19	General Purpose Output 0	O CMOS 3.3V	PU 2.2K 3.3V	

3.3.6. USB

Signal	Pin	Description	I/O	PU/PD	Comment
U2_USB1_P U2_USB1_N	96 94	USB 2.0 differential data pairs for Port 1	I/O 3.3VSB		USB 1.1/ 2.0 compliant
U2_USB2_P U2_USB2_N	90 88	USB 2.0 differential data pairs for Port 2	I/O 3.3VSB		USB 1.1/ 2.0 compliant
U2_USB3_P U2_USB3_N	89 87	USB 2.0 differential data pairs for Port 3	I/O 3.3VSB		USB 1.1/ 2.0 compliant
U2_USB4_P U2_USB4_N	83 81	USB 2.0 differential data pairs for Port 4	I/O 3.3VSB		USB 1.1/ 2.0 compliant
U2_USB5_P U2_USB5_N	84 82	USB 2.0 differential data pairs for Port 5	I/O 3.3VSB		USB 1.1/ 2.0 compliant
U3_USB0_TX_P U3_USB0_TX_N	134 132	USB transmit differential pair for superspeed USB 3.0 port 0	O		USB 3.0 compliant AC coupled -on module
U3_USB0_RX_P U3_USB0_RX_N	146 144	USB receive differential pair for superspeed USB 3.0 port 0	I		USB 3.0 compliant AC coupled close to respective device
U3_USB1_TX_P U3_USB1_TX_N	77 75	USB transmit differential pair for superspeed USB 3.0 port 1	O		USB 3.0 compliant AC coupled -on module
U3_USB1_RX_P U3_USB1_RX_N	78 80	USB receive differential pair for superspeed USB 3.0 port 1	I		USB 3.0 compliant AC coupled close to respective device
USB_OC0# ~~USB_0_1_OC#~~	85 86	USB over-current sense, USB ports 1 and 2. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3V Suspend	Do not pull high on carrier
USB_OC1# ~~USB_2_3_OC#~~	79 80	USB over-current sense, USB ports 3 and 4. A pull-up for this line shall be present on the module. An open drain driver from a USB current monitor on the carrier board may drive this line low.	I 3.3VSB	PU 10k 3.3V Suspend	Do not pull high on carrier
USB_VBUS	91	USB VBUS pin, 5V tolerant VBUS resistance has to be placed on the module VBUS capacitance has to be placed on the carrier board	I CMOS 5.0V		
USB_OTG_ID	92	USB On-The-Go ID pin. Configures the mode of USB OTG Port. The resistance of this pin measured to ground is used to determine whether USB OTG is going to be used as USB Client to enable/ disable USB Client support.	O Analog	PU 10k 3.3V Suspend	

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3.3.7. LVDS

Signal	Pin	Description	I/O	PU/PD	Comment
LVDS_A0+ LVDS_A0- LVDS_A1+ LVDS_A1- LVDS_A2+ LVDS_A2- LVDS_A3+ LVDS_A3-	99 101 103 105 107 109 113 115	LVDS Channel A differential pairs	O LVDS		LVDS is default (through eDP to LVDS bridge) **Note:** eDP support is a build option
LVDS_A_CK+ LVDS_A_CK-	119 121	LVDS Channel A differential clock	O LVDS		
LVDS_B0+ LVDS_B0- LVDS_B1+ LVDS_B1- LVDS_B2+ LVDS_B2- LVDS_B3+ LVDS_B3-	100 102 104 106 108 110 114 116	LVDS Channel B differential pairs	O LVDS		
LVDS_B_CK+ LVDS_B_CK-	120 122	LVDS Channel B differential clock	O LVDS		
LVDS_3P3_VDD_EN	111	LVDS panel power enable	O 3.3V		
LVDS_3P3_BKLT_EN	112	LVDS panel backlight enable	O 3.3V		
LVDS_3P3_BKLT_CTRL	123	LVDS panel backlight brightness control	O 3.3V		ePD to LVDS requirement
3P3_LVDS_DDC_CLK	127	DDC lines used for flat panel detection and control	O 3.3V	PU 2.2k 3.3V	
3P3_LVDS_DDC_DAT	125	DDC lines used for flat panel detection and control	I/O 3.3V	PU 2.2k 3.3V	

3.3.8. eDP Build Option

Signal	Pin	Description	I/O	PU/PD	Comment
eDP0_TX2+ eDP0_TX2- eDP0_TX1+ eDP0_TX1- eDP0_TX0+ eDP0_TX0-	107 109 103 105 99 101	eDP differential pairs	O PCIE		AC coupled on module
eDP0_TX3+ eDP0_TX3-	113 115	eDP differential pairs	O PCIE		AC coupled on module
eDP0_AUX+	119	eDP AUX+	I/O PCIE		AC coupled on module
eDP0_AUX-	121	eDP AUX-	I/O PCIE		AC coupled on module
eDP0_HPD#	126	embedded DisplayPort Hotplug detection	I 3.3V		
eDP1_HPD#	128	embedded DisplayPort Hotplug detection	I 3.3V		

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3.3.9. DisplayPort

Signal	Pin	Description	I/O	PU/PD	Comment
DP_LANE3+ DP_LANE3-	131 133	DDI1 differential pair for DisplayPort lane 3	O eDP/DP		AC coupled -on module
DP_LANE1+ DP_LANE1-	137 139	DDI1 differential pair for DisplayPort lane 1	O eDP/DP		AC coupled -on module
DP_LANE2+ DP_LANE2-	143 145	DDI1 differential pair for DisplayPort lane 2	O eDP/DP		AC coupled -on module
DP_LANE0+ DP_LANE0-	149 151	DDI1 differential pair for DisplayPort lane 0	O eDP/DP		AC coupled -on module
DP_HPD#	154	DDI1 Hot Plug Detect signal for DisplayPort that serves as an interrupt request	I CMOS 3.3V		
DP_AUX+ DP_AUX-	138 140	DDI1 Differential pair lines, auxiliary channel used for link management and device control	I/O eDP/DP		AC coupled -on module

3.3.10. HDMI Build Option

Signal	Pin	Description	I/O	PU/PD	Comment
TMDS_CLK+ TMDS_CLK-	131 133	DDI1 differential pair for HDMI clock	O eDP/DP		AC coupled -on module
TMDS_LANE1+ TMDS_LANE1-	137 139	DDI1 differential pair for HDMI lane 1	O eDP/DP		AC coupled -on module
TMDS_LANE0+ TMDS_LANE0-	143 145	DDI1 differential pair for HDMI lane 0	O eDP/DP		AC coupled -on module
TMDS_LANE2+ TMDS_LANE2-	149 151	DDI1 differential pair for HDMI lane 2	O eDP/DP		AC coupled -on module
HDMI_HPD#	153	DDI1 Hot Plug Detect signal for HDMI that serves as an interrupt request	I CMOS 3.3V		
HDMI_CTRL_DAT	150	DDC based control signal (data) for HDMI device. ***Note:*** *Level shifters must be implemented on the carrier board for this signal in order to be compliant with the HDMI Specification.*	I/O CMOS 3.3V OD	PU 2.2K 3.3V	
HDMI_CTRL_CLK	152	DDC based control signal (clock) for HDMI device. ***Note:*** *Level shifters must be implemented on the carrier board for this signal in order to be compliant with the HDMI Specification.*	I/O CMOS 3.3V OD	PU 2.2K 3.3V	

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3.3.11. PCI Express

Signal	Pin	Description	I/O	PU/PD	Comment
PCIE0_TX+ PCIE0_TX-	179 181	PCI Express channel 0, Transmit Output differential pair.	O PCIE		AC coupled on module
PCIE0_RX+ PCIE0_RX-	180 182	PCI Express channel 0, Receive Input differential pair.	I PCIE		AC coupled close to respective device
PCIE1_TX+ PCIE1_TX-	173 175	PCI Express channel 1, Transmit Output differential pair.	O PCIE		AC coupled on module
PCIE1_RX+ PCIE1_RX-	174 176	PCI Express channel 1, Receive Input differential pair.	I PCIE		AC coupled close to respective device
PCIE2_TX+ PCIE2_TX-	167 169	PCI Express channel 2, Transmit Output differential pair.	O PCIE		AC coupled on module
PCIE2_RX+ PCIE2_RX-	168 170	PCI Express channel 2, Receive Input differential pair.	I PCIE		AC coupled close to respective device
PCIE3_TX+ PCIE3_TX-	161 163	PCI Express channel 3, Transmit Output differential pair.	O PCIE		PCIe port 3 is used by LAN by default. Build option supports PCIe port 3.
PCIE3_RX+ PCIE3_RX-	162 164	PCI Express channel 3, Receive Input differential pair.	I PCIE		PCIe port 3 is used by LAN by default. Build option supports PCIe port 3.
PCIE_CLK_REF+ PCIE_CLK_REF-	155 157	PCI Express Reference Clock output for all PCI Express and PCI Express Graphics Lanes.	O PCIE		
PCIE_WAKE#	156	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	I CMOS 3.3V Suspend	PU 1K 3.3V suspend	
PCIE_RST#	158	Reset Signal for external devices	O CMOS 3.3V		

3.3.12. UART

Signal	Pin	Description	I/O	PU/PD	Comment
UART0_TX	171	Serial Data Transmitter	O CMOS 3.3V		
UART0_RX	177	Serial Data Receiver	I CMOS 3.3V		
UART0_CTS#	178	Handshake signal, clear to send data	I CMOS 3.3V		
UART0_RTS#	172	Handshake signal, request to send data	O CMOS 3.3V		

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3.3.13. LPC Bus

Signal	Pin	Description	I/O	PU/PD	Comment
LPC_AD0	185	LPC multiplexed address, command, and data bus signal 0	I/O CMOS 3.3V		
LPC_AD1	186	LPC multiplexed address, command, and data bus signal 1	I/O CMOS 3.3V		
LPC_AD2	187	LPC multiplexed address, command, and data bus signal 2	I/O CMOS 3.3V		
LPC_AD3	188	LPC multiplexed address, command, and data bus signal 3	I/O CMOS 3.3V		
LPC_CLK	189	LPC clock output signal	I/O CMOS 3.3V		
LPC_FRAME#	190	LPC frame signal indicating the start of a new LPC cycle or the termination of a broken cycle	I/O CMOS 3.3V		
LPC_LDRQ#	192	LPC serial DMA request signal	I/O CMOS 3.3V		
LPC_SERIRQ	191	LPC serial interrupt signal	I/O CMOS 3.3V		

3.3.14. SPI

Signal	Pin	Description	I/O	PU/PD	Comment
SPI_MOSI	199	Master serial output/Slave serial input signal. SPI serial output data from Qseven® module to the SPI device.	O CMOS 3.3V		
SPI_MISO	201	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven® module.	I CMOS 3.3V		
SPI_CS0#	200	SPI chip select 0 output	O CMOS 3.3V	PU 10K 3.3V suspend	
SPI_CS1#	202	SPI chip select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.	O CMOS 3.3V		
SPI_SCK	203	SPI clock output.	O CMOS 3.3V		

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3.3.15. Power and System Management

Signal	Pin	Description	I/O	PU/PD	Comment
PWRBTN#	20	Power Button: Low active power button input. This signal is triggered on the falling edge.	I CMOS 3.3V	PU 100K 3.3V suspend	
SUS_S3#	18	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram) or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	O CMOS 3.3V Suspend		
SUS_S5#	16	S5 State: This signal indicates S5 (Soft Off) state.	O CMOS 3.3V Suspend		
WAKE#	17	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	I CMOS 3.3V Suspend	PU 10K 3.3V suspend	
BATLOW#	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	I CMOS 3.3V Suspend	PU 10K 3.3V suspend	
RSTBTN#	28	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module.	I CMOS 3.3V	PU 4.7K 3.3V suspend	
LID_BTN#	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. Open/Close state may be software configurable.	I CMOS 3.3V Suspend	PU 10K 3.3V suspend	
SLP_BTN#	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.	I CMOS 3.3V Suspend	PU 10K 3.3V suspend	
PWGIN	26	High active input for the Qseven® module indicates that all power rails located on the carrier board are ready for use.	I CMOS 5V	PU 10K 5V suspend	

3.3.16. Power and Ground

Signal	Pin	Description	I/O	PU/PD	Comment
VCC_5V_SBY	205-206	Standby Power Supply +5VDC ±5%.	P		
VCC_RTC	193	3V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.4 - 3.3 V).	P		
GND	1, 2, 23, 24, 25, 34, 39, 40, 57, 58, 73, 74, 97, 98, 117, 118, 135, 136, 141, 142, 147, 148, 159, 160, 165, 166, 183, 184, 197, 198	Power Ground	P		

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3.3.17. Thermal Management

Signal	Pin	Description	I/O	PU/PD	Comment
THRM#	70	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	I CMOS 3.3V		
THERMTRIP#	72	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off).	O CMOS 3.3V		

3.3.18. Fan Control Management

Signal	Pin	Description	I/O	PU/PD	Comment
BMC_ PWM_OUT	196	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output.	O CMOS 3.3V OC		
BMC_TACHIN	195	Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input.	I CMOS 3.3V		

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4. Connector Pinouts on Module

This chapter describes connectors, LEDs, and switches that are used on the module.

4.1. Connector, Switch, and LED Locations

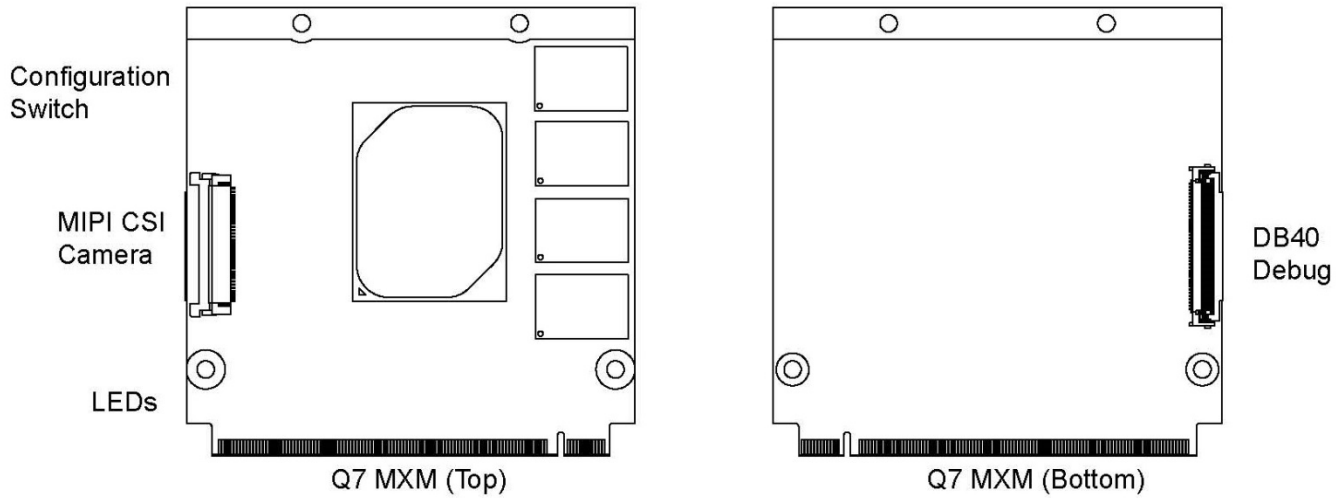


Figure 7: Q7-AL Connector, Switch and LED Locations

4.2. Q7-AL and the DB40 Debug Module

The DB40 debug board can be connected via a FPC 40-pin flat cable to the module. It provides bus extensions to the SPI bus (out of band BIOS flashing) and the BMC (access to Board Management Controller). It also can be used to show BIOS POST CODE Display 80/81h (on LPC) and it provides Test Points with Signaling LEDs

- PWRBTN
- SYS_RESET#
- CB_RESET#
- CB_PWROK
- SUS_S3#
- SUS_S4#
- SUS_S5#

Moreover there is a PWRBTN / SYS_RESET switch and a BIOS Mode Selection: Failsafe.

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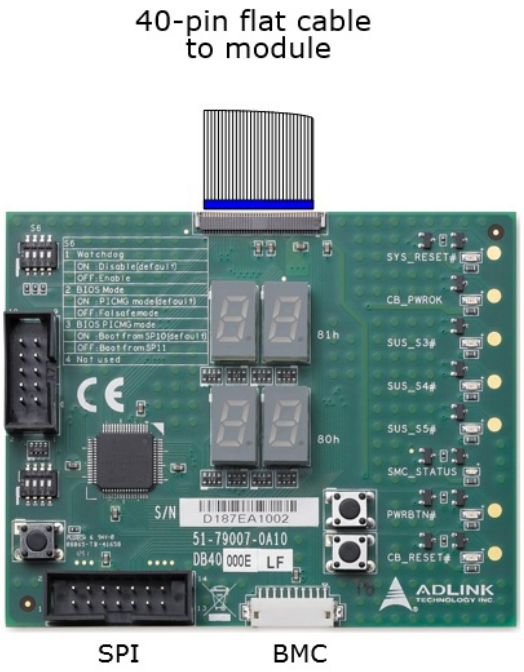


Figure 8: Q7-AL and the DB40 Debug Module

4.3. 36-pin MIPI-CSI2 Camera Connector

FPC Connector Type: Flatfoil with 0.5mm pitch

Pin Orientation



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Table 2: 36-pin MIPI-CSI Camera Connector Pin Definition on the Qseven Module

Pin	Signal	Description
1	V3P3S	3.3 volts +/-5% to power the camera device (output)
2	V3P3S	3.3 volts +/-5% to power the camera device (output)
3	MCSI1_D0_P	CSI1 Camera 0 Data Lane 0+
4	MCSI1_D0_N	CSI1 Camera 0 Data Lane 0-
5	GND	Ground
6	MCSI1_D1_P	CSI1 Camera 0 Data Lane 1+
7	MCSI1_D1_N	CSI1 Camera 0 Data Lane 1-
8	GND	Ground
9	MCSI1_D2_P	CSI1 Camera 0 Data Lane 2+
10	MCSI1_D2_N	CSI1 Camera 0 Data Lane 2-
11	MCSI1_CAM0RST#	Camera 0 Reset (active low; CMOS 1.8V; output)
12	MCSI1_D3_P	CSI1 Camera 0 Data Lane 3+
13	MCSI1_D3_N	CSI1 Camera 0 Data Lane 3-
14	GND	Ground
15	MCSI1_CLK_P	CSI1 Camera 0 Differential Clock+ (Strobe; PHY; input)
16	MCSI1_CLK_N	CSI1 Camera 0 Differential Clock- (Strobe; PHY; input)
17	GND	Ground
18	CN_I2C_CAM0_CK	Camera 0 Control Interface Clock (I2C-like interface; CMOS 1.8V OD; output)
19	CN_I2C_CAM0_DAT	Camera 0 Control Interface Data (I2C-like interface; CMOS 1.8V OD; input/output)
20	CAM0_ENA#	Camera 0 Enable (active low; CMOS 1.8V; output)
21	CAM_MCLK_R	Master Clock (may be used by cameras to drive internal PLL; frequency range: 6-27MHz; CMOS 1.8V; output)
22	CAM1_ENA#	Camera1 Enable (active low; CMOS 1.8V; output)
23	CN_I2C_CAM1_CK	Camera 1 Control Interface Clock (I2C-like interface; CMOS 1.8V OD; output)
24	CN_I2C_CAM1_DAT	Camera 1 Control Interface Data (I2C-like interface; CMOS 1.8V OD; input/output)
25	GND	Ground
26	MCSI2_CLK_P	CSI2 Camera 1 Differential Clock+ (Strobe; PHY; input)
27	MCSI2_CLK_N	CSI2 Camera 1 Differential Clock- (Strobe; PHY; input)
28	GND	Ground
29	MCSI2_D0_P	CSI2 Camera 1 Data Lane 0+ (D-PHY; input)
30	MCSI2_D0_N	CSI2 Camera 1 Data Lane 0- (D-PHY; input)
31	MCSI_CAM1RST#	Camera 1 Reset (active low; CMOS 1.8V; output)
32	MCSI2_D1_P	CSI2 Camera 1 Data Lane 1+ (D-PHY; input)
33	MCSI2_D1_N	CSI2 Camera 1 Data Lane 1- (D-PHY; input)
34	GND	Ground
35	CAM0_GPIO	GPIO for Camera 0 (CMOS 1.8V; input/output)
36	CAM1_GPIO	GPIO for Camera 1 (CMOS 1.8V; input/output)

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4.4. 40-pin Debug Connector

FPC Connector Type: FCI 59GF Flex 10042867

Pin Orientation



1 40

Table 3: 40-pin Debug Connector Pin Definition on the Qseven Module

Pin	Interface	Signal
1	NC	RESERVED
2	SMC Debug	SMC_STATUS
3		BIOS_MODE
4		SEL_BIOS
5		POSTWDT_DIS#
6	Test Point	SUS_S5#
7		SUS_S4#
8		SUS_S3#
9		CB_PWROK
10		CB_RESET#
11		SYS_RESET#
12		PWRBTN#
13	SMC Program Interface	SMC_OCD0B
14		SMC_OCD0A
15		SMC_CLK
16		SMC_DATA
17		SMC_RESET_IN#
18		SMC_FLMD0
19		SMC_RXD6
20		SMC_TXD6
21		GND
22		3V3_DUAL
23		3V3_SMC1
24	LPC Debug Card Interface	LPC_AD0
25		LPC_AD1
26		LPC_AD2
27		LPC_AD3
28		LPC_FRAME#

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Pin	Interface	Signal
29		CLK33_LPC
30		RST#
31		BIOS_DIS0
32		GND
33		LPC_3V3
34	SPI Program Interface	SPI_BIOS_CLK
35		SPI_BIOS_MOSI
36		SPI_BIOS_MISO
37		SPI_BIOS_CS1#
38		SPI_BIOS_CS0#
39		GND
40		VCC_SPI_IN (SPI power input from flash tool to module)

Note: The pin definition on the debug module is the inverse of that on the Qseven module.

4.5. Status LEDs

To facilitate easier maintenance, status LEDs are mounted on the board.

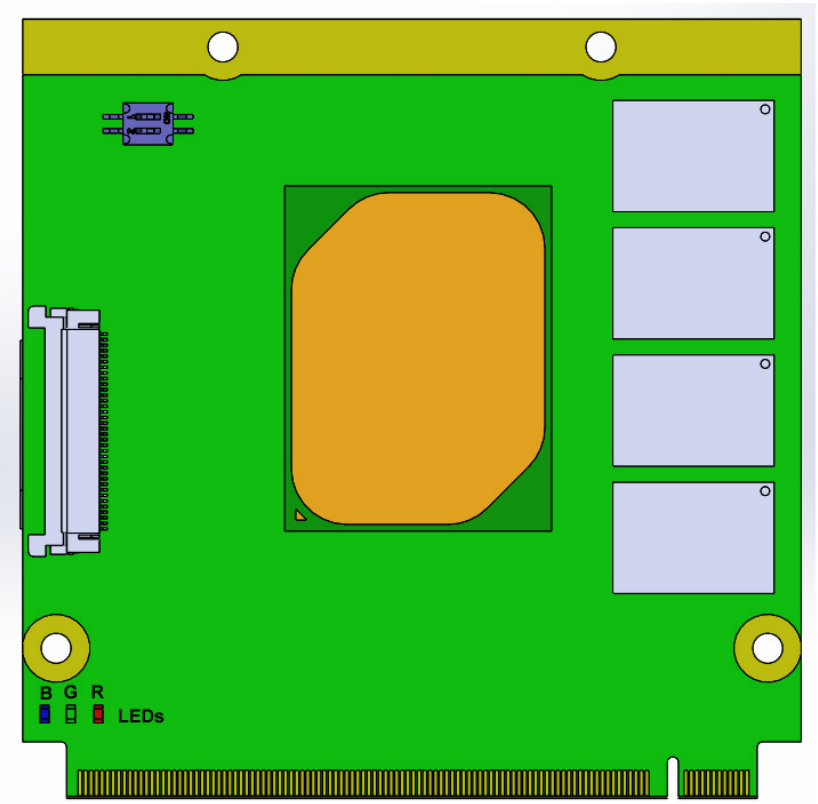


Figure 9: Q7-AL LED Locations

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Table 4: LED Descriptions

Name	Color	Connection	Function
LED1	Blue	BMC output	Power Sequence Status Code (BMC) Power Changes, RESET (see 5.1.4 Exception Codes below) During startup of the module this LED may be lit or show blink codes. During normal operation, this LED is switched off.
LED2	Green	Power Source 3Vcc	S0 LED ON S3/S5 LED OFF ECO mode LED OFF During normal operation this LED is switched on.
LED3	Red	BMC output and same signal as WDT (72) on BtB connector	This LED indicates the watchdog timer activity Module power up WD LED = LED OFF Watchdog counting WD LED = Keep Last State Watchdog timed out WD LED = LED ON Watchdog RESET WD LED = LED ON Rebooted after WD RESET WD LED = LED ON Rebooted after PWRBTN WD LED = LED OFF Rebooted after RESET BTN WD LED = LED OFF Note: only a RESET not initiated by the BMC can clear the WD LED (user action)

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4.6. BIOS Switch Settings

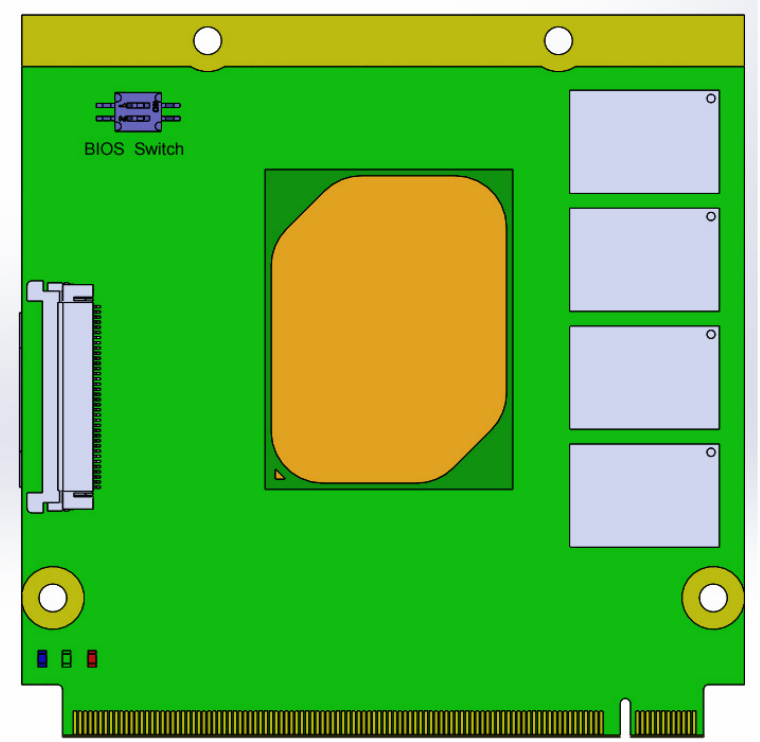


Figure 10: Q7-AL BIOS Switch Location

BIOS Select and Mode Configuration Switch

The module has two BIOS chips, and BIOS operation can be configured to "Normal" and dual-BIOS "Failsafe" modes using the BIOS Select and Mode Configuration switch (BSW1), Pin 2.

Setting the module to Normal mode will configure the BIOS chips on the module as SPI0 and SPI1. In Normal mode, a BIOS chip cannot be placed in the SPI0 slot on the carrier.

In dual-BIOS Failsafe mode, both BIOS chips on the module are configured as SPI1. Only one of the two is connected to the SPI bus at any given time. In case of failure of the primary SPI1 BIOS, the system will reboot and switch to the secondary SPI1 BIOS on the module. In Failsafe mode, the SPI0 BIOS socket on the carrier can be populated.

In either mode, the BIOS Select and Mode Configuration switch (BSW1), Pin 1 is used to select whether to boot from SPI0 or SPI1.

Table 5: BIOS Select and Mode Configuration Switch Settings

Mode	Pin 1	Pin 2
Boot from SPI0 (default)	On	—
Boot from SPI1	Off	—
Set BIOS to Normal mode	—	On
Set BIOS to Failsafe BIOS mode (default)	—	Off

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5. Smart Embedded Management Agent (SEMA)

The onboard microcontroller (BMC) implements power sequencing and Smart Embedded Management Agent (SEMA) functionality. The microcontroller communicates via the System Management Bus with the CPU/chipset. The following functions are implemented:

- Total operating hours counter. Counts the number of hours the module has been run in minutes.
- On-time minutes counter. Counts the seconds since last system start.
- Temperature monitoring of CPU and board temperature. Minimum and maximum temperature values of CPU and board are stored in flash.
- Power cycles counter
- Boot counter. Counts the number of boot attempts.
- Watchdog Timer. Set/Reset/Disable Watchdog Timer. Features auto-reload at power-up.
- System Restart Cause. Power loss/BIOS Fail/Watchdog/Internal Reset/External Reset
- Fail-safe BIOS support. In case of a boot failure, hardware signals tell external logic to boot from fail-safe BIOS.
- Flash area. 1kB Flash area for customer data
- Board Identify. Vendor/Board/Serial number/Production Date
- Main-current & voltage. Monitors drawn current and main voltages

For a detailed description of SEMA features and functionality, please refer to **SEMA Technical Manual** and **SEMA Software Manual**, downloadable at: **http://www.adlinktech.com/sema/**.

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5.1. Board Specific SEMA Functions

5.1.1. Voltages

The BMC of the Q7-AL implements a voltage monitor and samples several onboard voltages. The voltages can be read by calling the SEMA function “Get Voltages”. The function returns a 16-bit value divided into high-byte (MSB) and low-byte (LSB).

Table 6: SEMA Onboard Voltage Monitor

ADC Channel	Voltage Name	Voltage Formula [V]
0	VCC_CORE	(MSB<<8 + LSB) x 3.3 / 1024
1	VGG_S3	(MSB<<8 + LSB) x 3.3 / 1024
2	V1P05_S3	(MSB<<8 + LSB) x 3.3 / 1024
3	VDDQ	(MSB<<8 + LSB) x 3.3 / 1024
5	VRTCVIN	(MSB<<8 + LSB) x 3.3 / 1024
6	V3P3_S	(MSB<<8 + LSB) x 1.100 x 3.3 / 1024
7	V3P3_A	(MSB<<8 + LSB) x 1.100 x 3.3 / 1024
12	V1P24_A	(MSB<<8 + LSB) x 3.3 / 1024
13	V1P8_A	(MSB<<8 + LSB) x 3.3 / 1024
15	Q7	(MSB<<8 + LSB) x 1.826 x 3.3 / 1024
16	(MAIN CURRENT)	Use Main Current Function

5.1.2. Main Current

The BMC of the Q7-AL implements a current monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in high-byte (MSB) and low-byte (LSB). These 4 values represent the last 4 currents drawn by the board. The values are sampled every 250ms. The order of the 4 values is NOT in chronological order. Access by the BMC may increase the drawn current of the whole system. In this case, there are still 3 samples not influenced by the read access.

$$\text{Main Current} = (\text{MSB_n} << 8 + \text{LSB_n}) \times 8.06\text{mA}$$

5.1.3. BMC Status

This register shows the status of BMC controlled signals on the Q7-AL.

Table 7: SEMA BMC Status

Status Bit	Signal
0	WDT_OUT
1	LVDS_VDDEN
2	LVDS_BKLTEN
3	BIOS_MODE
4	POSTWDT_DISn
5	SEL_BIOS

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5.1.4. Exception Codes

In case of an error, the BMC drives a blinking code on the blue Status LED (LED1). The same error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash Storage and is cleared when the power is removed. Therefore, a “Clear Exception Code” command is not needed or supported.

Table 8: SEMA Exception Codes

Exception Code	Error Message
0	NOERROR
2	NO_SUSCLK
3	NO_SLP_S4_S5
4	NO_SLP_S3
5	BIOS_FAIL
6	RESET_FAIL
7	RESETIN_FAIL
8	NO_VIN_PWR_BAD
9	CRITICAL_TEMP
10	POWER_FAIL
11	VOLTAGE_FAIL
12	NO_3V3_5V_A_PG
13	NO_VNN_PG
14	NO_1V24_A_PG
15	NO_VDDQ_PG
16	NO_V1P05S_PG
17	NO_V3P3_S0_PG
18	NO_V12
19	MEMORY_ERROR
20	NO_P3V3_A_READY

5.1.5. BMC Flags

The BMC Flags register returns the last detected Exception Code since power-up and shows the BIOS in use and the power mode.

Table 9: SEMA BMC Flags

Bit	Description
[0 ~ 4]	Exception Code
[6]	0 = AT mode 1 = ATX mode
[7]	0 = Standard BIOS 1 = Fail-safe BIOS.

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6. System Resources

6.1. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
(4GB-2MB)	FFE00000 – FFFFFFFF	16 MB	High BIOS Area
(4GB-18MB) – (4GB-17MB-1)	FEE00000 – FEEFFFFF	1 MB	MSI Interrupts
(4GB-20MB) – (4GB-19MB-1)	FEC00000 – FECFFFFF	1 MB	APIC Configuration Space
15MB – 16MB	F00000 – FFFFFF	1 MB	ISA Hole
1MB -15MB	100000 - EFFFFF	14MB	Main Memory
0K –1MB	00000 – FFFFFF	1MB	DOS Compatibility Memory

6.2. Direct Memory Access Channels

Channel Number	Data Width	System Resource
0	8-bits	Generic
1	8-bits	Generic
2	8-bits	Generic
3	8-bits	Generic
4		Reserved - cascade channel
5	16-bits	Generic
6	16-bits	Generic
7	16-bits	Generic

6.3. I/O Map

Hex Range	Device
20h – 21h	Interrupt Controller
24h – 25h	Interrupt Controller
28h – 29h	Interrupt Controller
2Ch – 2Dh	Interrupt Controller
02E-02F	LPC/eSPI
30h – 31h	Interrupt Controller
34h – 35h	Interrupt Controller
38h – 39h	Interrupt Controller
3Ch – 3Dh	Interrupt Controller
040h	Timer/Counter
42h – 43h	Timer/Counter
4Eh – 4Fh	LPC/eSPI
50h	Timer/Counter

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Hex Range	Device
52h – 53h	Timer/Counter
60h	LPC/eSPI
61h	NMI Controller
62h	Microcontroller
63h	NMI Controller1
64h	Microcontroller
65h	NMI Controller1
66h	Microcontroller
67h	NMI Controller1
70h	RTC Controller
71h	RTC Controller
72h	RTC Controller
73h	RTC Controller
74h	RTC Controller
75h	RTC Controller
76h – 77h	RTC Controller
80h	LPC/eSPI or PCIe
84h – 86h	Reserved
88h	Reserved
8Ch – 8Eh	Reserved
90h	(Alias to 80h)
092	Reset Generator
94h – 96h	(Aliases to 8xh)
98h	(Alias to 88h)
9Ch – 9Eh	(Alias to 8xh)
A0h – A1h	Interrupt Controller
A4h – A5h	Interrupt Controller
A8h – A9h	Interrupt Controller
ACh – ADh	Interrupt Controller
B0h – B1h	Interrupt Controller
B2h – B3h	Interrupt Controller
B4h – B5h	Interrupt Controller
B8h – B9h	Interrupt Controller
BCh – BDh	Interrupt Controller
200 – 207h	Gameport Low
208–20Fh	Gameport High
4D0h – 4D1h	Interrupt Controller
CF9h	Reset Generator

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6.4. Interrupt Request (IRQ) Lines

PIC Mode

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 3 (COM3)	N/A	Note (1)
4	Serial Port 2 (COM2)	N/A	Note (1)
5	Serial Port 1 (COM1)	N/A	Note (1)
6	Generic	IRQ6 via SERIRQ / PIRQ	No
7	Serial Port 0 (COM0)	IRQ7 via SERIRQ / PIRQ	Note (1)
8	Real-time clock	N/A	No
9	Generic	N/A	Note (1)
10	Generic	IRQ10 via SERIRQ / PIRQ	Note (1)
11	Generic	IRQ11 via SERIRQ / PIRQ	Note (1)
12	PS/2 Mouse	IRQ12 via SERIRQ / PIRQ	Note (1)
13	GSPI, UART, I2C, SDIO	N/A	Note (1)
14	Gpio	PIRQ	Note (1)
15	Gpio	PIRQ	Note (1)

Note (1): These IRQs can be used for PCI devices when onboard device is disabled.

APIC Mode

IRQ#	Typical Interrupt Resource	Connected to Pin	Available
0	Counter 0	N/A	No
1	Keyboard controller	N/A	No
2	Cascade interrupt from slave PIC	N/A	No
3	Serial Port 3 (COM3)	N/A	Note (1)
4	Serial Port 2 (COM2)	N/A	Note (1)
5	Serial Port 1 (COM1)	N/A	Note (1)
6	N/A	N/A	Note (1)
7	Serial Port 0 (COM0)	IRQ7 via SERIRQ / PIRQ	Note (1)
8	Real-time clock	N/A	No
9	N/A	IRQ9 via SERIRQ / PIRQ	Note (1)
10	N/A	IRQ10 via SERIRQ / PIRQ	Note (1)
11	N/A	IRQ11 via SERIRQ / PIRQ	Note (1)
12	PS/2 Mouse	IRQ12 via SERIRQ / PIRQ	Note (1)
13	Math Processor	N/A	Note (1)
14	Primary IDE controller	IRQ14 via SERIRQ / PIRQ	Note (1)

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IRQ#	Typical Interrupt Resource	Connected to Pin	Available
15	Secondary IDE controller	IRQ15 via SERIRQ / PIRQ	Note (1)
16	N/A	P.E.G Root Port, Intel HDA, PCIE Port 0/1/2/3/4/5/6, EHCI Controller #2 , I.G.D ,XHCI Controller	Note (1)
17	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port,	Note (1)
18	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port, SMBus Controller, EHCI Controller #2	Note (1)
19	N/A	PCIE Port 0/1/2/3/4/5/6, P.E.G Root Port,	Note (1)
20	N/A	Gbe Controller	Note (1)
21	N/A		Note (1)
22	N/A	Intel HDA	Note (1)
23	N/A	EHCI Controller #1	Note (1)

Note (1): These IRQs can be used for PCI devices when onboard device is disabled.

6.5. PCI Configuration Space Map

Device: Functions #	Function Description
Bus 0: Device 31: Function 0	LPC Interface (eSPI Enable Strap = 0) eSPI Interface (eSPI Enable Strap = 1)
Bus 0: Device 31: Function 1	P2SB
Bus 0: Device 31: Function 2	PMC
Bus 0: Device 31: Function 3	Intel® High Definition Audio (Intel® HD Audio) (Audio, Voice, Speech)
Bus 0: Device 31: Function 4	SMBus Controller
Bus 0: Device 31: Function 5	SPI
Bus 0: Device 31: Function 6	GbE Controller
Bus 0: Device 31: Function 7	Intel® Trace Hub
Bus 0: Device 30: Function 0	UART #0
Bus 0: Device 30: Function 1	UART #1 (N/A)
Bus 0: Device 30: Function 2	SPI #0
Bus 0: Device 30: Function 4	eMMC*
Bus 0: Device 30: Function 6	SDCard
Bus 0: Device 29: Function 0	PCI Express Port 9
Bus 0: Device 29: Function 1	PCI Express Port 10
Bus 0: Device 29: Function 2	PCI Express Port 11
Bus 0: Device 29: Function 3	PCI Express Port 12
Bus 0: Device 28: Function 0	PCI Express Port 1
Bus 0: Device 28: Function 1	PCI Express Port 2
Bus 0: Device 28: Function 2	PCI Express Port 3

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Device: Functions #	Function Description
Bus 0: Device 28: Function 3	PCI Express Port 4
Bus 0: Device 28: Function 4	PCI Express Port 5
Bus 0: Device 28: Function 5	PCI Express Port 6
Bus 0: Device 28: Function 6	PCI Express Port 7
Bus 0: Device 28: Function 7	PCI Express Port 8
Bus 0: Device 25: Function 0	UART Controller #2
Bus 0: Device 25: Function 1	I2C Controller #5
Bus 0: Device 25: Function 2	I2C Controller #4
Bus 0: Device 23: Function 0	SATA Controller
Bus 0: Device 22: Function 0	Intel® MEI #1
Bus 0: Device 22: Function 1	Intel® MEI #2
Bus 0: Device 22: Function 2	IDE Redirection (IDE-R)
Bus 0: Device 22: Function 3	Keyboard and Text (KT) Redirection
Bus 0: Device 22: Function 4	Intel® MEI #3
Bus 0: Device 21: Function 0	I2C Controller #0
Bus 0: Device 21: Function 1	I2C Controller #1
Bus 0: Device 21: Function 2	I2C Controller #2
Bus 0: Device 21: Function 3	I2C Controller #3
Bus 0: Device 20: Function 0	USB 3.0 xHCI Controller
Bus 0: Device 20: Function 1	USB Device Controller (OTG)
Bus 0: Device 20: Function 2	Thermal Subsystem
Bus 0: Device 20: Function 3	Camera I/O Host Controller
Bus 0: Device 19: Function 0	Integrated Sensor Hub

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6.6. PCI Interrupt Routing Map

INT Line	P.E.G. Root Port	Audio Controller	xHCI Controller	ME Controller #1	ME Controller #2	IDE-R	KT
Int0	INTA:16	INTA:16	INTA:16	INTA:16			
Int1	INTB:17			INTD:17			
Int2	INTC:18			INTC:18			
Int3	INTD:19			INTB:19			

INT Line	GbE Controller	HDA Controller	PCIE port1	PCIE port 2	PCIE port 3	PCIE port 4	PCIE port5
Int0	INTA:16		INTA:16	INTB:17	INTC:18	INTD:19	INTA:16
Int1			INTB:17	INTC:18	INTD:19	INTA:16	INTB:17
Int2			INTC:18	INTD:19	INTA:16	INTB:17	INTC:18
Int3			INTD:19	INTA:16	INTB:17	INTC:18	INTC:19

INT Line	LPC Controller	SATA Controller #1	SMBus Controller	SATA Controller #2
Int0	INTA:16	INTA:16	INTA:16	
Int1	INTB:17			
Int2	INTC:18			
Int3	INTD:19			

6.7. SMBus Address Table

Device	Address
BMC	50h
Thermal Sensor	92h
NXP (eDP to LVDS transmitter)	C0h

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7. BIOS Setup

7.1. Menu Structure

This section presents the six primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right hand column of the respective table.

Main	Advanced	Chipset	Security	Boot	Save & Exit
BIOS Information System Information Board Information ► System Date System Time	CPU Configuration ► Graphics Configuration ► Power Management ► System Management ► Thermal Management ► Watchdog Timer ► CSM Configuration ► Super IO Configuration ► Serial Console Redirection ► USB ► Network ► Miscellaneous ► SDIO Configuration ►	North Bridge ► South Bridge ► Uncore Configuration ► South Cluster Configuration ►	Setup Administrator Password User Password Secure Boot menu ►	Boot Configuration ► Boot Option Priorities ►	Save Options ► Default Options ► Boot Override ►

Notes:

► indicates a submenu

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7.2. Main

The Main Menu provides read-only information about your system and also allows you to set the System Date and Time. Refer to the following tables for details of the submenus and settings.

7.2.1. BIOS Information

Feature	Options	Description
BIOS Vendor	Info only	Vendor
BIOS Version	Info only	Project BIOS Version
Build Data	Info only	Data and Time
MRC Version	Info only	Intel MRC Version
GOP Version	Info only	Intel GOP Version
TXE FW Version	Info only	Intel TXE FW Version
BIOS Boot Source	Info only	Display Platform Current Boot BIOS

7.2.2. System Information

Feature	Options	Description
Project Name	Info only	Project Name
CPU Board Version	Info only	Project Board Version
CPU Brand String	Info only	CPU Brand String Information
CPU Frequency	Info only	CPU Frequency Information
Total Memory	Info only	Total memory size
SOC SKU	Info only	SOC SKU Information

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7.2.3. Board Information

7.2.3.1. Board Information > Board Information

Feature	Options	Description
Serial Number	Info only	Display System Serial Number
Manufacturing Date	Read only	Display Manufacturing Date
Last Repair Date	Read only	Display Last Repair Date
MAC ID	Read only	Display MAC ID

7.2.3.2. Board Information > Runtime Statistics

Feature	Options	Description
Runtime Statistics	Info only	
Total Runtime	Read only	The returned value specifies the total time in minutes the system is running in S0 state.
Current Runtime	Read only	The returned value specifies the time in seconds the system is running in S0 state. This counter is cleared when the system is removed from the external power supply.
Power Cycles	Read only	The returned value specifies the number of times the external power supply has been shut down
Boot Cycles	Read only	The boot counter is increased after a HW- or SW-Reset or after a successful power-up.
Boot Reason	Read only	The boot reason is the event which causes the reboot of the system.

7.2.4. System Date and Time

Feature	Options	Description
System Date	Weekday, MM/DD/YYYY	Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)
System Time	HH/MM/SS	Presented as a 24-hour clock setting in hours, minutes, and seconds

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7.3. Advanced

This menu contains the settings for most of the user interfaces in the system.

7.3.1. Advanced > CPU Configuration

Feature	Options	Description
CPU Configuration	Info only	
Socket 0 CPU Information ►	Submenu	Display socket specific CPU Information
Speed	Info only	Display CPU Speed Frequency
64-bit	Info only	Display CPU 64-bit supported
CPU Power Management ►	Submenu	CPU Power Management options
Active Processor Cores	**Disabled** Enabled	Number of cores to enable in each processor package.
Intel Virtualization Technology	Disabled **Enabled**	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology
Bi-direction PROCHOT	Disabled **Enabled**	When a processor thermal sensor trips (either core), the PROCHOT# will be driven. If bi-direction is enabled, external agents can drive PROCHOT# to throttle the processor.
Thermal Monitor	Disabled **Enabled**	Enable/Disable Thermal Monitor.
Monitor Mwait	Disabled Enabled **Auto**	Enable/Disable Monitor Mwait
P-STATE Coordination	**HW_ALL** SW_ALL SW_ONLY	Change P-State Coordination type.
DTS	Disabled **Enabled**	Enabled/Disabled Digital Thermal Sensor.

7.3.1.1. Advanced > CPU Configuration > Socket 0 CPU Information

Feature	Options	Description
Socket 0 CPU Information	Info only	
CPU Signature	Info only	Display CPU Signature
Microcode Patch	Info only	Display Microcode Patch
Max CPU Speed	Info only	Display Max CPU Speed
Min CPU Speed	Info only	Display Min CPU Speed
Processor Cores	Info only	Display Processor Cores numbers
Intel HT Technology	Info only	Display Not Supported
Intel VT-x Technology	Info only	Display supported
L1 Data Cache	Info only	Display L1 Data Cache
L1 Code Cache	Info only	Display L1 Code Cache

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Feature	Options	Description
L2 Cache	Info only	Display L2 Cache
L3 Cache	Info only	Display L3 Cache

7.3.1.2. Advanced > CPU Configuration > CPU Power Management

Feature	Options	Description
CPU Power Management Configuration	Info only	
EIST	Disabled **Enabled**	Enable/Disable Intel SpeedStep
Intel Turbo Boost technology	Disabled **Enabled**	Intel turbo Boost Technology
Boot performance mode	**Max Performance** Max Battery	Select the performance state that the BIOS will set before OS handoff.
C-States	Disabled **Enabled**	Enable/Disable C States
Enhanced C-States	Disabled **Enabled**	Enable/Disable C1E. When enabled, CPU will switch to minimum speed when all cores enter C-State.
Max Package C State	**PC2** PC1 C0	Controls the Max Package C State that the processor will Support.
Max Core C State	**Fused Value** Core C10 Core C9 Core C8 Core C7 Core C6 Core C1 Unlimited	This option controls the Max Core C State that cores will support.
C-State Auto Demotion	Disabled **C1**	Configure C-State Auto Demotion
C-State Auto Un-Demotion	Disabled **C1**	Configure C-State Auto Un-Demotion
Power Limit 1 Enable	Disabled **Enabled**	Enable/Disable Power Limit 1
Power Limit 1	Info Only	Display Power Limit 1 value
Power Limit 1 Clamp Mode	Disabled **Enabled**	Enable/Disable Power Limit 1 Clamp Mode
Power Limit 1 power	**Auto** 6 7 8 9 10 11 12 13 14	Power Limit 1 in Watts. Auto will program Power Limit 1 based on silicon default support value.

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Feature	Options	Description
	15 16 17 18 19 20 21 22 23 24 25	
Power Limit 1 Time Window	**Auto** 1 2 3 4 5 6 7 8 10 12 14 16 20 24 28 32 40 48 56 64 80 96 112 128	Power Limit 1 Time Window value in Seconds. Auto will program Power Limit 1 Time Window based on silicon default support value.

7.3.2. Advanced > Graphics Configuration

Feature	Options	Description
LVDS	Info only	
Data format and Color Depth	VESA 24 bpp JEIDA 24 bpp **JEIDA/VESA 18 bpp**	Data format and Color Depth select
LVDS Output Mode	**Single LVDS bus** Dual LVDS bus	Single/Dual mode select
DE Polarity	**Active High** Active Low	DE Polarity select
Vsync Polarity	**Active High** Active Low	Vsync Polarity select
Hsync Polarity	**Active High**	Hsync Polarity select

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Feature	Options	Description
	Active Low	
LVDS Backlight Brightness	**Value Range**	A change takes effect immediately. The Value range starts by 0 and ends of 255.

7.3.3. Advanced > Power Management

Feature	Options	Description
Enable ACPI Auto Configuration	**Disabled** Enabled	Enable/Disable BIOS ACPI Auto Configuration.
Enable Hibernation	Disabled **Enabled**	Enable/Disable System ability to hibernate. This option may be not effective with some OS.
ACPI Sleep State	**S3 only (Suspend to RAM)** Suspend Disabled	Select ACPI sleep state the system will enter when the SUSPEND button is pressed.
Emulation AT/ATX	Emulation AT **ATX**	Select Emulation AT or ATX function. If this option set to [Emulation AT], BIOS will report no suspend functions to ACPI OS. Win Windows XP, it will make OS show shutdown message during system shutdown.
Lock Legacy Resources	**Disabled** Enabled	Enables or Disables Lock of Legacy Resources
LID Function	**Disabled** Enabled	Enables or Disables LID function
ECO Mode	**Disabled** Enabled	Reduces the power consumption of the system, but after a shut down, you have to wait at least 5 seconds before you can restart the system.
Power Consumption ►	Submenu	Power Consumption

7.3.3.1. Advanced > Power Management > Power Consumption

Feature	Options	Description
Power Consumption	Info only	
Current Input Current	Read only	Display input current
Current Input Power	Read only	Display input power
V-CORE	Read only	Display actual VCORE voltage
VGFX	Read only	Display actual VGFX voltage
VMEM	Read only	Display actual VMEM voltage
5VSB	Read only	Display actual 5VSB voltage
VIN(12V)	Read only	Display actual VIN(12V) voltage
5V	Read only	Display actual 5V voltage
3.3V	Read only	Display actual 3.3V voltage
3.3VSB	Read only	Display actual 3.3VSB voltage

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7.3.4. Advanced > System Management

Feature	Options	Description
System Management	Info only	
Version	Info only	Display Version
SEMA Firmware	Read only	Display SEMA firmware
Build Date	Read only	Display SEMA firmware build date
SEMA Boot loader	Read only	Display SEMA boot loader
Build Date	Read only	Display SEMA boot loader build date
SEMA Features ►	Submenu	SEMA Features information
Flags ►	Submenu	SEMA Flags information

7.3.4.1. Advanced > System Management > SEMA Features

Feature	Options	Description
SEMA Supported Features	Info only	
Uptime & Power Cycles Counter	Info only	
System Reset Event	Info only	
1024 Bytes User-Flash	Info only	
Watchdog	Info only	
Temperatures	Info only	
Voltage Monitor	Info only	
Display Backlight control	Info only	
Power-Up Watchdog	Info only	
Power Monitor (current sense)	Info only	
Boot Counter	Info only	
Dual-BIOS	Info only	
I2C bus 1	Info only	
I2C bus 2	Info only	
Programmable CPU fan	Info only	
Programmable System fan	Info only	
AT/ATX mode	Info only	
ACPI Thermal Trigger	Info only	
Power-Up to last state	Info only	
Backlight restore	Info only	
DTS register available	Info only	
DTS offset registers programmable	Info only	
TIVA BMC	Info only	
PEC Control	Info only	
SoftFan	Info only	
SEMA Error Log	Info only	

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7.3.4.2. Advanced > System Management > Flags

Feature	Options	Description
Flags	Info only	
BMC Flags	Read only	
BIOS Select	Read only	Display the selection of current BIOS ROM.
ATX/AT-Mode	Read only	Display ATX/AT-Mode.
Exception Code	Read only	System exception reason.

7.3.5. Thermal Management

Feature	Options	Description
Temperatures and Fan Speed ▶	Submenu	Temperatures and Fan Speed.
Smart Fan ▶	Submenu	Smart Fan.
Critical Trip Point	Enabled **Disabled**	This value is the temperature threshold of the critical trip point.
Passive Cooling Trip Point	Enabled **Disabled**	The time-out value for Control, Bulk, and Interrupt transfers.

7.3.5.1. Advanced > Thermal Management > Temperatures and Fan Speed

Feature	Options	Description
Temperatures and Fan	Info only	
CPU Temperature	Info only	
Current	Read only	Display current board temperature
Board Temperatures	Info only	
Current	Read only	Display board current. temperature
Startup	Read only	Display board startup. temperature
Min	Read only	Display board Min. temperature
Max	Read only	Display board Max. temperature
CPU Fan Speed	Read only	Display CPU Fan RPM

7.3.5.2. Advanced > Thermal Management > Smart Fan

Feature	Options	Description
Smart Fan	Info only	
CPU Smart Fan Temperature Source	CPU Sensor **Board Sensor**	CPU smart fan temperature source
CPU Fan Mode	**AUTO (Smart Fan)** Fan Off Fan On	CPU fan mode
PWM Level	30	PWM level

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7.3.6. Advanced > Watchdog Timer

Feature	Options	Description
Watchdog Timer	Info only	
RunTime Watchdog	**Disabled** Enabled	The Runtime Watchdog resets the system after a certain amount of time after power up

7.3.7. Advanced > CSM Configuration

Feature	Options	Description
Compatibility Support Module Configuration	Info only	
CSM Support	Enabled **Disabled**	Enable/Disable CSM Support
CSM16 Module Version	Read Only	Display CSM16 Module Version
GateA20 Active	**Upon Request** Always	UPON REQUEST - GA20 can be disabled using BIOS services. ALWAYS - do not allow disabling GA20; this option is useful when any RT code is executed above 1MB
Boot option filter	**UEFI and Legacy** Legacy only UEFI only	This option controls Legacy/UEFI ROMs priority
Option ROM execution	Info only	
Network	Do not launch **UEFI** Legacy	Controls the execution of UEFI and Legacy PXE OpROM
Storage	Do not launch **UEFI** Legacy	Controls the execution of UEFI and Legacy Storage OpROM
Video	Do not launch **UEFI** Legacy	Controls the execution of UEFI and Legacy Video OpROM
Other PCI device	Do not launch **UEFI** Legacy	Determines OpROM execution policy for devices other than Network, Storage, or Video.

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7.3.8. Advanced > Super IO Configuration

Feature	Options	Description
W83627DHG	Info only	
Serial Port1 Configuration ►	Submenu	Set Parameters of serial port 1
Serial Port 1 Configuration	Info only	
Serial Port	Disabled **Enabled**	Enable or Disable Serial Port (COM)
Device Setting	Info only	
Change Setting	Auto IO=3F8;IRQ=4; IO=3F8;IRQ=3,4,5,7,9,10,11,12 IO=2F8;IRQ=3,4,5,7,9,10,11,12 IO=3E8;IRQ=3,4,5,7,9,10,11,12 IO=2E8;IRQ=3,4,5,7,9,10,11,12	Select an optimal setting for Super IO Device.

7.3.9. Advanced > Serial Console Redirection (UART)

Feature	Options	Description
COM 1	Info only	
Console Redirection	**Disabled** Enabled	Console Redirection enable or disable
Console Redirection Settings ►	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
COM 2	Info only	
Console Redirection	**Disabled** Enabled	Console Redirection enable or disable
Console Redirection Settings ►	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
COM 3	Info only	
Console Redirection	**Disabled** Enabled	Console Redirection enable or disable
Console Redirection Settings ►	Submenu	The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

7.3.9.1. Advanced > Serial Console Redirection > Console Redirection Settings

Feature	Options	Description
COM0 Console Redirection Settings	Info only	
Terminal Type	VT100 **VT100+** VT-UTF8 ANSI	VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes. ANSI: Extended ASCII char set.

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Feature	Options	Description
Bits per second	9600 19200 38400 57600 **115200**	Selects serial port transmission speed. The speed must be matched on the remote computer. Long or noisy lines may require lower speeds.
Data Bits	7 **8**	Select data bits.
Parity	**None** Even Odd Mark Space	Select parity.
Stop Bits	**1** 2	Select number of stop bits.
Flow Control	**None** Hardware RTS/CTS	Select flow control.
VT-UTF8 Combo Key Support	Disabled **Enable**	Enable VT-UTF8 combination key support for ANSI/VT100 terminals.
Recorder Mode	**Disabled** Enable	With this mode enabled only text will be sent. This is to capture terminal data.
Resolution 100x31	**Disabled** Enable	Enables or disables extended terminal resolution
Legacy OS Redirection	**80x24** 80x25	On legacy OSes, the number of rows and columns supported by redirection
Putty KeyPad	**VT100** LINUX XTERMR6 SCO ESCN VT400	Select Function Key and KeyPad on Putty.
Redirection After BIOS Post	**Always Enabled** BootLoader	The Settings specify if BootLoader is selected, then legacy console redirection is disabled before booting to legacy OS.

7.3.10. Advanced > USB

Feature	Options	Description
USB Module version	Info only	
USB Controllers	Info only	
USB Devices	Info only	
Legacy USB Support	**Enabled** Disabled	Enables Legacy USB support.
XHCI Hand-off	Disabled **Enabled**	This is a workaround for OSes without XHCI hand-off support.
USB Mass Storage Driver Support	**Enabled** Disabled	Enable/Disable USB Mass Storage Driver Support.
USB hardware delays and time-outs:	PCH USB Configuration	
USB transfer time-out	1 sec 5 sec 10 sec **20 sec**	The time-out value for Control, Bulk, and Interrupt transfers.

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Feature	Options	Description
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device start unit command time-out.
Device power-up delay	**Auto** Manual	Maximum time the device will take before it properly reports itself to the host controller.
USB Storage Devices:	Info Only	

7.3.11. Advanced > Network

Feature	Options	Description
Onboard LAN Controller	Disabled **Enabled**	Enable/Disable onboard Intel I210LM LAN Controller
Network Stack	**Disabled** Enabled	Enable/Disable UEFI Network Stack

7.3.12. Advanced > Miscellaneous

Feature	Options	Description
Smart Battery Function	**Disabled** Enabled	Enable/Disable Smart Battery Function

7.3.13. Advanced > SDIO Configuration

Feature	Options	Description
SDIO Configuration	Info only	
SDIO Access Mode	**Auto** ADMA SDMA PIO	Auto Option: Access SD device in DMA mode if controller supports it, otherwise in PIO mode. DMA Option: Access SD device in DMA mode. PIO Option: Access SD device in PIO Mode.

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7.4. Chipset

Feature	Options	Description
North Bridge ►	Submenu	North Bridge Parameters
South Bridge ►	Submenu	South Bridge Parameters
Uncore Configuration ►	Submenu	Uncore Configuration.
South Cluster Configuration ►	Submenu	South Cluster Configuration

7.4.1. Chipset > North Bridge

Feature	Options	Description
Memory Information	Info Only	
Total memory	Read Only	Display Memory Size information
Memory Voltage	Read Only	Display Memory voltage
Memory Slot0	Read Only	Display Memory Slot0 information
Memory Slot1	Read Only	Display Memory Slot1 information
Memory Slot2	Read Only	Display Memory Slot2 information
Memory Slot3	Read Only	Display Memory Slot3 information
Max TOLUD	**2 GB** 2.25 GB 2.5 GB 2.75 GB 3 GB	Maximum Value of TOLUD
Above 4GB MMIO BIOS assignment	**Disable** Enable	Enable/Disable above 4GB memory mapped IO BIOS assignment. This is disable automatically when Aperture Size is set to 2048MB
PCIE VGA Workaround	**Disable** Enable	Enable it if your PCIe card cannot boot to DOS. This is for Test only.

7.4.2. Chipset > South Bridge

Feature	Options	Description
Serial IRQ Mode	Quiet **Continuous**	Configure Serial IRQ Mode
SMBus Support	Disable **Enable**	Enable/Disable SMBus Support
OS Selection	**Windows** Android Win7 Intel Linux	Select the target OS.
PCI CLOCK RUN	Disable **Enable**	Enable CLKRUN# logic to stop PCI clocks.
Real Time Option	**RT Disabled** RT Enabled, Agent IDI1 RT Enabled, Agent Disabled	Select Real-Time Enable and IDI Agent Real-Time traffic Mask Bits

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7.4.3. Chipset > Uncore Configuration

7.4.3.1. Chipset > Uncore Configuration > GOP Configuration

Feature	Options	Description
Active LFP Config	**No LFP** eDP	Active Local Flat Panel Config
LVDS Backlight Mode	GTT Mode **BMC Mode**	Select LVDS Backlight control function.
DDI Port 2	No Device Display Port HDMI **DisplayPort with HDMI/DVI Compatible**	DDI port 2 function choose to display Port or HDMI
LCD Panel Type	**Auto** 640x480 800x600 1024x768 1280x1024 1400x1050 1600x1200 1366x768 1680x1050 1920x1200 1440x900 1600x900 1280x800 1920x1080 2048x1536	Select LFP panel used by Internal Graphics Device by selecting the appropriate setup item.
GOP Brightness level	**Value**	Set GOP Brightness Level1; Value ranges from 0-255

7.4.3.2. Chipset > Uncore Configuration > IGD Configuration

Feature	Options	Description
IGD Configuration	Info only	
Integrated Graphics Device	**Enabled** Disabled	Enable: Enable Integrated Graphics Device (IGD) when selected as the Primary Video Adaptor. Disable: Always disable IGD
Primary Display	**IGD** PCIE HG	Select which of IGD/PCI Graphics device should be Primary Display.
Aperture Size	128MB **256MB** 512MB	Select the Aperture Size.
DVMT Pre-Allocated	**64MB** 96MB 128MB 160MB 192MB 224MB 256MB 288MB	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.

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Feature	Options	Description
	320MB 352MB 384MB 416MB 448MB 480MB 512MB	
DVMT Total Gfx Mem	128M **256M** MAX	Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.

7.4.4. Chipset > South Cluster Configuration

Feature	Options	Description
HD-Audio Configuration ►	Submenu	HD-Audio Configuration Settings
PCI Express Configuration ►	Submenu	PCI Express Configuration Settings
SATA Devices ►	Submenu	Press <Enter> to select the SATA Device Configuration Setup options.
SCC Configuration ►	Submenu	SCC Configuration Settings
USB Configuration ►	Submenu	USB Configuration Settings
Miscellaneous ►	Submenu	Enable/Disable Misc. Features

7.4.4.1. Chipset > South Cluster Configuration > HD-Audio Configuration

Feature	Options	Description
HD-Audio Configuration	Info only	
HD-Audio Support	Disabled **Enabled**	Enable/Disable HD-Audio Support
HD-Audio I/O Buffer Ownership Sale	HD_Audio link owns all the I/O buffers **I2C port owns all the I/O buffers**	Set HD-Audio I/O Buffer Ownership

7.4.4.2. Chipset > South Cluster Configuration > PCI Express Configuration

Feature	Options	Description
PCIExpress Configuration	Info only	
PCIE Port assigned to LAN	Info only	
Compliance Mode	**Disabled** Enabled	Compliance Mode Enable/Disable
PCIE Ports 1-4 Configuration	**4x1 Port** **1x2 2x1 Port** **2x2 2x2 Port** **1x4 Port**	To configuration PCI-E Port 1-4 of PCH
PCIe Express Root Port1 ►	Submenu	Control the PCI Express Root Port. Auto: To disable unused root port automatically for the most optimum power savings.

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Feature	Options	Description
		Enable: Enable PCIE root port Disable: Disable PCIE root port
PCIe Express Root Port2 ▶	Submenu	Control the PCI Express Root Port. Auto: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIE root port Disable: Disable PCIE root port
PCIe Express Root Port3 ▶	Submenu	Control the PCI Express Root Port. Auto: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIE root port Disable: Disable PCIE root port
PCIe Express Root Port4 ▶	Submenu	Control the PCI Express Root Port. Auto: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIE root port Disable: Disable PCIE root port

Chipset > South Cluster Configuration > PCI Express Configuration > PCIe Express Root Port 1-4

Feature	Options	Description
PCIe Express Root Port 1-4	Disabled **Enabled**	Control the PCI Express Root Port. Auto: To disable unused root port automatically for the most optimum power savings. Enable: Enable PCIE root port Disable: Disable PCIE root port
ASPM	**Disable** L0s L1 L0sL1 Auto	PCI Express Active State Power Management settings.
L1 Substates	Disable L1.1 L1.2 **L1.1 & L1.2**	PCI Express L1 Substates Settings
ACS	Disabled **Enabled**	Enable/Disable Access Control Services Extend Capability.
URR	**Disabled** Enabled	PCI Express Unsupported Request Reporting Enable/Disable.
FER	**Disabled** Enabled	PCI Express Device Fatal Error Reporting Enable/Disable.
NFER	**Disabled** Enabled	PCI Express Device Non-Fatal Error Reporting Enable/Disable.
CER	**Disabled** Enabled	PCI Express Device Correctable Error Reporting Enable/Disable.
CTO	**Default Setting** 16-55 ms 65-210 ms 260-900 ms 1-3.5 s Disable	PCI Express Completion Timer To Enable/Disable

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Feature	Options	Description
SEFE	**Disabled** Enabled	Root PCI Express System Error on Fatal Error Enable/Disable.
SENFE	**Disabled** Enabled	Enable or disable Root PCI Express System Error on Non-Fatal Error.
SECE	**Disabled** Enabled	Root PCI Express System Error on Correctable Error Enable/Disable.
PME SCI	Disabled **Enabled**	PCI Express PME SCI Enable/Disable.
Hot Plug	**Disabled** Enabled	PCI Express Hot Plug Enable/Disable.
PCIe Speed	**Auto** Gen1 Gen2	Configure PCIe Speed.
Transmitter Half Swing	**Disabled** Enabled	Transmitter Half Swing Enable/Disable.
Extra Bus Reserved	**0**	Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
Reserved Memory	**10**	Reserved Memory and Prefetchable memory (1-20MB) Range for this Root Bridge.
Reserved I/O	**4**	Reserved I/O (4K/8K/12K/46K/20K) Range for this Root Bridge.
PCH PCIE LTR	Disabled **Enabled**	PCH PCIE Latency Reporting Enable/Disable.
Snoop Latency Override	Disable Manual **Auto**	Snoop Latency Override for PCH PCIE. Disable: Disable override. Manual: Manually enter override values Auto (Default): Maintain default BIOS flow.
Non Snoop Latency Override	Disable Manual **Auto**	Non Snoop Latency Override for PCH PCIE. Disable: Disable override. Manual: Manually enter override values Auto (Default): Maintain default BIOS flow.
PCIE LTR Lock	**Disabled** Enabled	PCIE LTR Configuration Lock.
PCIe Selectable De-emphasis	Disabled **Enabled**	When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. 1b – 3.5 dB 0b – 6 dB.

7.4.4.3. Chipset > South Cluster Configuration > SATA Devices

Feature	Options	Description
SATA Drives	Info only	
Chipset-SATA Controller Configuration	Info only	
Chipset SATA	Disabled **Enabled**	Enable/Disable the Chipset SATA Controller. The Chipset SATA Controller supports 2 black internal SATA ports (up to 3Gb/s supported per port).

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Feature	Options	Description
SATA Mode Selection	**AHCI**	Determines how SATA Controller(s) operate.
SATA Interface Speed	Gen1 **Gen2** Gen3	Select SATA Interface Speed, CHV A1 always with Gen1 Speed
SATA Test Mode	**Disabled** Enabled	Test mode **Enabled /** Disabled
Aggressive LPM Support	**Disabled** Enabled	Enable PCH to aggressively enter link power state.
SATA Port Configuration ►	Submenu	SATA Device Options Settings.
SATA Port 0	Info only	
Software Preserve	Info only	
Port 0	Disabled **Enabled**	Enable or Disable SATA Port.
SATA Port 0 Hot Plug Capability	**Disabled** Enabled	If enabled, SATA port will be reported as Hot Plug capable.
Configured as eSATA	Info only	
Mechanical Preserve Switch	Disabled **Enabled**	Controls reporting if this port has a Mechanical Preserve Switch. Note: Requires hardware support.
Spin Up Device	Enabled **Disabled**	If enabled for any ports, Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
SATA device Type	**Hard Disk Drive** Solid State Drive	Identify the SATA port is connected to solid state drive or Hard Disk drive
SATA port 0 DevSlp	**Disabled** Enabled	Enable/Disable SATA Port 0 DevSlp. Board rework for LP needed before enable.
DITO Configuration	**Disabled** Enabled	Enable/Disable DITO Configuration.
DITO Value	Read Only	
DM Value	Read Only	

7.4.4.4. Chipset > South Cluster Configuration > SCC Configuration

Feature	Options	Description
SCC SD Card Support (D27:F0)	Disabled **Enabled**	Enable/Disable SCC SD Card Support
SSC eMMC Support (D28:F0)	Disabled **Enabled**	Enable/Disable SCC eMMC Support
eMMC Max Speed	**HS400** HS200 DDR50	Select the eMMC max Speed allowed

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7.4.4.5. Chipset > South Cluster Configuration > USB Configuration

Feature	Options	Description
XHCI Pre-Boot Driver	**Disabled** Enabled	Enable/Disable XHCI Pre-Boot Driver Support
XHCI Mode	Disabled **Enabled**	Once disable, XHCI controller would be function disabled, none of the USB devices are detectable and usable during boot and in OS. Do not disable it unless for debug purpose.
USB Port Disable Override	**Disabled** Enabled	Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.
USB OTG Support	**Disabled** Enabled	Enable/Disable USB OTG Support
XHCI Disable Compliance Mode	**FALSE** TRUE	Options to disable/enable XHCI LINK Compliance Mode

7.4.4.6. Chipset > South Cluster Configuration > Miscellaneous

Feature	Options	Description
State After G3	**S0 State** S5 State Last State	Specify what state to go to when power is re-applied after a power failure (G3 State). S0 State: System will boot directly as soon as power applied. S5 State: System keeps in power-off state until power button is pressed.
Wake on LAN	**Disabled** Enabled	Enable or Disable the Wake on LAN

7.5. Security

7.5.1. Security > Password Description

Feature	Options	Description
Setup Administrator Password	Enter password	
User Password	Enter password	
Secure Boot menu ►	Submenu	Customizable Secure Boot settings.

7.5.1.1. Security > Password Description > Secure Boot Menu

Feature	Options	Description
System Mode	Setup	
Secure Boot	Info only	
Vendor Boot	Info only	
Secure Boot Control	Disabled **Enabled**	Secure Boot can be enabled if: 1. System is running in User mode with enrolled Platform Key (PK) 2. CSM function is disabled.

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7.6. Boot

7.6.1. Boot > Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**1**	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	**On** Off	Select the keyboard NumLock state.
Quiet Boot	Disabled **Enabled**	Enable or disables Quiet Boot option.
Fast Boot	**Disabled** Enabled	Enable or Disable Fast Boot features. Most probes are skipped to reduce time cost during boot.
New Boot Option Policy	**Default** Place First Place Last	Controls the placement of newly detected UEFI boot options
Boot Mode select	Legacy **UEFI**	Select boot mode LEGACY/UEFI
Boot Option #1~ #8	**Hard Disk** CD/DVD USB Hard Disk USB CD/DVD USB Key USB Floppy USB LAN Network Disabled	Set the system boot order

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8. BIOS Checkpoints, Beep Codes

This section lists checkpoints and beep codes generated by the AMI Aptio BIOS. The checkpoints defined in this document are inherent to the AMIBIOS generic core and do not include any chipset or board specific checkpoint definitions.

Checkpoints and Beep Codes Definition

A checkpoint is either a byte or word value output to I/O port 80h. The BIOS outputs checkpoints throughout bootblock and Power-On Self Test (POST) to indicate the task the system is currently executing. Checkpoints are very useful for debugging problems that occur during the preboot process.

Beep codes are used by the BIOS to indicate a serious or fatal error. They are used when an error occurs before the system video has been initialized, and generated by the system board speaker.

Aptio Boot Flow

While performing the functions of the traditional BIOS, Aptio 5.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers to the following "boot phases", which may apply to various status code & checkpoint descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

Viewing BIOS Checkpoints

Viewing all checkpoints generated by the BIOS requires a checkpoint card, also referred to as a POST Card or POST Diagnostic Card. These are PCI add-in cards that show the value of I/O port 80h on an LED display.

Some computers display checkpoints in the bottom right corner of the screen during POST. This display method is limited, since it only displays checkpoints that occur after the video card has been activated.

Keep in mind that not all computers using AMI Aptio BIOS enable this feature. In most cases, a checkpoint card is the best tool for viewing AMI Aptio BIOS checkpoints.

[1]Analogous to "bootblock" functionality of legacy BIOS
[2]Analogous to "POST" functionality in legacy BIOS

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8.1. Status Code Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

8.2. Standard Status Codes

8.2.1. SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

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SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

8.2.2. SEC Beep Codes

None

8.2.3. PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization

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Status Code	Description
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes

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Status Code	Description
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

8.2.4. PEI Beep Codes

# of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

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8.2.5. DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration

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Status Code	Description
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console Input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)

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Status Code	Description
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

8.2.6. DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

8.2.7. ACPI/ASL Checkpoint

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state

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Status Code	Description
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

8.3. OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

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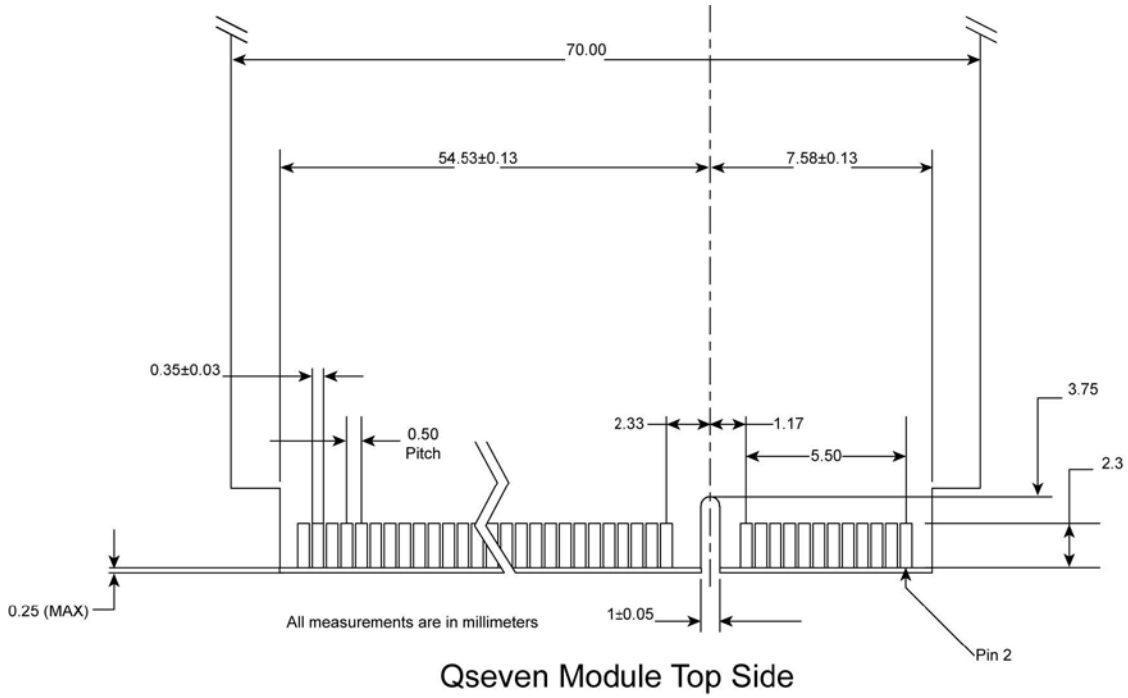
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9. Mechanical Information

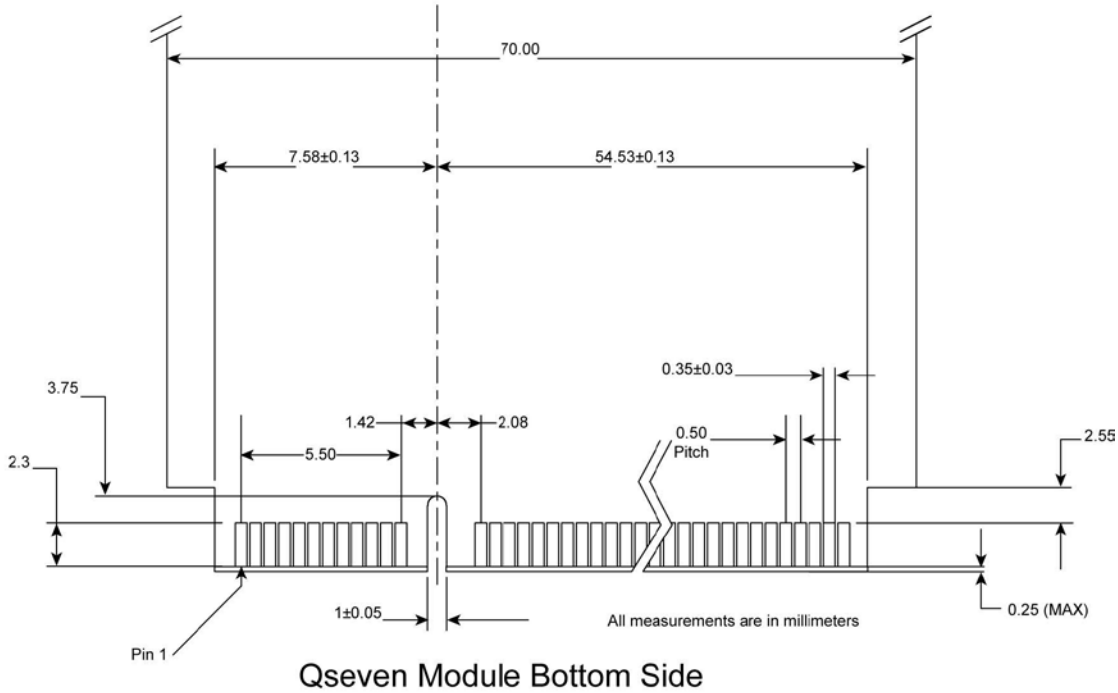
9.1. Board-to-Board Connector

The high-speed serialized Qseven edge connector is designed for ultra-low power CPUs and chipsets with ultra-low Thermal Design Power (TDP). Refer to the following illustration for the mechanical dimensions of the Qseven edge connector.

NOTE: The edge fingers found on the top and bottom sides of the Qseven connector are not mirrored and are therefore slightly offset.



Qseven Module Top Side



Qseven Module Bottom Side

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9.2. Thermal Solution

9.2.1. Heat Spreaders

The function of the heat spreader is to ensure an identical mechanical profile for all Qseven modules. By using a heat spreader, the thermal solution that is built on top of the module is compatible with all Qseven modules.

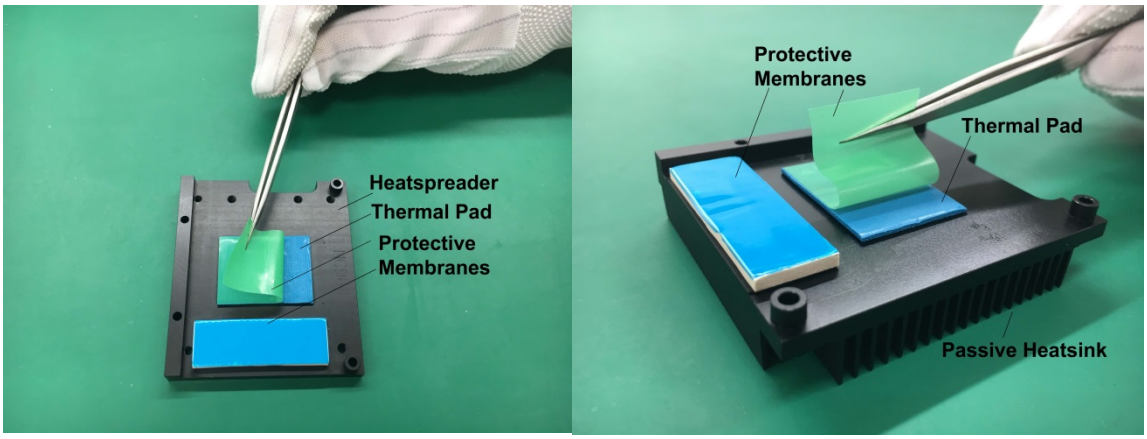
9.2.2. Heatsinks

A heatsink can be used as a thermal solution for a specific Qseven module and can have a fan or be fanless, depending on the thermal requirements.

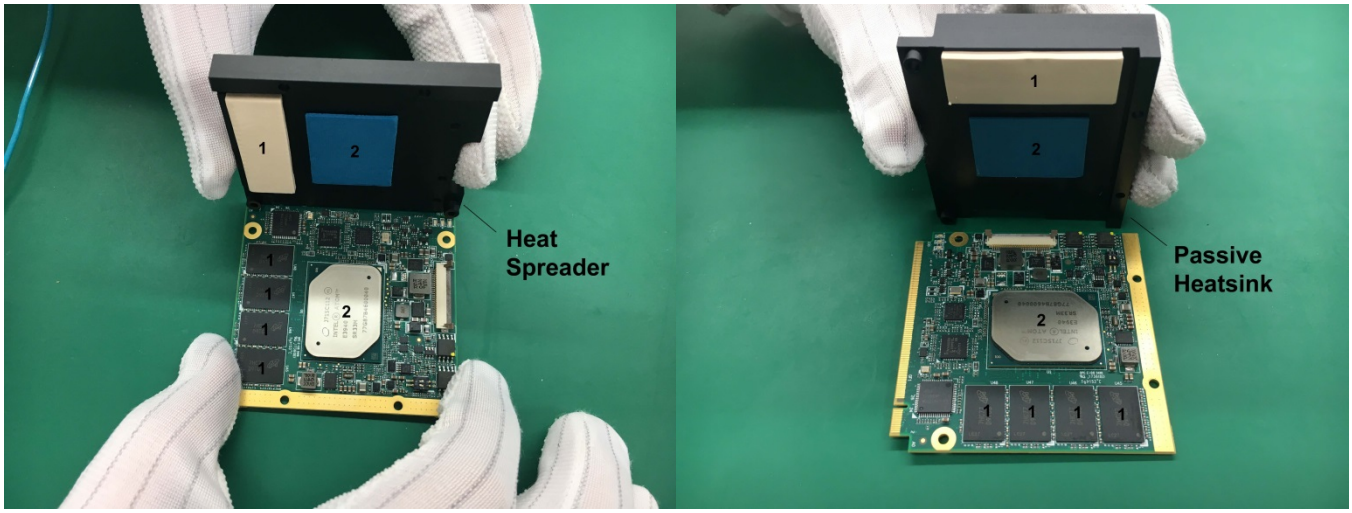
9.2.3. Installation

Install a heat spreader or passive heat sink using the following instructions.

Step 1: Remove the protective membranes from the thermal pads on the heat spreader or passive heatsink.

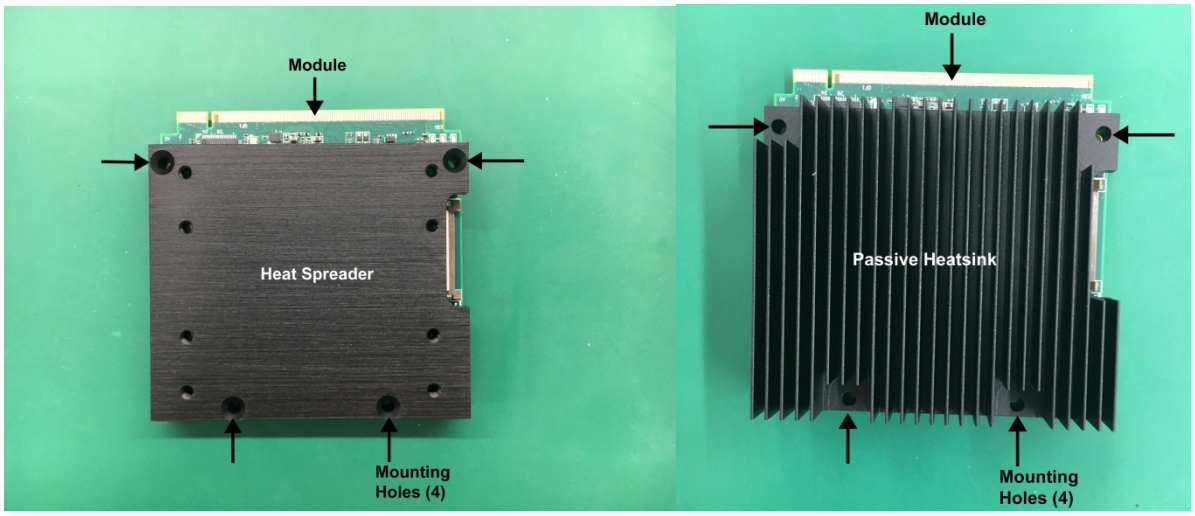


Step 3: Align the heat spreader or heatsink with the module so that the thermal pads on the heat spreader or heatsink line up with their respective components on the module as shown in the following illustrations.

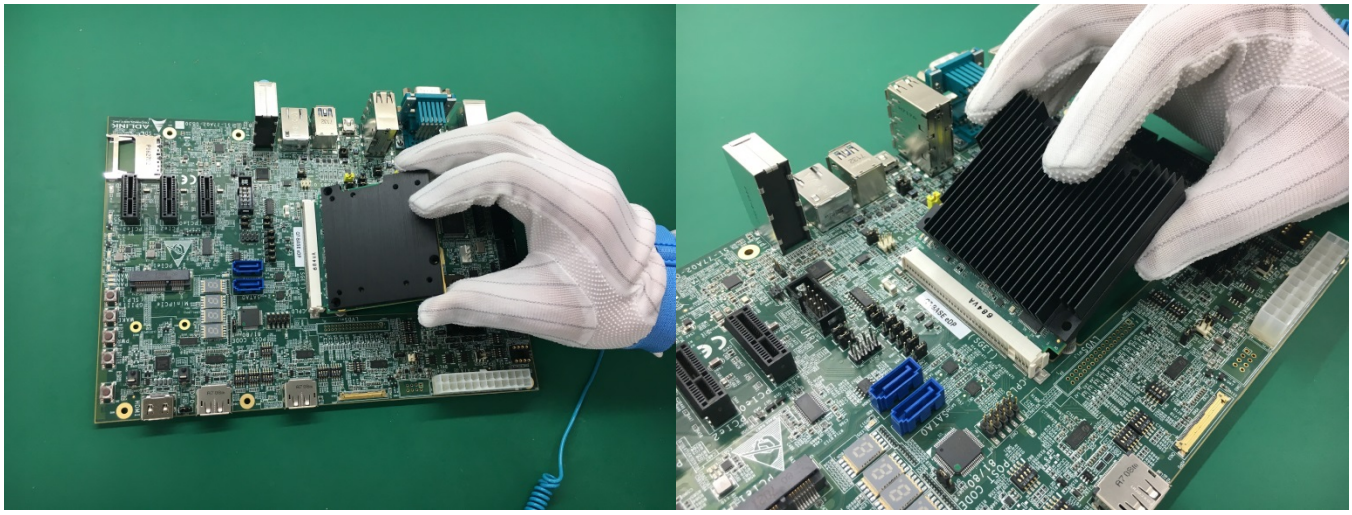


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Step 4: Lay the heat spreader or heatsink on the module so that the thermal pads on the heat spreader or heatsink completely cover their respective components on the module, and the mounting holes on the heat spreader or heatsink line up with the mounting holes on the module. See the following two photos.



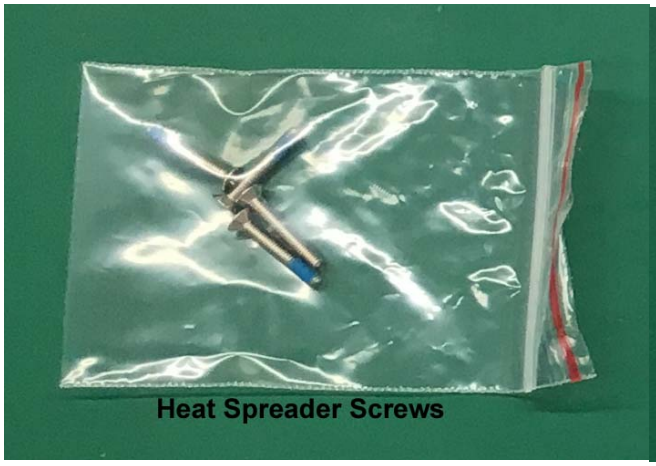
Step 5: Insert the Qseven module with mounted heat spreader or heatsink assembly into the Qseven edge connector on the carrier board as shown.



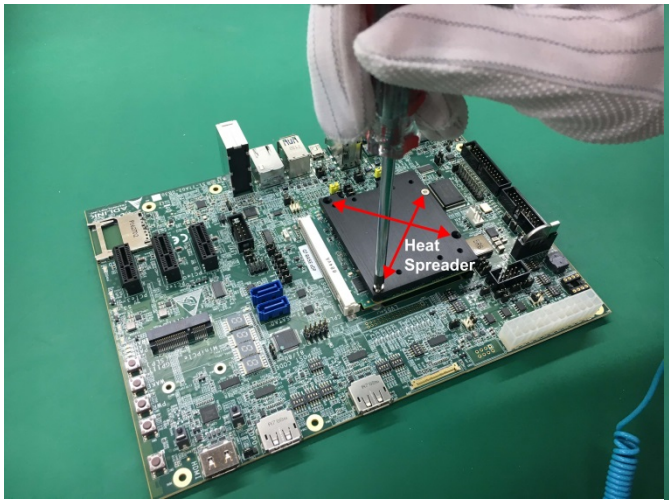
Insert the module until it is firmly seated in the carrier board connector.

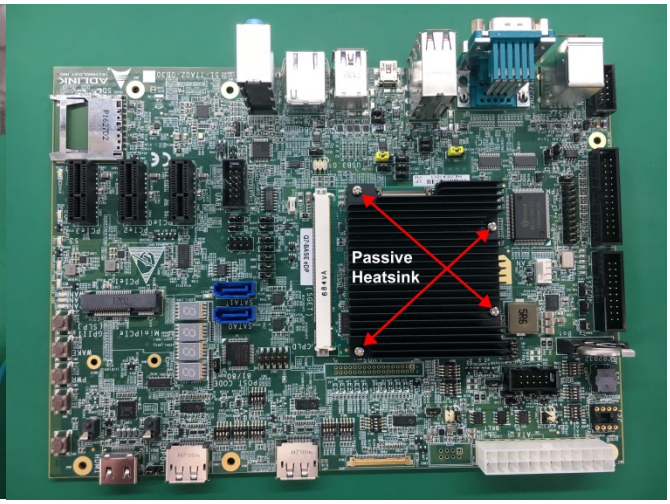
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Step 4: Use the four 2.7mm countersink screws provided to fasten the heat spreader or four 2.7mm panhead screws to fasten the passive heatsink to the module. Refer to the following four photos. Install the screws using an alternating installation sequence as the red arrows in the second two photos indicate.









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9.3. Mounting Requirements

Qseven modules accommodate Top mounting to the carrier board. In Top mounting, the threaded standoffs are on the carrier board and the thermal solution is equipped with through-hole standoffs. For mounting dimension requirements, refer to the following diagram from the Qseven 2.0 specification.

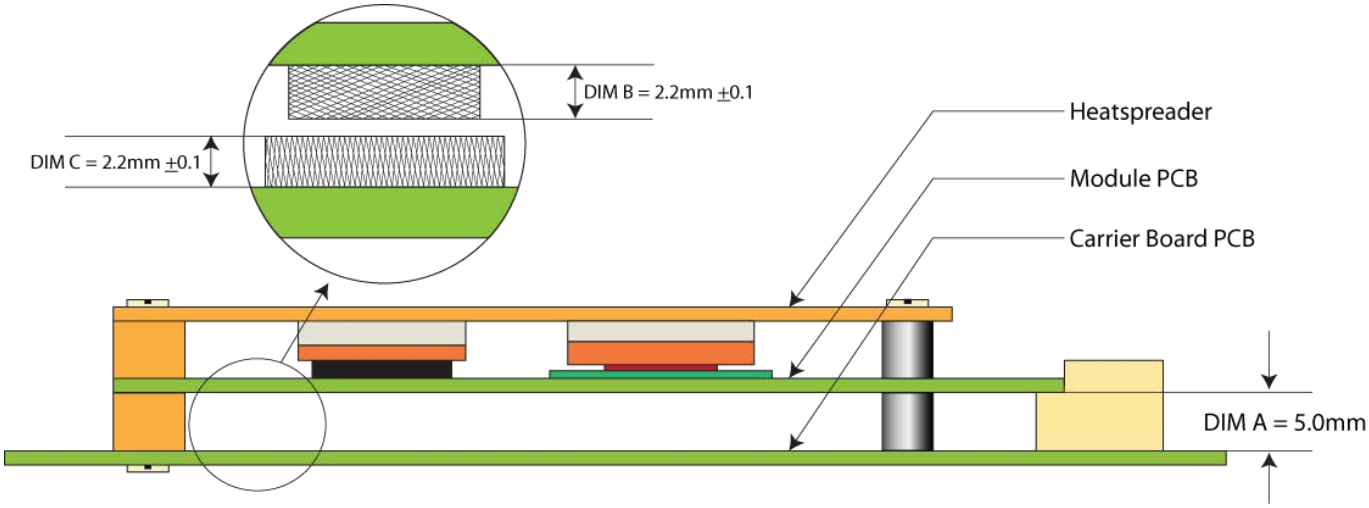


Figure 11: Qseven Mounting Requirements

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Safety Instructions

Read and follow all instructions marked on the product and in the documentation before you operate your system. Retain all safety and operating instructions for future use.

- Please read these safety instructions carefully.
- Please keep this User‘s Manual for later reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment, turn off the power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources.
  - Keep equipment away from high heat or high humidity.
  - Keep equipment properly ventilated (do not block or cover ventilation openings).
  - Make sure to use recommended voltage and power source settings.
  - Always install and operate equipment near an easily accessible electrical socket-outlet.
  - Secure the power cord (do not place any object on/over the power cord).
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings.
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.
- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

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Ask an Expert: http://askanexpert.adlinktech.com

ADLINK Technology, Inc.
Address: 9F, No.166 Jian Yi Road, Zhonghe District
New Taipei City 235, Taiwan
Tel: +886-2-8226-5877
Fax: +886-2-8226-5717
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
Address: 5215 Hellyer Avenue, #110, San Jose, CA 95138, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-360-0222
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
Address: 300 Fang Chun Rd., Zhangjiang Hi-Tech Park, Pudong New Area
Shanghai, 201203 China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

LiPPERT ADLINK Technology GmbH
Address: Hans-Thoma-Strasse 11, D-68163, Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

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