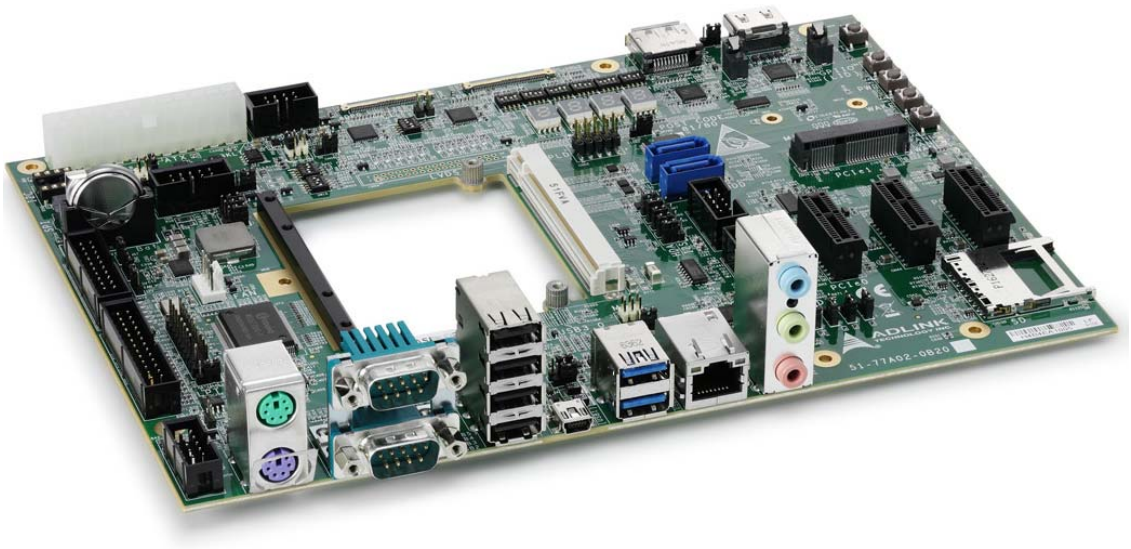
Q7-BASE

Technical Reference

Qseven Reference Carrier Board



Revision: 3.00
Revision Date: October 03, 2017
Part Number: 50-1Z180-1020

Leading **EDGE COMPUTING**

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Preface

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Revision History

Revision	Date	Description of Change(s)
1.00	April 2015	Initial Release
2.00	8/26/2016	Revised content to reflect new board layout
3.00	10/03/2017	Revised content to reflect Version 2.1 of the Qseven Specification

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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

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Important Safety Instructions

For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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Conventions

The following conventions may be used throughout this manual, denoting special levels of information.



This information adds clarity or specifics to text and illustrations.



This information indicates the possibility of ***minor*** physical injury, component damage, data loss, and/or program corruption.



This information warns of possible ***serious*** physical injury, component damage, data loss, and/or program corruption.

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1 Product Overview

This chapter presents a general overview of the Q7-BASE carrier. After reviewing this chapter you should understand the following features of the Q7-BASE carrier board.

- Carrier Description
- I/O Features
- Functional Block Diagram
- Carrier Specifications

1.1 Carrier Description

The ADLINK Q7-BASE is the host carrier board for ADLINK's Qseven modules and serves as design reference for systems based on the Qseven form factor. The Qseven module plugs directly into the Q7-BASE, where the carrier board becomes a design platform for testing and developing your applications. Figure 1-1 provides an overview photo of the Q7-BASE interface hardware. The proceeding sections and chapters in this manual present these features in further detail.

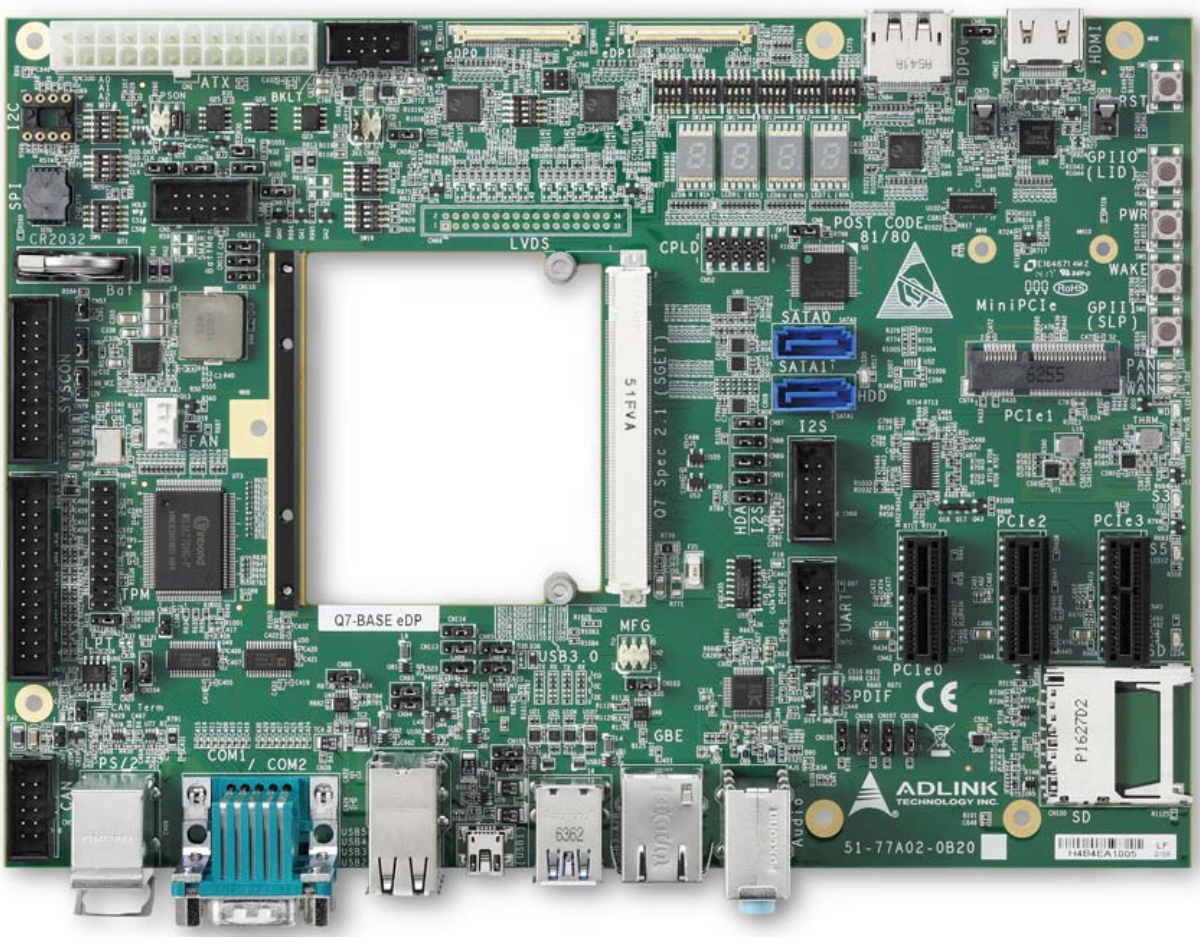


Figure 1-1: Q7-BASE IO Overview

The ADLINK Q7-BASE supports the features of Qseven Hardware Specification Version 2.1. The following section presents a list of features of the Q7-BASE.

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1.2 Features

- Qseven interface MXM connector
- PCI Express Bus
  - 4x PCIE x1 links
  - 3x PCIE x1 slots
  - 1x PCIE Mini slot
- Serial Port UART interfaces (2)
  - Null Modem RS-232 on serial ports COM1 / COM2
  - 4-wire connectors
  - COM1 / COM2 interfaces on two 9-pin, DB9 connectors
- USB interfaces
  - One USB, 4-connector stack for ports 2 through 5 (USB 2.0)
  - One USB dual connector for ports 0, 1, 6, and 7 (USB 2.0/3.0)
  - One mini-USB for USB 2.0 OTG or client
- Gigabit Ethernet interface
  - One standard RJ-45 connector
  - Activity/Link and Speed LED on Ethernet connector
- SDMMC interface
  - One SDMMC slot, 4.x (for SD card)
- Audio interfaces
  - Supports HD Audio and AC'97
  - One 3-in-1 stack audio jack for HD audio with Line In-Out / MIC
  - One 4-pin, digital audio header for SPDIF Input / Output
  - One I2S audio header
- Video interfaces
  - One dual-channel LVDS header (18/24-bit)
  - One LVDS backlight header
  - One standard DisplayPort connector
  - One standard HDMI connector
  - Two optional eDP connectors
- Power interface
  - One ATX Power In connector (all standard voltages available to baseboard headers)
  - +5 Volts needed to power Qseven module
  - One header for BattMan smart battery
- Fan interfaces
  - One fan power header
  - One fan function header
- SATA interfaces
  - Two standard SATA3 connectors
  - One SATA power LED
- CAN interface
  - One CAN header
- SPI System interfaces
  - One SPI System header

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- Miscellaneous
  - Smart Battery
  - RTC Battery Socket
  - Control Buttons and Switches

1.3 Ordering Information

Table 1-1: Q7-BASE Models

Model Number	Description
Q7-BASE LVDS (91-77A02-000E or higher)	Qseven Reference Carrier for Qseven compliant modules, featuring an MXM2 230-pin module interface with LVDS display support.
Q7-BASE eDP (91-77A02-010E or higher)	Qseven Reference Carrier for Qseven compliant modules, featuring an MXM2 230-pin module interface with eDP display support.

1.4 Block Diagram

Figure 1-2 presents a functional representation of the carrier.

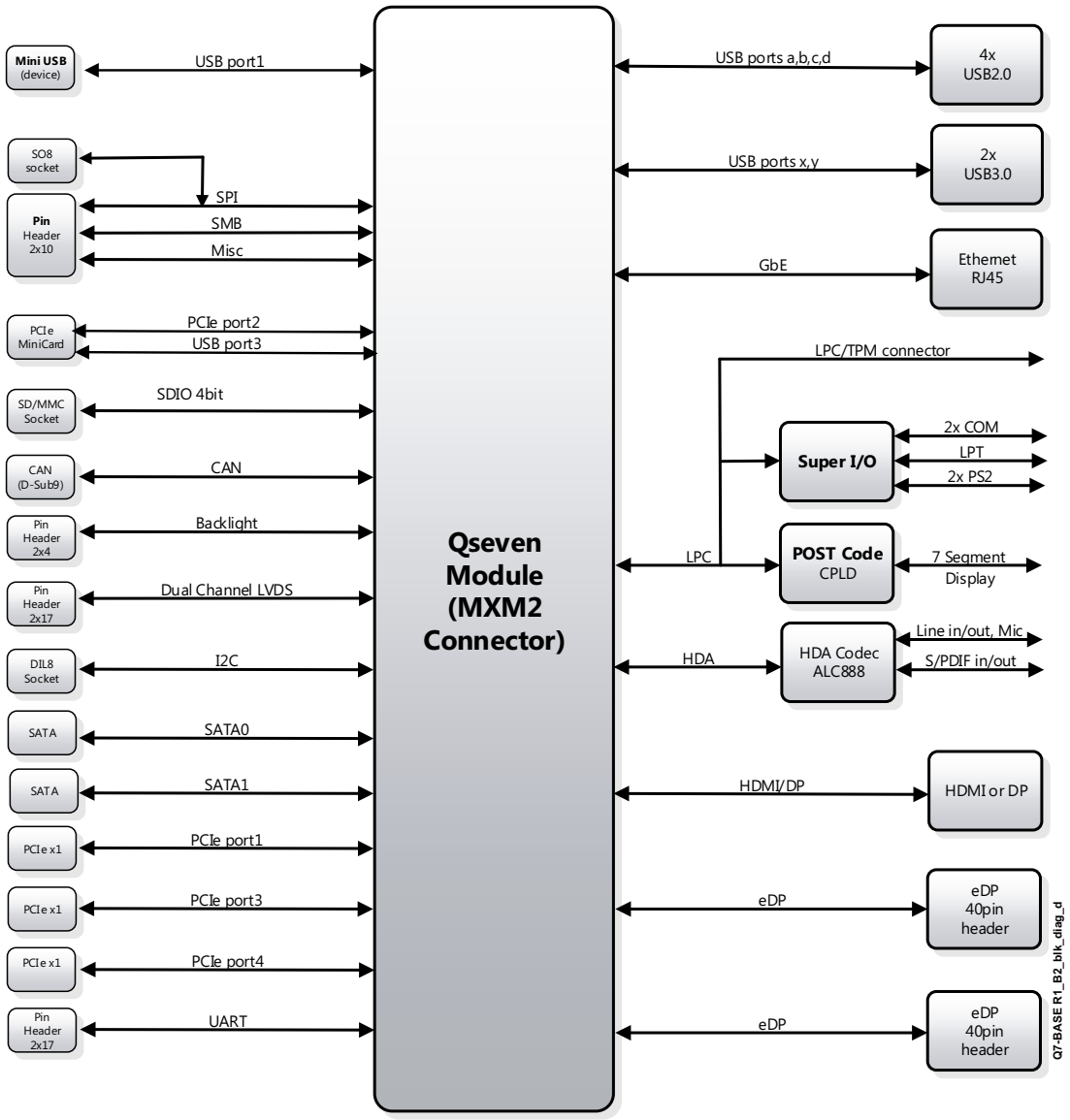


Figure 1-2: Functional Block Diagram

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1.5 Specifications

1.5.1 Physical

Table 1-2 lists the physical dimensions of the baseboard.

Table 1-2: Weight and Footprint Dimensions

Item	Dimension	
Weight	0.32 kg	Overall height is measured from the upper board surface to the top of the highest permanent component on the upper board surface. This measurement does not include the cooling solution, which can vary. The cooling solution will probably increase this dimension.
Height (overall)	38.00 mm	
PCB thickness	2.00 mm	
Width	170.00 mm	
Length	237.00 mm	

1.5.2 Electrical

Table 1-3 specifies the voltage input characteristics of the carrier.

Table 1-3: Carrier Voltage Inputs

Parameter	Value
Standard	12V +/-5% and 5V +/-5% from ATX connector
RTC Battery	3.0V, 2.4V to 3.3V (battery), +/-20mV ripple
BattMan Supply	12V +/-5% (3A max), 5.0V +/-5% (4A max), +/-50mV ripple

1.5.3 Environmental

Most components on the Q7-BASE carrier are selected as extended temperature range parts (-40°C to +85°C). Some components are not available in this temperature range. In these cases, the component temperature ranges are narrower. The Q7-BASE is validated in the -40°C to +85°C range.

The overall system performance depends on the combination of module and carrier subsystems. Some Qseven modules are available in the industrial temperature range. Others are commercial temperature range parts. Similar considerations apply to any of the add-on cards or peripherals that are used with the Q7-BASE.

Table 1-4 defines the environmental conditions under which the carrier is qualified to operate and to be stored.

Table 1-4: Validated Temperature and Humidity Ranges

Parameter	Temperature
Temperature ▶ Standard ▶ Storage	 ▶ -40°C to +85°C ▶ -55°C to +85°C
Humidity ▶ Operating ▶ Non-operating	 ▶ 5% to 90% relative humidity, non-condensing ▶ 5% to 95% relative humidity, non-condensing

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1.5.4 Mechanical

Figure 1-3 provides the mechanical dimensions and mounting hole sizes of the Q7-BASE. The Q7-BASE can be mounted to a chassis using M4, B-head screws. Mezzanine cards can be mounted to the carrier using female-female standoffs with M2.5 threads and M2.5, B-head screws.

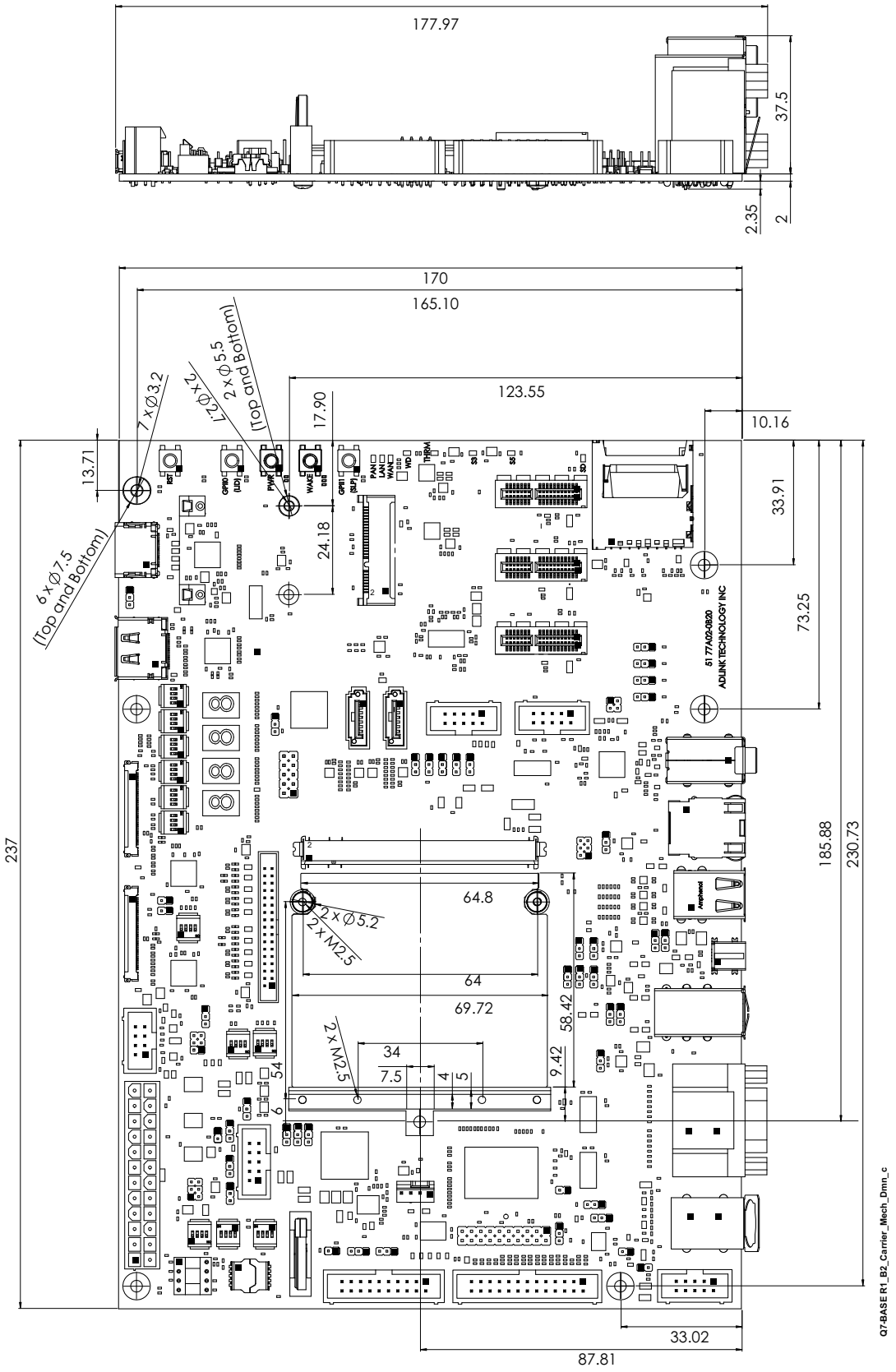


Figure 1-3: Mechanical Dimensions (Top Side)

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2 Hardware

This chapter describes the physical specifications of the interface connectors, headers, LEDs, and switches on the Q7-BASE. The third section of this chapter further describes the industry standard IO hardware on the carrier.

2.1 Interface Headers, Jumper Headers, Switches, LEDs, and Connectors

Table 2-1 describes the headers, switches, LEDs, and connectors for the Q7-BASE carrier shown in Figure 2-1 and Figure 2-3

Table 2-1: Header, Connector, Switch, and LED Descriptions

Header / Connector#	Signal / Device	Description
AJ1	Audio Jack	13-pin standard audio jack for three HD audio signals: Line In (Blue), Line Out (Green), and MIC In (Pink) [FOXXCONN, JA33331-HA1P-4F]
BT1	Battery Socket	3-pin, 220V socket for CR2032 battery that runs at 3V [LOTES, AAA-BAT-038-K01]
CN1	ATX Power	24-pin, 0.165" (4.2mm) ATX standard shrouded connector for ATX power signals [ALEX, 9359-24]
CN2	Manufacturing	6-pin, 2mm jumper header reserved for manufacturing use [JIHVEI, 27S1001-OPS35-01G-B, BLACK]
CN3	ATX / BattMan +5V Standby Select	3-pin, 2.0mm jumper header for selecting ATX or BattMan +5V Standby mode [JIH21N12050-03S10B-01G-4/2.8-G]
CN4	ATX / BattMan +5V Power Good Select	2-pin, 2.0mm jumper header for selecting ATX or BattMan +5V Power Good mode [JIH21N12050-02S10B-01G-4]
CN5	Smart Battery	10-pin, 2.54 box header for BattMan signals [JIHVEI, 23N6960-10S10B-01G-G, BLACK]
CN8	Post Code Enable	3-pin, 2.0mm jumper header for enabling or disabling Post Code 80h / 81h [JIH21N12050-03S10B-01G-4/2.8-G]
CN10	eDP0	40-pin, 0.5mm right-angle connector for embedded Display Port I/O (Featured on only the eDP version of the carrier) [I-PEX, 20455-040E-12]
CN11	eDP1	40-pin, 0.5mm right-angle connector for embedded Display Port I/O (Featured on only the eDP version of the carrier) [I-PEX, 20455-040E-12]
CN20	PS/2 Power Source Select	3-pin, 2.0mm jumper header for selecting PS/2 WAKE power source [JIH21N12050-03S10B-01G-4/2.8-G]
CN39	COM1/COM2	Dual 9-pin, 0.109" (2.77mm) standard DB9 connectors for COM1 and COM2 serial ports [FOXXCONN, DM10151-H531-4F]
CN42, CN44, CN45	PCI Express	36-pin, 0.039" (1mm) standard edge connector for PCI Express x1 interface [FOXXCONN, 2EG01817-D2D-DF]
CN46	Digital Audio	4-pin, 0.079" (2mm) header for incoming and outgoing SPDIF digital audio signals [SAMTEC, TMM-102-01-T-D-SM]

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Table 2-1: Header, Connector, Switch, and LED Descriptions (Continued)

Header / Connector#	Signal / Device	Description
CN50	CAN	10-pin, 0.100" (2.54mm) shrouded header for transmitting and receiving Controller Area Network signals [JIHVEI, 23N6960-10S10B-01G-G]
CN51	CAN Termination	2-pin, 0.079" (2mm) jumper header for terminating the CAN interface with 120 ohms [JIH, 21N12050-02S10B-01G-4/2.8-G]
CN52	CPLD Programming	10-pin, 0.100" (2.54mm) header for CPLD programming signals [SAMTEC, TSM-105-01-S-DV]
CN53	Fan Control	4-pin, 0.100" (2.54mm) header for system fan +12V power, power management, and tachometer [JVE, 24W1163-04S10-01T-02]
CN57	Battery Termination	2-pin, 0.079" (2mm) jumper header for connecting or disconnecting the battery in the BT1 socket [JIH, 21N12050-02S10B-01G-4/2.8-G]
CN59	Backlight Voltage Select	3-pin, 2.0mm jumper header for selecting +5V or +12V ATX Power On voltage to the LCD backlight [JIH21N12050-03S10B-01G-4/2.8-G]
CN61	Keyboard Controller Enable	2-pin, 0.079" (2mm) jumper header for selecting the keyboard controller SIO address [JIH, 21N12050-02S10B-01G-4/2.8-G]
CN62	LCD Voltage Select	6-pin, 0.079" (2mm) jumper header for LCD display power management to select 3V3, 5V, or 12V [NELTRON, 2208SM-06G-CR]
CN63	ATX PS_ON	6-pin, 0.079" (2mm) jumper header for setting Power Signal_ON for the ATX connector [NELTRON, 2208SM-06G-CR]
CN64	USB0 Voltage Select	3-pin, 0.079" (2mm) jumper header for selecting USB0 voltage source: Standby or Voltage In [JIH, 21N12050-03S10B-01G-4/2.8-G]
CN65	LVDS Backlight Interface	8-pin, 0.100" (2.54mm) shrouded header for LVDS backlight [JIHVEI, 23N6960-08S10B-01G-G]
CN66	LVDS Interface	34-pin, 0.079" (2mm) header for LVDS video [JIHVEI, 23N6850-34S10B-01G-G]
CN69	SIO Enable	3-pin, 0.079" (2mm) jumper header for enabling or disabling the SIO (1-2 = Enable; 2-3 = Disable) [JIH, 21N12050-03S10B-01G-4/2.8-G]
CN70	UART Interface	10-pin, 0.100" (2.54mm) shrouded header for high-speed, four-wire RS232 serial signals [JIHVEI, 23N6960-10S10B-01G-G]
CN71	LPT Interface	26-pin, 0.100" (2.54mm) shrouded header for parallel signals [JIHVEI, 23N6960-26S10B-01G-G]
CN73	System Interface	20-pin, 0.100" (2.54mm) shrouded header for system management signals [JIHVEI, 23N6960-20S10B-01G-G]
CN74	PCIe Mini	52-pin, 0.032" (0.80mm) standard socket for PCIe Mini cards [ATTEND, 119A-80A00-R02]

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Table 2-1: Header, Connector, Switch, and LED Descriptions (Continued)

Header / Connector#	Signal / Device	Description
CN75, CN76	PCIe Mini Latch	Dual latches for PCIe Mini card socket [ATTEND, 119A-LATCH-80]
CN77	CAN Enable 5V	2-pin, 0.079" (2mm) jumper header for enabling 5V on pin 9 of the CAN interface [JIH, 21N12050-02S10B-01G-4/2.8-G]
CN78	LPC / TPM Interface	20-pin, 0.100" (2.54mm) shrouded header for TPM signals [JIH, 21N22564-20S10B-01G-6]
CN79	FAN Voltage Select	3-pin, 0.079" (2mm) jumper header for selecting +5V or +12V ATX power for the system fan [JIH, 21N12050-03S10B-01G-4/2.8-G]
CN80	USB1 Voltage Select	3-pin, 2.0mm jumper header for selecting USB1 voltage source: Standby or Voltage In [JIH21N12050-03S10B-01G-4/2.8-G]
CN81	ATX_PWRGD Mode Select	3-pin, 2.0mm jumper header for selecting the mode of ATX Power Good (ATX or BattMan) [JIH21N12050-03S10B-01G-4/2.8-G]
CN84	DisplayPort, Standard	20-pin standard, right-angle connector for DisplayPort signals [FOXCONN, 3VD51203-D7JJ-7H, BLACK]
CN85	Display Mode Select, DP / HDMI	3-pin, 2.0mm jumper header for selecting between HDMI B and DP display mode [JIH21N12050-03S10B-01G-4/2.8-G]
CN86	I2S	10-pin, 2.54mm shrouded header for I2S signals [JIHVEI, 23N6960-10S10B-01G-G, BLACK]
CN87	HDA_SYNC / I2S_WS Select	3-pin, 2.0mm jumper header for selecting between HDA_SYNC and I2S_WS [JIH21N12050-03S10B-01G-4/2.8-G]
CN88	HDA_RST# / I2S_RST# Select	3-pin, 2.0mm jumper header for selecting between HDA_RST and I2S_RST [JIH21N12050-03S10B-01G-4/2.8-G]
CN89	HDA_BITCLK / I2S_CLK Select	3-pin, 2.0mm jumper header for selecting between HDA_BITCLK and I2S_CLK [JIH21N12050-03S10B-01G-4/2.8-G]
CN90	HDA_SDO / I2S_SDO Select	3-pin, 2.0mm jumper header for selecting between HDA_SDO and I2S_SDO [JIH21N12050-03S10B-01G-4/2.8-G]
CN91	HDA_SDI / I2S_SDI Select	3-pin, 2.0mm jumper header for selecting between HDA_SDI and I2S_SDI [JIH21N12050-03S10B-01G-4/2.8-G]
CN92	EN_V3P3S Mode Select	3-pin, 2.0mm jumper header for selecting between ATX mode and SUS_S3# [JIH21N12050-03S10B-01G-4/2.8-G]
CN93	USB3_CN_p / USB3_mPCIe_p Select	3-pin, 2.0mm jumper header for selecting between USB3_CN_p and USB3_mPCIe_p [JIH21N12050-03S10B-01G-4/2.8-G]
CN94	USB3_CN_n / USB3_mPCIe_n Select	3-pin, 2.0mm jumper header for selecting between USB3_CN_n and USB3_mPCIe_n [JIH21N12050-03S10B-01G-4/2.8-G]
CN95	USB OTG Power Control Select	3-pin, 2.0mm jumper header for selecting between USB_DRIVE_VBUS and USB_ID for OTG power [JIH21N12050-03S10B-01G-4/2.8-G]

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Table 2-1: Header, Connector, Switch, and LED Descriptions (Continued)

Header / Connector#	Signal / Device	Description
CN96	USB_VBUS Source Select	3-pin, 2.0mm jumper header for selecting between USB_VBUS and USB_CC [JIH21N12050-03S10B-01G-4/2.8-G]
CN97	PWM Backlight Voltage Select	3-pin, 2.0mm jumper header for selecting PWM backlight voltage level [JIH21N12050-03S10B-01G-4/2.8-G]
CN98	eDP1 Backlight Control	2-pin, 2.0mm jumper header for controlling eDP1 backlight [JIH21N12050-02S10B-01G-4/2.8-G]
CN99	eDP1 Backlight Enable	2-pin, 2.0mm jumper header for enabling eDP1 backlight [JIH21N12050-02S10B-01G-4/2.8-G]
CN100	SD-Card Slot	9-pin, 0.11" (2.8mm) standard, right-angle socket for SD cards [TYCO, 1939115-1, BLACK]
CN101	USB5_CN_p / USB5_20_p Select	3-pin, 2.0mm jumper header for selecting between USB3_CN_p and USB3_20_p [JIH21N12050-03S10B-01G-4/2.8-G]
CN102	USB5_CN_n / USB5_20_n Select	3-pin, 2.0mm jumper header for selecting between USB3_CN_n and USB3_20_n [JIH21N12050-03S10B-01G-4/2.8-G]
CN103	USB 3.0 Voltage Select	3-pin, 2.0mm jumper header for selecting USB 3.0 voltage source: Standby or Voltage In [JIH21N12050-03S10B-01G-4/2.8-G]
CN104	LRESET# Source Select	3-pin, 2.0mm jumper header for selecting between CB_RESET# and R/C [JIH21N12050-03S10B-01G-4/2.8-G]
CN105	ACT/LINK LED Source Select	3-pin, 2.0mm jumper header for selecting between GBE_LINK# and GBE_ACT#R/C [JIH21N12050-03S10B-01G-4/2.8-G]
CN106	ACT/LINK LED Anode Select	3-pin, 2.0mm jumper header for selecting between +V3P3A and GBE_ACT# [JIH21N12050-03S10B-01G-4/2.8-G]
CN107	1000Mbit Anode Select	3-pin, 2.0mm jumper header for selecting between GBE_LINK1000# and +V3P3A [JIH21N12050-03S10B-01G-4/2.8-G]
CN108	100Mbit Anode Select	3-pin, 2.0mm jumper header for selecting between GBE_LINK100# and +V3P3A [JIH21N12050-03S10B-01G-4/2.8-G]
CN109	ATX_PWRGD Source Select	3-pin, 2.0mm jumper header for selecting the source of ATX Power Good (+V5P0_SBY or +V5_IN#) [JIH21N12050-03S10B-01G-4/2.8-G]
CN110	SMB_ALERT_5V# Source Select	3-pin, 2.0mm jumper header for selecting between SMB_ALERT_5V# and SMB_ALERT# [JIH21N12050-03S10B-01G-4/2.8-G]
CN111	SMB_CLK_5V# Source Select	3-pin, 2.0mm jumper header for selecting between SMB_CLK_5V# and SMB_CLK# [JIH21N12050-03S10B-01G-4/2.8-G]
CN112	SMB_DATA_5V# Source Select	3-pin, 2.0mm jumper header for selecting between SMB_DATA_5V# and SMB_DATA# [JIH21N12050-03S10B-01G-4/2.8-G]
CN113	USB 2.0 OC# Target Select	3-pin, 2.0mm jumper header for selecting the OC target (USB45_OC# or USB67_OC#) [JIH21N12050-03S10B-01G-4/2.8-G]

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Table 2-1: Header, Connector, Switch, and LED Descriptions (Continued)

Header / Connector#	Signal / Device	Description
CN114	USB 3.0 OC# Target Select	3-pin, 2.0mm jumper header for selecting the OC target (USB01_OC# or USB67_OC#) [JIH21N12050-03S10B-01G-4/2.8-G]
HDMI1	HDMI Interface	19-pin, 0.019" (0.50mm) standard connector for HDMI video signals [TechBest, HDMI-KRPS00-A30N2A-L]
LED1	PCIe Mini WWAN	Yellow Activity LED for Wireless Wide Area Network (ON = low level) [LIGITEK, LG-170HY-CT]
LED2	PCIe Mini WLAN	Yellow Activity LED for Wireless Local Area Network (ON = low level) [LIGITEK, LG-170HY-CT]
LED3	PCIe Mini WPAN	Yellow Activity LED for Wireless Personal Area Network [LIGITEK, LG-170HY-CT] (ON = low level)
LED4	SDIO	Yellow Power LED for SD card socket (ON = high level) [LIGITEK, LG-170HY-CT]
LED5	SATA	Yellow Power LED for SATA interface (ON = low level) [LIGITEK, LG-170HY-CT]
LED6	POST 80 High	Seven-segment display LED for 80H POST codes (high nibble of address 80h) [Kingbright, KCSA02-101]
LED7	POST 80 Low	Seven-segment display LED for 80L POST codes (low nibble of address 80h) [Kingbright, KCSA02-101]
LED8	POST 81 High	Seven-segment display LED for 81H POST codes (high nibble of address 81h) [Kingbright, KCSA02-101]
LED9	POST 81 Low	Seven-segment display LED for 81H POST codes (low nibble of address 81h) [Kingbright, KCSA02-101]
LED11	S3 Suspend	Yellow Activity LED for S3 sleep state (ON = high level) [LIGITEK, LG-170HY-CT]
LED12	S5 Suspend	Yellow Activity LED for S5 sleep state (ON = high level) [LIGITEK, LG-170HY-CT]
LED13	Thermal Trip	Red Activity LED for thermal management (ON = low level) [Ligitek, LG-170HR-CT]
LED14	Watchdog	Red Activity LED for Watchdog Timer (ON = high level) [Ligitek, LG-170HR-CT]
PS1	Keyboard and Mouse	6-pin, dual standard, mini-DIN connector for PS/2 keyboard (bottom) and mouse (top) I/O [FOXCONN, MH11061-P36-4F]
RJ451	Gb Ethernet	16-pin standard, RJ45 connector with transformer and LED for Gigabit Ethernet [UDE, RT7-174AAM1A, BLACK]
SATA0	SATA	7-pin, 0.050" (1.27mm) standard connector for SATA0 interface [WIN WIN, WATM-07ABN4A3B8UW]
SATA1	SATA	7-pin, 0.050" (1.27mm) standard connector for SATA1 interface [WIN WIN, WATM-07ABN4A3B8UW]

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Table 2-1: Header, Connector, Switch, and LED Descriptions (Continued)

Header / Connector#	Signal / Device	Description
SW1	Reset Button	4-pin, 0.170" (4.3mm) push-button switch for asserting warm reset to the module [DIPTRONIC, DTSM-61N-V-T]
SW2	Sleep Button	4-pin, 0.170" (4.3mm) push-button switch for asserting sleep state to the module [DIPTRONIC, DTSM-61N-V-T]
SW3	Power Button	4-pin, 0.170" (4.3mm) push-button switch for turning on power to the Qseven module [DIPTRONIC, DTSM-61N-V-T]
SW4	LID Button	4-pin, 0.170" (4.3mm) push-button switch for asserting LID to the Qseven connector [DIPTRONIC, DTSM-61N-V-T]
SW5	WAKE Button	4-pin, 0.170" (4.3mm) push-button switch for asserting wake signal to the Qseven module [DIPTRONIC, DTSM-61N-V-T]
SW6	I2C EEPROM Address Select	4-pole, 0.050" (1.27mm)dip switch for configuring and write protecting I2C EEPROM address [DIPTRONICS, DHNF-04-T-Q-T]
SW9	SPI EEPROM	4-pole, 0.050" (1.27mm)dip switch for selecting SPI EEPROM interface [DIPTRONICS, DHNF-04-T-Q-T]
SW11	DP Control	4-pole, 0.050" (1.27mm)dip switch for configuring DisplayPort control [DIPTRONICS, DHNF-04-T-Q-T]
SW12	DP Enable	4-pole, 0.050" (1.27mm)dip switch for configuring DisplayPort enable [DIPTRONICS, DHNF-04-T-Q-T]
SW13	DP Operation	4-pole, 0.050" (1.27mm)dip switch for configuring DisplayPort operation [DIPTRONICS, DHNF-04-T-Q-T]
SW14	eDP0 Enable	4-pole, 0.050" (1.27mm)dip switch for configuring eDP0 enable [DIPTRONICS, DHNF-04-T-Q-T]
SW15	eDP0 Operation	4-pole, 0.050" (1.27mm)dip switch for configuring eDP0 operation [DIPTRONICS, DHNF-04-T-Q-T]
SW16	eDP0 Control	4-pole, 0.050" (1.27mm)dip switch for configuring eDP0 control [DIPTRONICS, DHNF-04-T-Q-T]
SW17	eDP1 Enable	4-pole, 0.050" (1.27mm)dip switch for configuring eDP1 enable [DIPTRONICS, DHNF-04-T-Q-T]
SW18	eDP1 Operation	4-pole, 0.050" (1.27mm)dip switch for configuring eDP1 operation [DIPTRONICS, DHNF-04-T-Q-T]
SW19	eDP1 Control	4-pole, 0.050" (1.27mm)dip switch for configuring eDP1 control [DIPTRONICS, DHNF-04-T-Q-T]
SW20	I2C EEPROM Interface Select	4-pole, 0.050" (1.27mm)dip switch for configuring I2C EEPROM interface select [DIPTRONICS, DHNF-04-T-Q-T]

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Table 2-1: Header, Connector, Switch, and LED Descriptions (Continued)

Header / Connector#	Signal / Device	Description
USB1	USB 2.0	16-pin, 0.138" (3.50mm) quadruple-stacked, standard connector for USB 2.0 signals (ports 2, 3, 4, 5) [FOXCONN,UB1112C-QHDF-4F]
USB2	Mini USB 2.0	5-pin, 0.80mm standard Mini USB connector for USB 2.0 device (OTG or client) signals (port1) [AMP, 1734035-4, BLACK]
USB3	USB 3.0/2.0 [top] USB 2.0 [bottom]	18-pin, standard dual USB 3.0 / 2.0 connectors for USB interface ports 0, 1, 6, and 7 [Amphenol, GSB3112311HR, BLUE]

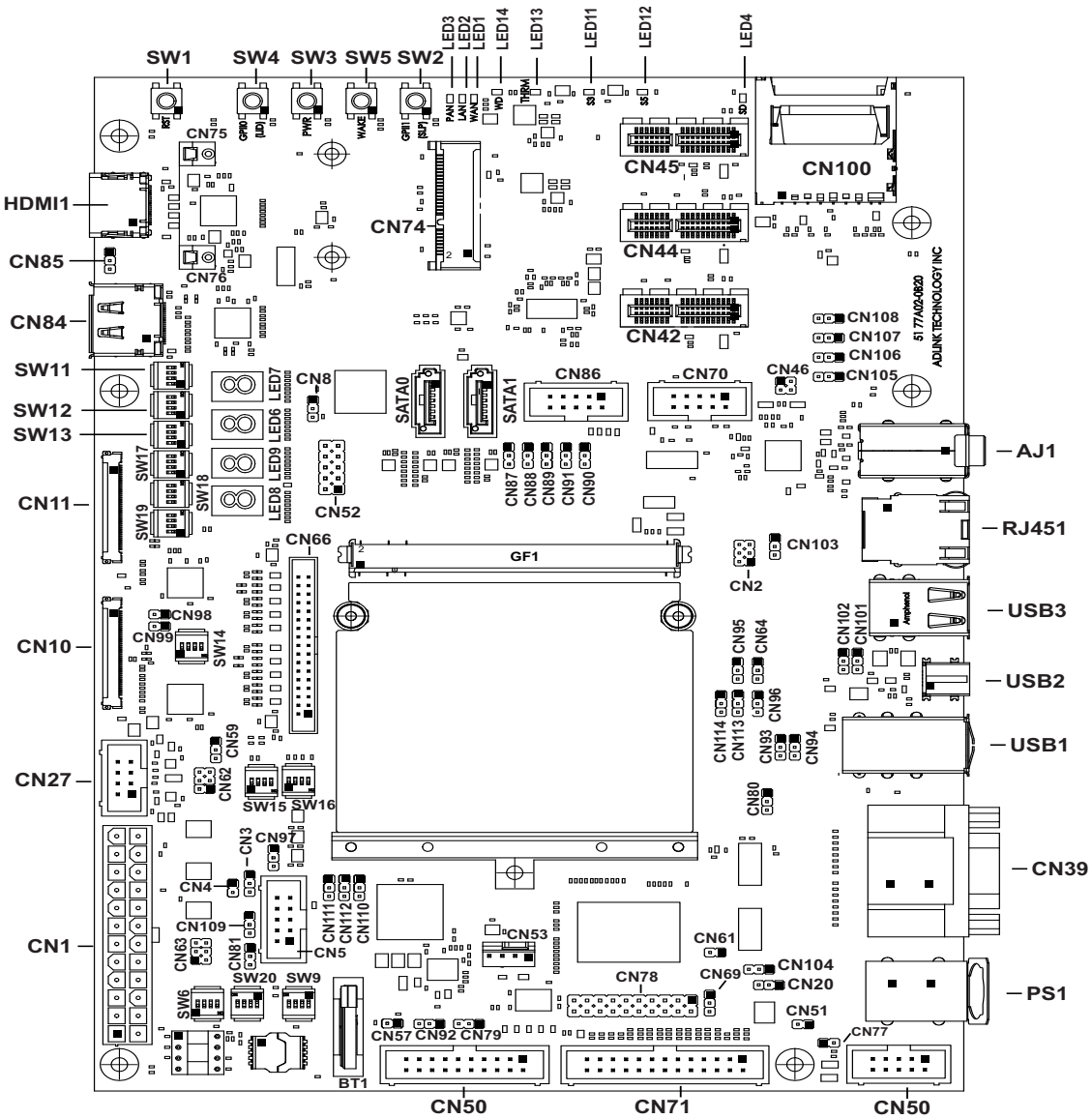


Figure 2-1: Connector Locations (Top Side)

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CONNECTORS:

AJ1 - Audio Jack
BT1 - Battery Socket
CN1 - ATX Power
CN2 - Manufacturing
CN3 - BattMan / ATX Power Mode Select
CN4 - BattMan / ATX Power Mode Select
CN5 - Smart Battery
CN8 - Post Code Enable
CN10 - eDP 0
CN11 - eDP 1
CN20 - PS/2 Power Source Select
CN39 - COM1/COM2 (standard connector)
CN42 - PCI Express (slot 1)
CN44 - PCI Express (slot 2)
CN45 - PCI Express (slot 3)
CN46 - Digital Audio
CN50 - CAN Interface
CN51 - CAN Termination
CN52 - CPLD Programming
CN53 - FAN control
CN57 - Battery Termination
CN59 - Backlight Voltage Select
CN61 - Enable Keyboard Controller
CN62 - LCD Voltage Select
CN63 - ATX PS_ON Select
CN64 - USB0 Voltage Select
CN65 - LVDS Backlight
CN66 - LVDS Interface
CN69 - SIO Enable
CN70 - UART Interface
CN71 - LPT Interface
CN72 - SD/MMC 4.x Slot
CN73 - System Interface
CN74 - PCIe Mini Card Slot
CN75 - PCIe Mini Latch
CN76 - PCIe Mini Latch
CN77 - CAN Enable 5V
CN78 - LPC / TPM Interface
CN79 - FAN Power Select
CN80 - USB1 Voltage Select
CN81 - ATX_PWRGD Mode Select
CN84 - DP Interface
CN85 - Display Mode Select
CN86 - I2S Interface
CN87 - HDA_SYNC or I2S_WS Select
CN88 - HDA_RST or I2S_RST Select
CN89 - HDA_BITCLK or I2S_CLK Select
CN90 - HDA_SDO or I2S_SDO Select
CN91 - HDA_SDI or I2S_SDI Select
CN92 - EN_V3P3S Mode Select
CN93 - USB3_CN_p or USB3_mPCIe_p Select
CN94 - USB3_CN_n or USB3_mPCIe_n Select
CN95 - USB OTG Control Select
CN96 - USB_VBUS Source Select
CN97 - Backlight Voltage Select
CN98 - eDP Backlight Control
CN99 - eDP Backlight Enable
CN100 - SD Card Slot
CN101 - USB5_CN_p or USB5_20_p Select
CN102 - USB5_CN_n or USB5_20_n Select
CN103 - USB 3.0 Voltage Select
CN104 - LRESET# Source Select
CN105 - ACT/LINK LED Source Select
CN106 - ACT/LINK LED Anode Select
CN107 - 1000Mbit Anode Select
CN108 - 100Mbit Anode Select
CN109 - ATX_PWRGD Source Select
CN110 - SMB_ALERT_5V# Source Select
CN111 - SMB_CLK_5V# Source Select
CN112 - SMB_DATA_5V# Source Select
CN113 - USB 2.0 OC# Target Select
CN114 - USB 3.0 OC# Target Select
HDMI1 - HDMI Socket
PS1 - PS/2 Keyboard and Mouse
RJ451 - Gb Ethernet (Standard)
SATA0 - SATA (Standard)
SATA1- SATA (Standard)
USB1 - USB 2.0 (Standard)
USB2 - Mini USB (Standard
USB3 - USB 3.0 / USB 2.0 (Standard)

SWITCHES:

SW1 - Reset Button
SW2 - Sleep Button
SW3 - Power Button
SW4 - LID Button
SW5 - Wake Button
SW6 - I2C EEPROM Address
SW9 - SPI EEPROM Interface Select
SW11 - DP Control
SW12 - DP Enable
SW13 - DP Operation
SW14 - eDP0 Enable
SW15 - eDP0 Operation
SW16 - eDP0 Control
SW17 - eDP1 Enable
SW18 - eDP1 Operation
SW19 - eDP1 Control
SW20 - I2C EEPROM Interface Select

LEDs:

LED1 - PCIe Mini WWAN
LED2 - PCIe Mini WLAN
LED3 - PCIe Mini WPAN
LED4 - SD/MMC
LED5 - SATA Activity
LED6 - POST 80 High
LED7 - POST 80 Low
LED8 - POST 81 High
LED9 - POST 81 Low
LED11 - S3 Suspend
LED12 - S5 Suspend
LED13 - Thermal Trip
LED14 - Watchdog

Q7-BASE R1_B2_top_conn_refkey_a

Figure 2-2: Reference Key for Headers, Connectors, Switches, and LEDs

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Figure 2-3 illustrates the faces of the standard interface connectors mounted along one edge of the carrier. These connectors are for PS1 Keyboard and Mouse, Serial Port, USB, Ethernet, and Audio industry-standard cable connectors.

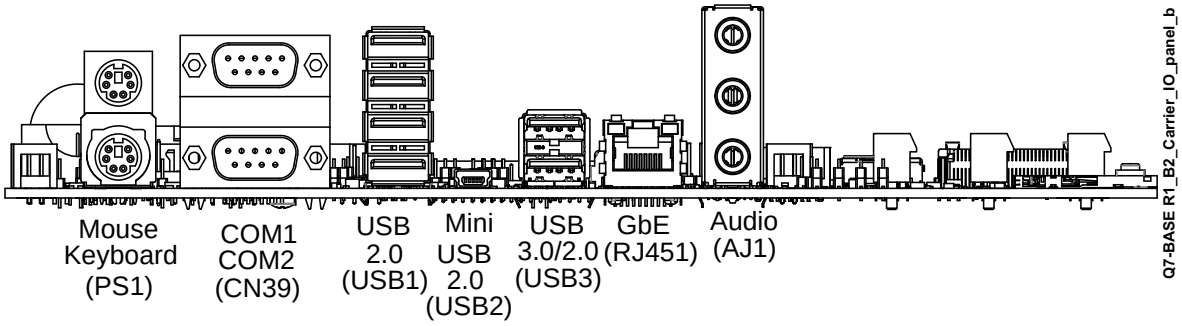


Figure 2-3: IO Panel Connector Locations

Figure 2-4 illustrates the faces of the standard interface connectors mounted along the opposite edge of the carrier shown in Figure 2-3. These connectors are for HDMI, DisplayPort, and embedded DisplayPort industry-standard cable connectors.

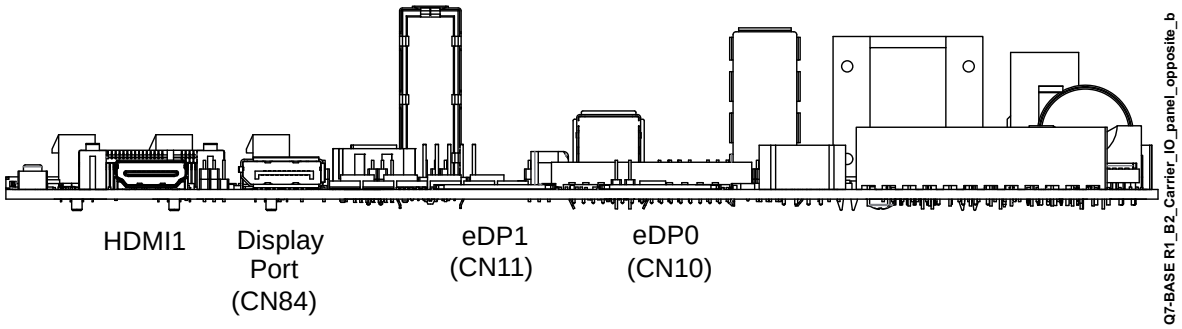


Figure 2-4: IO Panel Connector Locations (opposite side)

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2.2 Standard Hardware References

This section further describes the supported features of the Q7-BASE standard, on-board hardware.

2.2.1 Audio IO Jack

The Q7-BASE provides one standard audio jack for HD audio (AJ1). One audio codec supports this interface. Figure 2-5 depicts the three lines of the audio jacks: Line In (1 - Blue), Line Out (2 - Green), and MIC In (3 - Pink). Figure 2-6 presents the functional block diagram of HDA/I2S signals and hardware on the carrier.

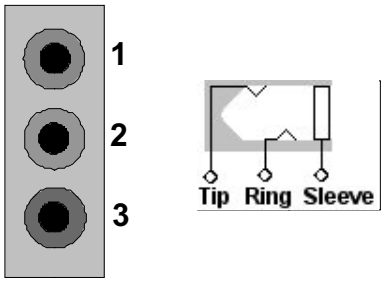


Figure 2-5: Stereo Jack Configuration

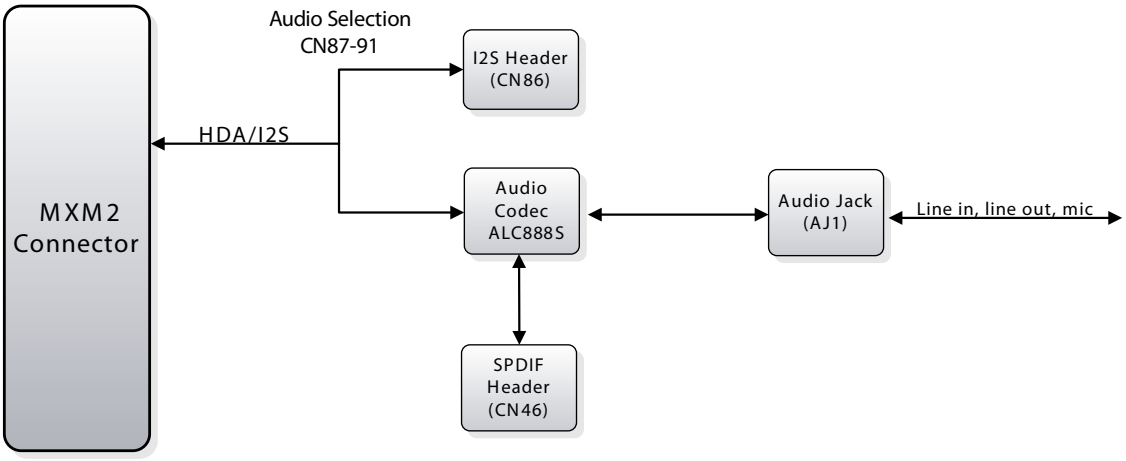


Figure 2-6: Audio Block Diagram

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2.2.2 PCIe Mini Card Slot

The Q7-BASE is equipped with one PCI Express Mini Card slot (CN74). Figure 2-7 presents the mini card slot with one of the two fastening latches.

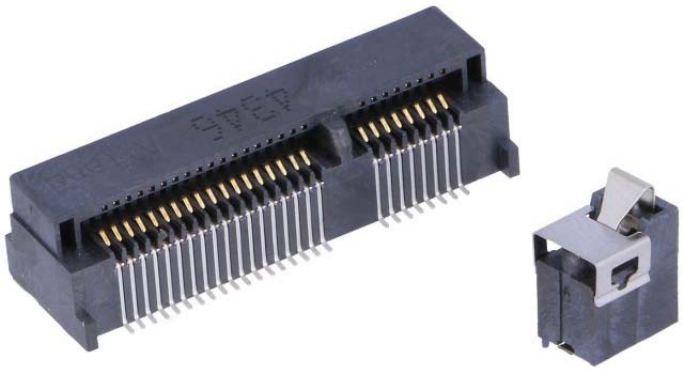


Figure 2-7: PCIe Mini Card Slot with Latch

2.2.3 SD Card Slot

The SD Card slot (CN100) provides the standard 4-bit, push-push interface for SD memory cards. LED5 provides indication of SD power.

NOTE:

UHS cards with 1.8V data signaling are supported. The card supply is always 3.3V regardless if either 1.8V signaling or 3.3V signaling is committed by both card controllers. The SoC and the SD card will agree on which standard they are compatible and will choose the appropriate standard.

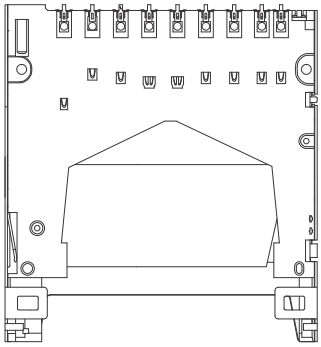
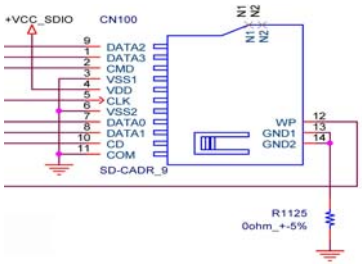


Figure 2-8: SD Card Slot

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Table 2-2: SD Card Slot (CN100)

Pin #	Signal	Description	Scheme
1	SDIO_D3	SDIO data bit3	
2	SDIO_CMD	SDIO Command	
3	GND	Ground	
4	+VCC_SDIO	3.3V power supply	
5	SDIO_CK	SDIO clock	
6	GND	Ground	
7	SDIO_D0	SDIO data bit0	
8	SDIO_D1	SDIO data bit1	
9	SDIO_D2	SDIO data bit2	
10	SDIO_CD#	SDIO card detect	
11	GND	Ground	
12	SDIO_WP	SDIO write protect	

Note: Shaded table cells denote power or ground.

2.2.4 Battery Socket

One vertical, AAA battery socket provides power for an external RTC coin cell battery. Figure 2-9 illustrates the top and side views of the socket. Table 2-3 provides the signals for socket.

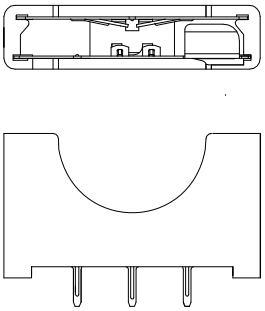


Figure 2-9: Battery Socket

Table 2-3: Battery Socket (BT1)

Pin #	Signal	Description
1	3V_BAT	+3 volts power for RTC
2	GND	Ground
3	3V_BAT	+3 volts power for RTC

Note: Shaded table cells denote power or ground. Jumper required on CN46 to enable the RTC.



A CR2032 battery may explode if incorrectly installed. Replace only with the same or equivalent type recommended by the socket manufacturer.

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3 Interfaces

This chapter provides the pin signals for all the non-standard user interfaces on the Q7-BASE. Unless pinouts for industry standard interfaces have been modified, those pinout tables will not appear in this manual. Signal definitions for standard interfaces such as SATA, USB, and PCIe connectors can be found in their respective specification data sheets.



The tables in this section define pin sequence using the method in the following example: A 10-pin header with two rows of pins, using odd/even numbering, where pin 2 is directly across from pin 1, is noted as **10 pins, 2 rows, odd/even pin sequence (1, 2)**. Consecutive numbering is noted, for example, as **24 pins, 2 rows, consecutive pin sequence (1, 13)**, where pin 13 is directly across from pin 1. Refer to Figure 2-1 for pin-1 locations.

3.1 ATX Power (CN1)

Table 3-1 lists the signals of the standard ATX Power connector, which provides 24 pins, 2 rows, consecutive pin sequence (1, 13) with 4.20mm pitch. Use the SW3 button switch on the carrier to apply power to the module.

Table 3-1: ATX Power Signals (CN1)

Pin#	Signal	Description	Pin#	Signal	Description
1	+V3P3_ATX	Power Supply DC voltage	13	+V3P3_ATX	Power Supply DC voltage
2	+V3P3_ATX	Power Supply DC voltage	14	NC	Not Connected
3	GND	Ground	15	GND	Ground
4	+V5P0_ATX	Power Supply DC voltage	16	ATX_PS_ON#	Switch to turn on power supply, shorted to Ground
5	GND	Ground	17	GND	Ground
6	+V5P0_ATX	Power Supply DC voltage	18	GND	Ground
7	GND	Ground	19	GND	Ground
8	ATX_PWRGD_5V	Status from the power supply, notifying the computer that the DC operating voltages are within the required ranges	20	NC	Not Connected
9	+V5P0_SBY	Power Supply Standby DC voltage	21	+V5P0_ATX	Power Supply DC voltage
10	+V12P0_ATX	Power Supply DC voltage	22	+V5P0_ATX	Power Supply DC voltage
11	+V12P0_ATX	Power Supply DC voltage	23	+V5P0_ATX	Power Supply DC voltage
12	+V3P3_ATX	Power Supply DC voltage	24	GND	Ground

NOTE: Shaded table cells denote power or ground. The # symbol indicates the signal is Active Low.

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3.2 Manufacturing (CN2)

Table 3-2 lists the pin signals of the Manufacturing header, which provides 6 pins, 2 rows, with odd/even pin sequence (1, 2) and 0.079" (2.00mm) pitch.

Table 3-2: Manufacturing (CN2)

Pin #	Signal	Pin #	Signal
1	MFG_NC0 (Reserved for manufacturing and debugging)	2	MFG_NC1 (Reserved for manufacturing and debugging)
3	MFG_NC2 (Reserved for manufacturing and debugging)	4	MFG_NC3 (Reserved for manufacturing and debugging)
5	MFG_NC4 (Reserved for manufacturing and debugging)	6	GND

3.3 ATX / BattMan +5V Standby Mode Select (CN3)

Table 3-3 lists the pin signals of the ATX / BattMan +5V Standby mode select jumper header, which provides 3 pins with 0.079" (2.00mm) pitch.

Table 3-3: ATX / Battman +5V Standby Mode Select (CN3)

Pin #	Signal	Jumper Position
1	+V5P0_SBY	• Jumper Installed (1-2) - ATX +5V Standby selected (**Default**) • Jumper Installed (2-3) - BattMan +5V Standby selected
2	5V0_SBY_OFF	
3	ATX_PS_ON#	

NOTE: Shaded table cell denotes ground.

3.4 ATX / BattMan +5V Power Good Mode Select (CN4)

Table 3-4 lists the pin signals of the ATX / BattMan +5V Power Good mode select jumper header, which provides 2 pins with 0.079" (2.00mm) pitch.

Table 3-4: ATX / Battman +5V Power Good Mode Select (CN4)

Pin #	Signal	Jumper Position
1	ATX_PWRGD_5V	• Jumper Installed (1-2) - ATX +5V Power Good selected (**Default**) • Jumper Removed - BattMan +5V Power Good selected
2	GND	

NOTE: Shaded table cell denotes ground.

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3.5 Smart Battery (BattMan) Interface (CN5)

Table 3-5 lists the pin signals of the Smart Battery header, which provides 10 pins in 2 rows, odd/even pin sequence (1, 2), and 2.54mm pitch.



You must configure the jumper settings as described in Table 3-5, or system damage could occur when using a BattMan power supply to Power On the carrier.

Table 3-5: Smart Battery (BattMan) Interface (CN5)

Pin #	Signal	Jumper Settings
1	SMB_CLK_5V (SMBus clock)	Make sure to set the following jumper configurations before implementing a BattMan power supply to Power On the carrier: • Remove the jumper from the 2-pin jumper header, **CN3** (Select +5V Standby) • Remove the jumper from the 2-pin jumper header, **CN4** (Select +5V Power Good) • Install a jumper on pins 1-2 of the **CN81** jumper header (ATX_PWRGD)
2	SMB_DAT_5V (SMBus data)	
3	Not Connected	
4	Not Connected	
5	ATX_PS_ON# (ATX power supply)	
6	Not Connected	
7	+V12P0_ATX (12-volt power)	
8	+V5P0_SBY (5-volt standby power)	
9	SMB_ALERT_5V# (SMBus alert)	
10	GND	

NOTE: The # symbol indicates the signal is Active Low. Shaded table cells denote power or ground.

3.6 Post Code Enable (CN8)

Table 3-6 lists the pin signals of the Post Code Enable jumper header, which provides 3 pins in a single row with 0.079" (2.00mm) pitch.

Table 3-6: Post Code Enable (CN8)

Pin #	Signal	Jumper Position
1	LPC_CLK_POST	• Jumper Installed 1-2 - Post Code enabled (**Default**) • Jumper Installed 2-3 - Post Code disabled
2	POST_CLK	
3	GND	

NOTE: The shaded table cells denote ground.

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3.7 eDP Display

The following two subsections describe the embedded DisplayPort interface available on the Q7-BASE eDP version of the board. See Figure 3-1 for a display signal map of the Q7-BASE eDP model.

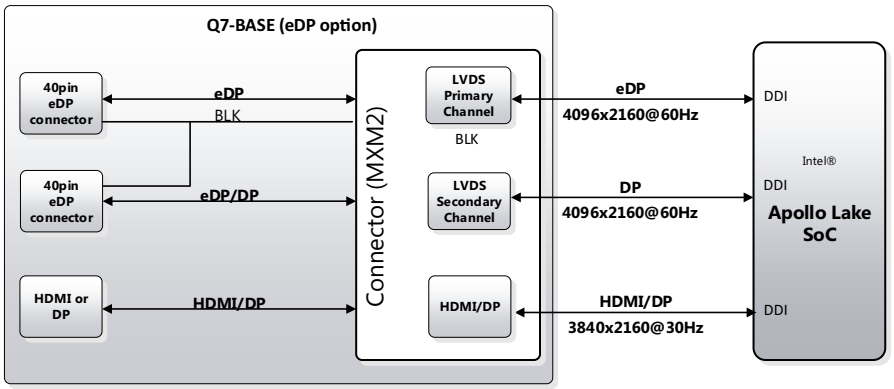


Figure 3-1: eDP Mapping Block Diagram

3.7.1 eDP0 (CN10)

Table 3-7 lists the pin signals of the embedded DisplayPort 0 connector, which provides 40-pins, single row with 0.5mm pitch.

Table 3-7: eDP0 Video Signals (CN10)

Pin #	Signal	Description
1	NC	Not Connected
2	eDP0_BKLT_PWR	Backlight power (5V / 12V [selected at CN59])
3	eDP0_BKLT_PWR	Backlight power (5V / 12V [selected at CN59])
4	eDP0_BKLT_PWR	Backlight power (5V / 12V [selected at CN59])
5	eDP0_BKLT_PWR	Backlight power (5V / 12V [selected at CN59])
6	NC	Not Connected
7	NC	Not Connected
8	eDP0_BKLT_PWM	Backlight brightness via pulse width modulation (PWM)
9	eDP0_BKLT_ENABLE	Backlight power enable
10	eDP0_BKLT_GND	Backlight ground
11	eDP0_BKLT_GND	Backlight ground
12	eDP0_BKLT_GND	Backlight ground
13	eDP0_BKLT_GND	Backlight ground
14	eDP0_HPD	Hot Plug Detect
15	eDP0_LCD_GND	LCD ground
16	eDP0_LCD_GND	LCD ground
17	eDP0_LCD_GND	LCD ground
18	eDP0_LCD_GND	LCD ground
19	NC	Not Connected
20	eDP0_LCD_VCC	LCD power (3.3V / 5V / 12V)
21	eDP0_LCD_VCC	LCD power (3.3V / 5V / 12V)

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Table 3-7: eDP0 Video Signals (CN10) (Continued)

Pin #	Signal	Description
22	eDP0_LCD_VCC	LCD power (3.3V / 5V / 12V)
23	eDP0_LCD_VCC	LCD power (3.3V / 5V / 12V)
24	eDP0_HS_GND	High-Speed Ground
25	eDP0_AUX_n	Auxiliary differential pair - negative
26	eDP0_AUX_p	Auxiliary differential pair - positive
27	eDP0_HS_GND	High-Speed Ground
28	eDP0_TX0_p	Lane 0 Display Port primary channel differential pair 0 - positive
29	eDP0_TX0_n	Lane 0 Display Port primary channel differential pair 0 - negative
30	eDP0_HS_GND	High-Speed Ground
31	eDP0_TX1_p	Lane 1 Display Port primary channel differential pair 1 - positive
32	eDP0_TX1_n	Lane 1 Display Port primary channel differential pair 1 - negative
33	eDP0_HS_GND	High-Speed Ground
34	eDP0_TX2_p	Lane 2 Display Port primary channel differential pair 2 - positive
35	eDP0_TX2_n	Lane 2 Display Port primary channel differential pair 2 - negative
36	eDP0_HS_GND	High-Speed Ground
37	eDP0_TX3_p	Lane 3 Display Port primary channel differential pair 3 - positive
38	eDP0_TX3_n	Lane 3 Display Port primary channel differential pair 3 - negative
39	eDP0_HS_GND	High-Speed Ground
40	NC	Not Connected

NOTE: The shaded table cells denote power or ground.

3.7.2 eDP1 (CN11)

Table 3-8 lists the pin signals of the embedded DisplayPort 1 connector, which provides 40-pins, single row with 0.5mm pitch.

Table 3-8: eDP1 Video Signals (CN11)

Pin #	Signal	Description
1	NC	Not Connected
2	eDP1_BKLT_PWR	Backlight power (5V / 12V [selected at CN59])
3	eDP1_BKLT_PWR	Backlight power (5V / 12V [selected at CN59])
4	eDP1_BKLT_PWR	Backlight power (5V / 12V [selected at CN59])
5	eDP1_BKLT_PWR	Backlight power (5V / 12V [selected at CN59])
6	NC	Not Connected
7	NC	Not Connected
8	eDP1_BKLT_PWM	Backlight brightness via pulse width modulation (PWM)
9	eDP1_BKLT_ENABLE	Backlight power enable
10	eDP1_BKLT_GND	Backlight ground
11	eDP1_BKLT_GND	Backlight ground
12	eDP1_BKLT_GND	Backlight ground
13	eDP1_BKLT_GND	Backlight ground
14	eDP1_HPD	Hot Plug Detect
15	eDP1_LCD_GND	LCD ground
16	eDP1_LCD_GND	LCD ground
17	eDP1_LCD_GND	LCD ground
18	eDP1_LCD_GND	LCD ground
19	NC	Not Connected

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Table 3-8: eDP1 Video Signals (CN11) (Continued)

Pin #	Signal	Description
20	eDP1_LCD_VCC	LCD power (3.3V / 5V / 12V)
21	eDP1_LCD_VCC	LCD power (3.3V / 5V / 12V)
22	eDP1_LCD_VCC	LCD power (3.3V / 5V / 12V)
23	eDP1_LCD_VCC	LCD power (3.3V / 5V / 12V)
24	eDP1_HS_GND	High-Speed Ground
25	eDP1_AUX_n	Auxiliary differential pair - negative
26	eDP1_AUX_p	Auxiliary differential pair - positive
27	eDP1_HS_GND	High-Speed Ground
28	eDP1_TX0_p	Lane 0 Display Port primary channel differential pair 0 - positive
29	eDP1_TX0_n	Lane 0 Display Port primary channel differential pair 0 - negative
30	eDP1_HS_GND	High-Speed Ground
31	eDP1_TX1_p	Lane 1 Display Port primary channel differential pair 1 - positive
32	eDP1_TX1_n	Lane 1 Display Port primary channel differential pair 1 - negative
33	eDP1_HS_GND	High-Speed Ground
34	eDP1_TX2_p	Lane 2 Display Port primary channel differential pair 2 - positive
35	eDP1_TX2_n	Lane 2 Display Port primary channel differential pair 2 - negative
36	eDP1_HS_GND	High-Speed Ground
37	eDP1_TX3_p	Lane 3 Display Port primary channel differential pair 3 - positive
38	eDP1_TX3_n	Lane 3 Display Port primary channel differential pair 3 - negative
39	eD1_HS_GND	High-Speed Ground
40	NC	Not Connected

NOTE: The shaded table cells denote power or ground.

3.8 PS/2 Power Source Select (CN20)

Table 3-9 lists the pin signals of the PS/2 Power Source Select jumper header, which provides 3 pins in a single row with 0.079" (2.00mm) pitch.

Table 3-9: PS/2 Power Source Select (CN20)

Pin #	Signal	Jumper Position
1	+V5P0_SBY	• Jumper Installed 1-2 - 5V Standby voltage (**Default**) • Jumper Installed 2-3 - 5V A
2	+5V_PS2	
3	+V5_IN	

NOTE: The shaded table cells denote power.

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3.9 COM1 / COM2 (CN39)

This section describes the signals of the dual, standard DB9 serial port connector for RS232 signals. Table 3-10 and Table 3-11 list the pin signals of the 4-wire RS232 interface (COM1 and COM2), which provides a standard dual DB9 connector.

Table 3-10: COM1 Signals (CN39)

Pin #	Signal	Description
1	COM1_DCD#	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
2	COM1_RXD	Serial Input. This pin is used to transmit serial data out to the communication link.
3	COM1_TXD	UART A Serial Output. This pin is used to transmit serial data out to the communication link.
4	COM1_DTR#	UART A Data Terminal Ready. An Active-Low signal informs the modem or data set that the controller is ready to communicate.
5	COM1_GND	Ground
6	COM1_DSR#	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
7	COM1_RTS#	UART A Request to Send. An Active-Low signal informs the modem or data set that the controller is ready to send data.
8	COM1_CTS#	Clear to Send. This is the modem-control input. The function of this pin can be tested by reading bit 4 of the handshake status register.
9	COM1_RI#	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.

NOTE: Shaded table cell denotes ground. The # symbol indicates the signal is Active Low. This port supports only RS232.

Table 3-11: COM2 Signals (CN39)

Pin #	Signal	Description
1	COM2_DCD#	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
2	COM2_RXD	Serial Input. This pin is used to transmit serial data out to the communication link.
3	COM2_TXD	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
4	COM2_DTR#	UART B Data Terminal Ready. An Active-Low signal informs the modem or data set that the controller is ready to communicate.
5	COM2_GND	Ground
6	COM2_DSR#	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
7	COM2_RTS#	UART B Request to Send. An Active-Low signal informs the modem or data set that the controller is ready to send data.
8	COM2_CTS#	Clear to Send. This is the modem-control input. The function of this pin can be tested by reading bit 4 of the handshake status register.
9	COM2_RI#	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.

NOTE: Shaded table cell denotes ground. The # symbol indicates the signal is Active Low. This port supports only RS232.

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3.10 PCI Express x1 (CN42, CN44, CN45)

Table 3-12 lists the signals for the PCIe A x1 connector, which provides 36 pins, two rows, consecutive pin sequence (1, 13) with 1.00mm pitch.

Table 3-12: PCIe x1 (CN42, CN44, CN45)

Pin	Signal	Pin	Signal
B1	+V12P0_ATX	A1	PCIE_A_PRSNT1#
B2	+V12P0_ATX	A2	+V12P0_ATX
B3	+V12P0_ATX	A3	+V12P0_ATX
B4	GND	A4	GND
B5	SMB_CK	A5	Not Connected
B6	SMB_DAT	A6	Not Connected
B7	GND	A7	Not Connected
B8	+3VP3	A8	Not Connected
B9	Not Connected	A9	+3VP3S
B10	+3VP3A (auxiliary)	A10	+3VP3S
B11	PCIE_WAKE#	A11	PCIE_RST#
B12	Not Connected	A12	GND
B13	GND	A13	PCIE_CLK_P
B14	PCIE_TX_P	A14	PCIE_CLK_N
B15	PCIE_TX_N	A15	GND
B16	GND	A16	PCIE_RX_P
B17	PCIE_PRSNT2#	A17	PCIE_RX_N
B18	GND	A18	GND

NOTE: Shaded table cells denote power or ground. The # symbol indicates the signal is Active Low.

3.11 Digital Audio (CN46)

Table 3-13 lists the pin signals of the Digital Audio interface, which provides 4 pins, 2 rows, with odd/even pin sequence (1, 2) and 0.079" (2mm) pitch.

Table 3-13: Digital Audio Signals (CN46)

Pin #	Signal	Description
1	CON_SPDIFI	Digital Audio In
2	GND	Ground
3	CON_SPDIFO	Digital Audio Out
4	GND	Ground

NOTE: The shaded table cells denote ground.

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3.12 USB Signals

3.12.1 Standard USB Interfaces

All USB interfaces on Q7-BASE are supported through standard connectors, and their signal definitions can be found in their respective specification datasheets. Refer to the following block diagram for illustrations of the standard and optional USB interface mappings on the carrier.

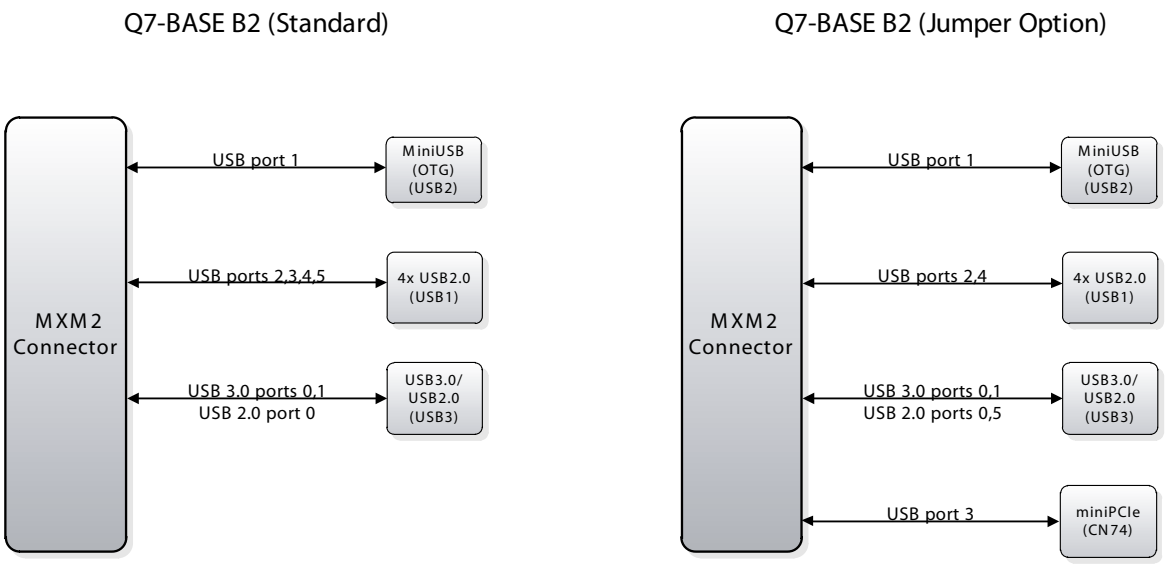


Figure 3-2: USB Mapping Block Diagram

The USB signals are routed from the module to the following connectors on the carrier: USB1 (Ports 2, 3, 4, 5 USB 2.0), USB2 (Port 1 [USB 2.0 OTG or client]), and USB3 (Ports 0, 6, 7 [USB 3.0 / USB 2.0]). The following subsections provide further details on the USB interfaces.

3.12.2 USB1

This 4-port stack provides USB 2.0 signals for ports 2, 3, 4, and 5 of the USB interface. As a jumper option, signals shared with port 5 from the Qseven module can be routed to this connector if they are not used by the USB3 connector.

3.12.3 USB2

This connector is used as a Mini USB 2.0 device connector. The signals are routed to USB port 1 on the Qseven connector.

3.12.4 USB3

This 2-port stack provides USB 3.0 signals (top connector) for ports 0 and 1 (SSRX0/SSTX0 and SSRX1/SSTX1) from the Qseven module and USB 2.0 signals (bottom connector) for ports 6 and 7 from the Qseven module. As a jumper option, USB 2.0 signals for port 5 are available on the bottom connector if they are not used by the USB1 connector.

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3.13 CAN (Controller Area Network - CN50)

Table 3-14 lists the pin signals of the Controller Area Network interface (CAN), which provides 10 pins in 2 rows, odd/even pin sequence (1, 2), and 2.54mm pitch.

Table 3-14: CAN Signals (CN50)

Pin #	Signal
1	Not Connected
2	CAN_GND
3	CAN_Low
4	CAN_High
5	CAN_GND
6	Not Connected
7	Not Connected
8	Not Connected
9	CAN_+5VP0 (Enabled by CN77)
10	CAN_PE (Protective Earth)

NOTE: These pins are connected over the CAN transceiver to the CAN0 pins (TX/RX) on the Qseven connector interface. Shaded table cells denote power or ground.

3.14 CAN Termination (CN51)

Table 3-15 lists the pin signals of the CAN termination jumper header, which provides 2 pins with 2.00mm pitch.

Table 3-15: CAN Termination (CN51)

Pin #	Signal
1	CAN_L_TERM
2	CAN_H

NOTE: Default setting is empty pins. Installing a jumper on this header activates 120R termination between CAN_L and CAN_H.

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3.15 CPLD Programming (CN52)

Table 3-16 lists the pin signals of the CPLD Programming header, which provides 10 pins, 2 rows, with odd/even sequence and 0.100" (2.54mm) pitch.

Table 3-16: CPLD Programming Signals (CN52)

Pin #	Signal
1	POST_TCK (Test Clock)
2	GND
3	POST_TDO (Test Data Output)
4	+V3P3_ATX
5	POST_TMS (Test Mode Select)
6	Not Connected
7	Not Connected
8	Not Connected
9	POST_TDI (Test Data Input)
10	GND

NOTE: The shaded table cells denote Power or Ground.

3.16 FAN Control (CN53)

Table 3-17 lists the pin signals of the CPU fan header, which provides 4 pins in a single row with 2.54mm pitch.

Table 3-17: FAN (CN53)

Pin #	Signal
1	GND
2	FAN_VCC (+V12P0_ATX or +V5P0A [selected by CN79])
3	FAN_TACH_IN (measures fan speed)
4	FAN_PWM_OUT (sets fan speed)

NOTE: Shaded table cells denote power or ground.

3.17 Battery Enable (CN57)

Table 3-18 lists the pin signals of the coin cell battery enable jumper header, which provides 2 pins with 2.00mm pitch.

Table 3-18: Battery Enable (CN57)

Pin #	Signal	Jumper Position
1	3V_BAT	• Jumper Installed (1-2) - coin cell battery socket enabled (**Default**) • Empty - coin cell battery socket disabled
2	+VDD_RTC	

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3.18 Backlight Voltage Select (CN59)

Table 3-19 lists the pin signals of the Backlight Voltage Select jumper header, which provides 3 pins, single-row, with 0.079" (2mm) pitch.

Table 3-19: Backlight Voltage Select Signals (CN59)

Pin #	Signal	Jumper Position
1	LCD_12V	• Jumper Installed 1-2 - 12 volts (**Default**) • Jumper Installed 2-3 - 5 volts
2	BKLT_PWR_SRC	
3	LCD_5V	

NOTE: The shaded table cells denote power.

3.19 Keyboard Controller Enable (CN61)

Table 3-20 lists the pin signals of the Enable Keyboard Controller jumper header, which provides 2 pins with 0.079" (2mm) pitch.

Table 3-20: Keyboard Controller Enable (CN61)

Pin #	Signal
1	+V3P3S
2	SIO_ADDR (open = 2Eh [**Default**]; closed = 4Eh)

NOTE: The shaded table cells denote Power. Default = jumper removed.

3.20 LCD Supply Voltage Select (CN62)

Table 3-21 lists the pin signals of the LCD Supply Voltage Select jumper header, which provides 6 pins, 2 rows, with odd/even pin sequence (1, 2) and 0.079" (2mm) pitch.

Table 3-21: LCD Supply Voltage Select (CN62)

Pin #	Signal	
1	LCD_3P3V	• Jumper Installed 1-2 - 3.3 volts (**Default**) • Jumper Installed 3-4 - 5 volts • Jumper Installed 5-6 - 12 volts
2	LCD_PWR_SRC	
3	LCD_5V	
4	LCD_PWR_SRC	
5	LCD_12V	
6	LCD_PWR_SRC	

NOTE: The shaded table cells denote Ground or Power. Default = jumper installed on 1-2.

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3.21 ATX PS_ON Selection (CN63)

Table 3-22 lists the pin signals of the ATX PS_ON Selection jumper header, which provides 6 pins, 2 rows, with odd/even pin sequence (1, 2) and 0.079" (2mm) pitch.

Table 3-22: ATX PS_ON Selection (CN63)

Pin #	Signal
1	+V5P0_SBY
2	GND
3	SUS_S3#
4	GND
5	SUS_S5#
6	GND

NOTE: The shaded table cells denote Ground or Power. Default = jumper installed on 5-6

3.22 USB0 Voltage Select (CN64)

Table 3-23 lists the pin signals of the USB0 Voltage Select jumper header, which provides 3 pins, single-row, with 0.079" (2mm) pitch.

Table 3-23: USB0 Voltage Select Signals (CN64)

Pin #	Signal
1	+V5P0_SBY
2	+VCC_USB02PWR
3	+V5_IN

NOTE: The shaded table cells denote Ground or Power. Default = jumper installed on 1-2.

3.23 LVDS Backlight (CN65)

Table 3-24 lists the pin signals of the LVDS Backlight interface, which provides 8 pins, 2 rows, with odd/even pin sequence (1, 2) and 0.100" (2.54mm) pitch.

Table 3-24: LVDS Backlight (CN65)

Pin #	Signal
1	GND
2	+VCC_LVDS (fixed voltage 5V or 12V selected at CN62)
3	LVDS_BKLT_CTRL
4	GND
5	LVDS_BKLT_EN_B
6	GND
7	Not Connected
8	+VCC_BKLT (switched backlight voltage, controlled by chipset and selected at CN59)

NOTE: The shaded table cells denote Ground or Power.

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3.24 LVDS Interface (CN66)

This section describes the LVDS interface available on the Q7-BASE LVDS version of the board. See Figure 3-3 for a display signal map of the Q7-BASE LVDS model.

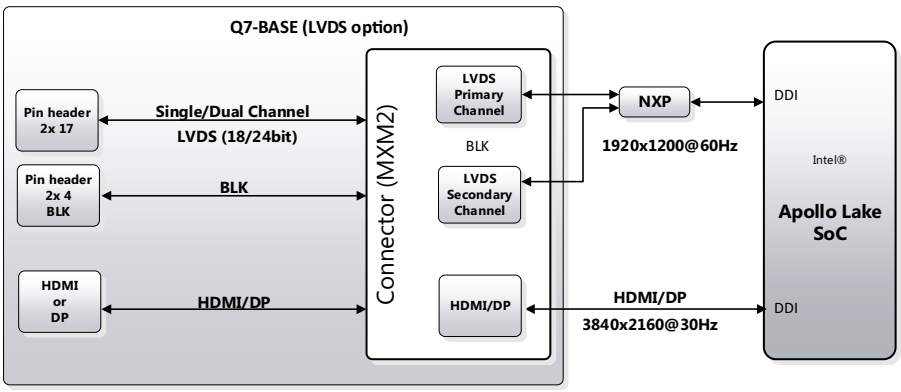


Figure 3-3: LVDS Mapping Block Diagram

Table 3-25 lists the pin signals of the LVDS Interface header, which provides 34 pins, 2 rows, with odd/even sequence (1, 2) and 0.079" (2mm) pitch.

Table 3-25: LVDS Interface Signals (CN66)

Pin #	Signal	Pin #	Signal
1	LVDS_CON_DC_DATA	2	LVDS_CON_DDC_CLK
3	+VCC_LVDS (switched LVDS voltage controlled by chipset and selected at CN62)	4	+VCC_LVDS
5	GND	6	LVDS_CON_A0_N
7	LVDS_CON_A0_P	8	LVDS_PWR_EN_NI
9	LVDS_CON_A1_N	10	LVDS_CON_A1_P
11	LVDS_BKLT_EN_NI	12	LVDS_CON_A2_P
13	LVDS_CON_A2_N	14	Not Connected
15	LVDS_CON_ACLK_N	16	LVDS_CON_ACLK_P
17	+VCC_LVDS	18	LVDS_CON_A3_P
19	LVDS_CON_A3_N	20	GND
21	LVDS_CON_B0_N	22	LVDS_CON_B0_P
23	GND	24	LVDS_CON_B1_N
25	LVDS_CON_B1_P	26	GND
27	LVDS_CON_B2_N	28	LVDS_CON_B2_P
29	GND	30	LVDS_CON_BKLT_P
31	LVDS_CON_BKLT_N	32	Not Connected
33	LVDS_CON_B3_P	34	LVDS_CON_B3_N

NOTE: The shaded table cells denote Ground or Power.

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3.25 SIO Enable (CN69)

Table 3-26 lists the pin signals of the SIO Enable jumper header, which provides 3 pins, single-row, with 0.079" (2mm) pitch. Select 1-2 to enable SIO, 2-3 to disable SIO.

Table 3-26: SIO Enable Signals (CN69)

Pin #	Signal
1	LPC_CLK
2	SIO_CLK
3	GND (SIO_OFF)

NOTE: The shaded table cells denote Ground. Default = jumper installed on 1-2.

3.26 UART Interface (CN70)

Table 3-27 lists the pin signals of the UART Interface header, which provides 10 pins, 2 rows, with odd/even sequence and 0.100" (2.54mm) pitch.

Table 3-27: UART Interface Signals (CN70)

Pin #	Signal
1	Not Connected
2	Not Connected
3	CON_UART_RX
4	CON_UART_RTS
5	CON_UART_TX
6	CON_UART_CTS
7	Not Connected
8	Not Connected
9	GND
10	+VCC_UART (+5 volts)

NOTE: The shaded table cells denote Power or Ground. This port supports only RS232.

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3.27 LPT Interface (CN71)

Table 3-28 lists the pin signals of the LPT Interface header, which provides 26 pins, 2 rows, with odd/even sequence (1, 2) and 0.100" (2.54mm) pitch.

Table 3-28: LPT Interface Signals (CN71)

Pin #	Signal	Pin #	Signal
1	LPT_STB#_R	2	LPT_AFD#_R
3	LPT_PD0_R	4	LPT_ERR#
5	LPT_PD1_R	6	LPT_INIT#_R
7	LPT_PD2_R	8	LPT_SLIN#_R
9	LPT_PD3_R	10	GND
11	LPT_PD4_R	12	GND
13	LPT_PD5_R	14	GND
15	LPT_PD6_R	16	GND
17	LPT_PD7_R	18	GND
19	LPT_ACK#	20	GND
21	LPT_BUSY	22	GND
23	LPT_PE	24	GND
25	LPT_SLCT	26	+VCC_LPT (+5 volts)

NOTE: The shaded table cells denote Ground or Power. The # symbol indicates the signal is Active Low.

3.28 System Interface (CN73)

Table 3-29 lists the pin signals of the System Interface header, which provides 20 pins, 2 rows, with odd/even sequence (1, 2) and 0.100" (2.54mm) pitch.

Table 3-29: System Interface Signals (CN73)

Pin #	Signal	Pin #	Signal
1	+V3P3_SYSCON	2	+V5P0_SYSCON
3	SMB_CLK	4	SPI_CLK
5	SMB_DATA	6	SPI_MISO
7	SMB_Q7_ALERT#	8	SPI_MOSI
9	SUS_STAT#	10	SPI_CS0#
11	GP1WIRE	12	SPI_CS1#
13	WD_TRIG#	14	THRM#
15	WD_OUT	16	THRMTRIP#
17	BIOS_DIS#	18	BATLOW#
19	GND	20	GND

NOTE: The shaded table cells denote Ground. The # symbol indicates the signal is Active Low.

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3.29 CAN 5-Volt Enable (CN77)

Table 3-30 lists the pin signals of the CAN 5-Volt Enable jumper header, which provides 2 pins with 0.079" (2mm) pitch. The jumper header enables an additional 5 volts and ground for the CAN header at CN50, pin 9.

Table 3-30: CAN 5-Volt Enable Signals (CN77)

Pin #	Signal
1	+V5P0_ATX
2	Pin 9 at CN50

NOTE: The shaded table cells denote Ground or Power. Default = open pins, no jumper installed.

3.30 LPC / TPM Interface (CN78)

Table 3-31 lists the pin signals of the LPC / TPM Interface socket, which provides 20 pins, 2 rows, with odd/even sequence (1, 2) and 0.100" (2.54mm) pitch.

Table 3-31: LPC / TPM Interface Signals (CN78)

Pin #	Signal	Pin #	Signal
1	LPC_CLK	2	GND
3	LPC_FRAME#	4	Removed
5	CB_RESET#	6	Not Connected
7	LPC_AD3	8	LPC_AD2
9	+V3P3_LPC_TPM	10	LPC_AD1
11	GP1WIRE	12	GND
13	Not Connected	14	Not Connected
15	+V3P3_SBY_LPC_TPM	16	LPC_SERIRQ
17	GND	18	Not Connected
19	LPC_PD#	20	Not Connected

NOTE: The shaded table cells denote Ground or Power. The # symbol indicates the signal is Active Low.

3.31 Fan Voltage Select (CN79)

Table 3-32 lists the pin signals of the Fan Voltage Select jumper header, which provides 3 pins, single-row, with 0.079" (2mm) pitch.

Table 3-32: Fan Voltage Select Signals (CN79)

Pin #	Signal
1	+V12P0_ATX
2	FAN_PWR_CN
3	+5V_IN

NOTE: The shaded table cells denote power or ground. Default = jumper installed on 2-3.

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3.32 USB1 Voltage Select (CN80)

Table 3-33 lists the pin signals of the USB1 Voltage Select jumper header, which provides 3 pins, single-row, with 0.079" (2mm) pitch.

Table 3-33: USB1 Voltage Select Signals (CN80)

Pin #	Signal
1	+V5P0_SBY
2	+VCC_USB2345PWR
3	+V5_IN

NOTE: The shaded table cells denote Ground or Power. Default = jumper installed on 1-2.

3.33 ATX_PWRGD Mode Select (CN81)

Table 3-34 lists the pin signals of the ATX_PWRGD Mode Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-34: ATX_PWRGD Mode Select (CN81)

Pin #	Signal	Jumper Position
1	+V5P0_SBY	• Jumper Installed 1-2 - BattMan mode • Jumper Installed 2-3 - ATX mode (**Default**)
2	ATX_PWRGD	
3	ATX_PWRGD_5V	

NOTE: For BattMan operation, this header requires a jumper installed on pins 1-2. The # symbol indicates the signal is Active Low.

3.34 DisplayPort (CN84)

Table 3-35 lists the pin signals of the embedded DisplayPort connector, which provides 40-pins, single row with 0.5mm pitch.

Table 3-35: DisplayPort Signals (CN84)

Pin #	Signal	Description
1	DP_D0_CON_P	Lane 0 DisplayPort primary channel differential pair 0 - positive
2	GND	Ground
3	DP_D0_CON_N	Lane 0 DisplayPort primary channel differential pair 0 - negative
4	DP_D1_CON_P	Lane 1 DisplayPort primary channel differential pair 1 - positive
5	GND	Ground
6	DP_D1_CON_N	Lane 1 DisplayPort primary channel differential pair 1 - negative
7	DP_D2_CON_P	Lane 2 DisplayPort primary channel differential pair 2 - positive
8	GND	Ground
9	DP_D2_CON_N	Lane 2 DisplayPort primary channel differential pair 2 - negative
10	DP_D3_CON_P	Lane 3 DisplayPort primary channel differential pair 3 - positive
11	GND	Ground
12	DP_D3_CON_N	Lane 3 DisplayPort primary channel differential pair 3 - negative
13	DP_CONFIG1_R	DisplayPort auxiliary
14	DP_CONFIG2_R	Connected to ground
15	DP_AUX_CON_P	DisplayPort auxiliary channel differential pair - positive
16	GND	Ground
17	DP_AUX_CON_N	DisplayPort auxiliary channel differential pair - negative
18	DP_CON_HDP	DisplayPort Hot Plug Detect
19	DP_RTN_PWR	DisplayPort Return Power

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Table 3-35: DisplayPort Signals (CN84) (Continued)

Pin #	Signal	Description
20	+3V3S_DP	DisplayPort Power

NOTE: The shaded table cells denote power or ground.

3.35 Display Mode Select (CN85)

Table 3-36 lists the pin signals of the Display Mode Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-36: Display Mode Select (CN85)

Pin #	Signal	Jumper Position
1	+V3PS	• Jumper Installed 1-2 - HDMI mode • Jumper Installed 2-3 - DisplayPort mode (**Default**)
2	DP/HDMI_SEL2	
3	GND	

3.36 I2S (CN86)

Table 3-37 lists the pin signals of the I2S header, which provides 10 pins in two rows with 2.54mm pitch.

Table 3-37: I2S Signals (CN86)

Pin #	Signal	Pin #	Signal
1	I2S_WS (Word Select from module Codec)	2	I2S_+V3P3S (3.3V for module Codec, 250mA max)
3	I2S_SDO (Data Output from module Codec)	4	I2S_+V1P8S (1.8V for module Codec, 250mA max)
5	I2S_SDI (Data Input from module Codec)	6	I2S_RST# (Reset module Codec)
7	I2S_CLK (Data Clock from module Codec)	8	GND (Ground for module Codec)
9	SMB_DATA	10	SMB_CLK

NOTE: Shaded table cells denote power or ground. The # symbol indicates the signal is Active Low.

3.37 HDA_SYNC / I2S_WS Select (CN87)

Table 3-38 lists the pin signals of the HDA_SYNC / I2S_WS Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-38: HDA_SYNC / I2S_WS Select (CN87)

Pin #	Signal	Jumper Position
1	I2S_WS	• Jumper Installed 1-2 - I2S • Jumper Installed 2-3 - HDA (**Default**)
2	HDA_SYNC/I2S_WS	
3	HDA_SYNC	

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3.38 HDA_RST# / I2S_RST# Select (CN88)

Table 3-39 lists the pin signals of the HDA_RST# / I2S_RST# Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-39: HDA_RST# / I2S_RST# Select (CN88)

Pin #	Signal	Jumper Position
1	I2S_RST#	• Jumper Installed 1-2 - I2S • Jumper Installed 2-3 - HDA (**Default**)
2	HDA_RST#/ I2S_RST#	
3	HDA_RST#	

NOTE: The # symbol indicates the signal is Active Low.

3.39 HDA_BITCLK / I2S_CLK Select (CN89)

Table 3-40 lists the pin signals of the HDA_BITCLK / I2S_CLK Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-40: HDA_BITCLK / I2S_CLK Select (CN89)

Pin #	Signal	Jumper Position
1	I2S_CLK	• Jumper Installed 1-2 - I2S • Jumper Installed 2-3 - HDA (**Default**)
2	HDA_BITCLK/ I2S_CLK	
3	HDA_BITCLK	

3.40 HDA_SDO / I2S_SDO Select (CN90)

Table 3-41 lists the pin signals of the HDA_SDO / I2S_SDO Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-41: HDA_SDO / I2S_SDO Select (CN90)

Pin #	Signal	Jumper Position
1	I2S_SDO	• Jumper Installed 1-2 - I2S • Jumper Installed 2-3 - HDA (**Default**)
2	HDA_SDO/I2S_SDO	
3	HDA_SDO	

3.41 HDA_SDI / I2S_SDI Select (CN91)

Table 3-42 lists the pin signals of the HDA_SDI / I2S_SDI Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-42: HDA_SDI / I2S_SDI Select (CN91)

Pin #	Signal	Jumper Position
1	I2S_SDI	• Jumper Installed 1-2 - I2S • Jumper Installed 2-3 - HDA (**Default**)
2	HDA_SDI/I2S_SDI	
3	HDA_SDI	

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3.42 EN_V3P3S Select (CN92)

Table 3-43 lists the pin signals of the EN_V3P3S Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-43: EN_V3P3S Select (CN92)

Pin #	Signal	Jumper Position
1	+V5_IN	• Jumper Installed 1-2 - ATX mode • Jumper Installed 2-3 - SUS_S3# (**Default**)
2	EN_V3P3S	
3	SUS_S3#	

3.43 USB3_CN_p / USB3_mPCIe_p Select (CN93)

Table 3-44 lists the pin signals of the USB3_CN_p / USB3_mPCIe_p Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-44: USB3_CN_p / USB3_mPCIe_p Select (CN93)

Pin #	Signal	Jumper Position
1	USB3_CN_p	• Jumper Installed 1-2 - USB connector (**Default**) • Jumper Installed 2-3 - MiniPCIe
2	USB3_L_p	
3	USB3_mPCIe_p	

3.44 USB3_CN_n / USB3_mPCIe_n Select (CN94)

Table 3-45 lists the pin signals of the USB3_CN_n / USB3_mPCIe_n Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-45: USB3_CN_n / USB3_mPCIe_p Select (CN94)

Pin #	Signal	Jumper Position
1	USB3_CN_n	• Jumper Installed 1-2 - USB connector (**Default**) • Jumper Installed 2-3 - MiniPCIe
2	USB3_L_n	
3	USB3_mPCIe_n	

3.45 USB OTG Power Control (CN95)

Table 3-46 lists the pin signals of the USB OTG Power Control jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-46: USB OTG Power Control (CN95)

Pin #	Signal	Jumper Position
1	USB_DRIVE_VBUS	• Jumper Installed 1-2 - USB_DRIVE_VBUS (**Default**) • Jumper Installed 2-3 - USB_OTG_ID
2	USB02_PWREN	
3	USB1_OTG_ID_INV	

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3.46 USB_VBUS Source Select (CN96)

Table 3-47 lists the pin signals of the USB_VBUS Source Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-47: USB_VBUS Source Select (CN96)

Pin #	Signal	Jumper Position
1	USB_VBUS_SRC	• Jumper Installed 1-2 - USB_VBUS (**Default**) • Jumper Installed 2-3 - USB_CC
2	USB_VBUS	
3	USB_CC (Client Connect)	

3.47 PWM Backlight Voltage Select (CN97)

Table 3-48 lists the pin signals of the PWM Backlight Voltage Select jumper header, which provides 3 pins in a single row with 2.00mm pitch.

Table 3-48: PWM Backlight Voltage Select (CN97)

Pin #	Signal	Jumper Position
1	+V3P3S	• Jumper Installed 1-2 - 3.3V (**Default**) • Jumper Installed 2-3 - 5V
2	LVDS_BKLT_CTRL_GP_PWM_OUT	
3	+V5_IN	

3.48 eDP1 Backlight Control (CN98)

Table 3-49 lists the pin signals of the eDP1 Backlight Control jumper header, which provides 2 pins in a single row with 2.00mm pitch.

Table 3-49: eDP1 Backlight Control (CN98)

Pin #	Signal	Jumper Position
1	LVDS_BKLT_CNTRL_GP_PWM_OUT_B	• Jumper Installed - eDP1 Backlight Control • Jumper Removed - LVDS Backlight Control (**Default**)
2	eDP1_BKLT_CNTRL	

3.49 eDP1 Backlight Enable (CN99)

Table 3-50 lists the pin signals of the eDP1 Backlight Enable jumper header, which provides 2 pins in a single row with 2.00mm pitch.

Table 3-50: eDP1 Backlight Enable (CN99)

Pin #	Signal	Jumper Position
1	LVDS_BLEN	• Jumper Installed - eDP1 Backlight Enable • Jumper Removed - LVDS Backlight Enable (**Default**)
2	eDP1_BKLT_EN	

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3.50 I2C EEPROM Address Select Switch (SW6)

Table 3-51 lists the pin signals of the I2C EEPROM address select dip switch, which provides 4 poles, 8 positions with 1.27mm pitch.

Table 3-51: I2C EEPROM Address Select Switch (SW6)

Pin #	Signal	Pin#	Signal
1 (off)	I2C_A0 [**Default**]	8 (on)	+VCC_I2C
2 (off)	I2C_A1 [**Default**]	7 (on)	+VCC_I2C
3 (off)	I2C_A2 [**Default**]	6 (on)	+VCC_I2C
4 (off)	I2C_WP#	5 (on)	+VCC_I2C [**Default**]

NOTE: ON=high, OFF=low

3.51 SPI EEPROM Select Interface Switch (SW9)

Table 3-52 lists the pin signals of the SPI EEPROM control dip switch, which provides 4 poles, 8 positions with 1.27mm pitch.

Table 3-52: SPI EEPROM Control Switch (SW9)

Pin #	Signal	Pin#	Signal
1 (off)	SPI_CS#	8 (on)	GND [**Default**]
2 (off)	SPI_CS# [**Default**]	7 (on)	GND
3 (off)	SPI_WP#	6 (on)	GND [**Default**]
4 (off)	SPI_HOLD#	5 (on)	+VCC_SPI [**Default**]

NOTE: SPI_CS0: 1-8=ON, 2-7=OFF, 3-6=ON, 4-5=ON [**Default**]

SPI_CS1: 1-8=OFF, 2-7=ON, 3-6=ON, 4-5=ON

The # symbol indicates the signal is Active Low.

3.52 DP Control Switch (SW11)

Table 3-53 lists the pin signals of the DP Control dip switch, which provides 4 poles, 8 positions with 1.27mm pitch.

Table 3-53: DP Control Switch (SW11)

Pin #	Signal	Pin#	Signal
1 (off)	DP_CNTRL [**Default**]	8 (on)	+V3P3S
2 (off)	DP_CNTRL [**Default**]	7 (on)	GND
3 (off)	DP_EQ [**Default**]	6 (on)	+V3P3S
4 (off)	DP_EQ [**Default**]	5 (on)	GND

NOTE: Setup for normal mode - 1=OFF, 2=ON, 3=OFF, 4=ON; Refer to the PI3EQXDP1201 DisplayPort Redriver datasheet for more details.

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3.53 DP Enable Switch (SW12)

Table 3-54 lists the pin signals of the DP Enable dip switch, which provides 4 poles, 8 positions with 1.27mm pitch.

Table 3-54: DP Enable Switch (SW12)

Pin #	Signal	Pin#	Signal
1 (off)	DP_ENABLE [**Default**]	8 (on)	GND
2 (off)	DP_AUTOEQ [**Default**]	7 (on)	GND
3 (off)	DP_OC_0 [**Default**]	6 (on)	GND
4 (off)	DP_OC_1 [**Default**]	5 (on)	GND

NOTE: Setup for normal mode - 1=OFF, 2=OFF, 3=ON, 4=ON; Refer to the PI3EQXDP1201 Display Port Redriver datasheet for more details.

3.54 eDP0 Enable Switch (SW14)

Table 3-55 lists the pin signals of the eDP0 Enable dip switch, which provides 4 poles, 8 positions with 1.27mm pitch.

Table 3-55: eDP0 Enable Switch (SW14)

Pin #	Signal	Pin#	Signal
1 (off)	eDP0_ENABLE [**Default**]	8 (on)	GND
2 (off)	eDP0_AUTOEQ [**Default**]	7 (on)	GND
3 (off)	eDP0_OC_0 [**Default**]	6 (on)	GND
4 (off)	eDP0_OC_1 [**Default**]	5 (on)	GND

NOTE: Setup for normal mode - 1=OFF, 2=OFF, 3=ON, 4=ON; Refer to the PI3EQXDP1201 DisplayPort Redriver datasheet for more details.

3.55 eDP0 Operation Switch (SW15)

Table 3-56 lists the pin signals of the eDP0 Operation dip switch, which provides 4 poles, 8 positions with 1.27mm pitch.

Table 3-56: eDP0 Operation Switch (SW15)

Pin #	Signal	Pin#	Signal
1 (off)	eDP0_OP_0 [**Default**]	8 (on)	GND
2 (off)	eDP0_OP_1 [**Default**]	7 (on)	GND
3 (off)	Not Connected [**Default**]	6 (on)	Not Connected
4 (off)	Not Connected [**Default**]	5 (on)	Not Connected

NOTE: Setup for normal mode - 1=ON, 2=ON, 3=OFF, 4=OFF; Refer to the PI3EQXDP1201 DisplayPort Redriver datasheet for more details.

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3.56 eDP0 Control Switch (SW16)

Table 3-57 lists the pin signals of the eDP0 Control dip switch, which provides 4 poles, 8 positions with 1.27mm pitch.

Table 3-57: eDP0 Control Switch (SW16)

Pin #	Signal	Pin#	Signal
1 (off)	eDP0_CNTRL [**Default**]	8 (on)	+V3P3S
2 (off)	eDP0_CNTRL [**Default**]	7 (on)	GND
3 (off)	eDP0_EQ [**Default**]	6 (on)	+V3P3S
4 (off)	eDP0_EQ [**Default**]	5 (on)	GND

NOTE: Setup for normal mode - 1=OFF, 2=ON, 3=OFF, 4=ON; Refer to the PI3EQXDP1201 DisplayPort Redriver datasheet for more details.

3.57 eDP1 Enable Switch (SW17)

Table 3-58 lists the pin signals of the eDP1 Enable dip switch, which provides 4 poles, 8 positions with 1.27mm pitch.

Table 3-58: eDP1 Enable Switch (SW17)

Pin #	Signal	Pin#	Signal
1 (off)	eDP1_ENABLE [**Default**]	8 (on)	GND
2 (off)	eDP1_AUTOEQ [**Default**]	7 (on)	GND
3 (off)	eDP1_OC_0 [**Default**]	6 (on)	GND
4 (off)	eDP1_OC_1 [**Default**]	5 (on)	GND

NOTE: Setup for normal mode - 1=OFF, 2=OFF, 3=ON, 4=ON; Refer to the PI3EQXDP1201 DisplayPort Redriver datasheet for more details.

3.58 eDP1 Operation Switch (SW18)

Table 3-59 lists the pin signals of the eDP1 Operation dip switch, which provides 4 poles, 8 positions with 1.27mm pitch.

Table 3-59: eDP1 Operation Switch (SW18)

Pin #	Signal	Pin#	Signal
1 (off)	eDP1_OP_0 [**Default**]	8 (on)	GND
2 (off)	eDP1_OP_1 [**Default**]	7 (on)	GND
3 (off)	Not Connected [**Default**]	6 (on)	Not Connected
4 (off)	Not Connected [**Default**]	5 (on)	Not Connected

NOTE: Setup for normal mode - 1=ON, 2=ON, 3=OFF, 4=OFF; Refer to the PI3EQXDP1201 DisplayPort Redriver datasheet for more details.

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3.59 eDP1 Control Switch (SW19)

Table 3-60 lists the pin signals of the eDP1 Control dip switch, which provides 4 poles, 8 positions with 1.27mm pitch.

Table 3-60: eDP1 Control Switch (SW19)

Pin #	Signal	Pin#	Signal
1 (off)	eDP1_CNTRL [**Default**]	8 (on)	+V3P3S
2 (off)	eDP1_CNTRL [**Default**]	7 (on)	GND
3 (off)	eDP1_EQ [**Default**]	6 (on)	+V3P3S
4 (off)	eDP1_EQ [**Default**]	5 (on)	GND

NOTE: Setup for normal mode - 1=OFF, 2=ON, 3=OFF, 4=ON; Refer to the PI3EQXDP1201 DisplayPort Redriver datasheet for more details.

3.60 I2C EEPROM Address Interface Select Switch (SW20)

Table 3-61 lists the pin signals of the I2C EEPROM Interface select dip switch, which provides 4 poles, 8 positions with 1.27mm pitch.

Table 3-61: I2C EEPROM Address Interface Select Switch (SW20)

Pin #	Signal	Pin#	Signal
1 (off)	I2C_CLK	8 (on)	+VCC_I2C [**Default**]
2 (off)	I2C_DATA	7 (on)	+VCC_I2C [**Default**]
3 (off)	LVDS_DID_CLK [**Default**]	6 (on)	+VCC_I2C
4 (off)	LVDS_DID_DATA [**Default**]	5 (on)	+VCC_I2C

NOTE: GPIO_I2C: 1-8=ON, 2-7=ON, 3-6=OFF, 4-5=OFF [**Default**]

LVDS_I2C: 1-8=OFF, 2-7=OFF, 3-6=ON, 4-5=ON

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Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in Table A-1 below. Requests for support through Ask an Expert are given the highest priorities, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the ADLINK web site at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called “My ADLINK”, unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the My Question area where you can check status, update your request, and access other features.
- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1: Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	**ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110 San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

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Table A-1: Technical Support Contact Information (Continued)

Method	Contact Information
	LiPPERT ADLINK Technology GmbH Address: Hans-Thoma-Strasse 11 D-68163 Mannheim, Germany Tel: +49-621-43214-0 Fax: +49-621 43214-30 Email: emea@adlinktech.com Please visit Contact page at www.adlinktech.com for information on how to contact the ADLINK regional office nearest you.

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