Q7-BT

Technical Reference

Qseven Computer On Module with
Intel® Atom™ E3800 Series Processors



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Leading **EDGE COMPUTING**

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Preface

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Revision History

Revision	Date	Description of Change(s)
1.00	9/21/2015	Initial Release
2.00	8/8/2016	Added changes for A3 board revision
2.1	6/18/2018	Updated pin 3 of SW4 in Table 2-2 from “Not Connected” to “Selecting BIOS”; added note to pin 3 of SW4 to indicate BIOS_DISABLE# must be pulled low; added Figure 1-1 to Chapter 1; added Battery and Prop 65 warnings to Preface

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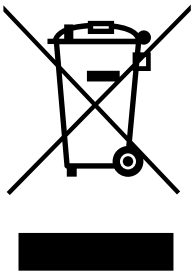
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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

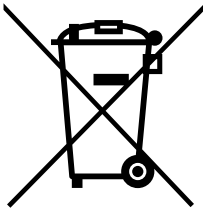
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Battery Labels (for products with battery)









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Conventions

The following conventions may be used throughout this manual, denoting special levels of information.



This information adds clarity or specifics to text and illustrations.



This information indicates the possibility of ***minor*** physical injury, component damage, data loss, and/or program corruption.



This information warns of possible ***serious*** physical injury, component damage, data loss, and/or program corruption.

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Important Safety Instructions

For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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1 Product Overview

1.1 Description

The Q7-BT Computer-On-Module (COM) combines the Qseven® 2.0 standard with the Intel® Atom™ E3800 series System-on-Chip (SoC), providing an ideal solution for mid-range power and high, pin/area density requirements. The module provides the high integration, high performance, low power, and ruggedness favored by Internet-of-Things (IoT) applications such as retail transactional clients, digital signage, and in-vehicle infotainment systems.

The Qseven form factor affords a more compact profile and footprint than the other COM platforms. With mechanical dimensions as small as 70mm width, 70mm length, and 2.3mm of overall height, Qseven ranks as the smallest COM standard currently available.

The Q7-BT module utilizes the E3800 SoC for contemporary, high-bandwidth interfaces such as PCI Express, USB, Gigabit Ethernet, SATA, and HD Audio. The module generates its own LVDS, TMDS, and DisplayPort video signals using DDI output from the SoC.

A series of optional eMMC devices offers up to 64GB of on-board NAND Flash storage with an MMC interface, and an optional SATA, Solid State Drive (SSD) provides up to 64GB of on-board NAND Flash storage. Two SPI Flash chips implement a fail-safe BIOS, allowing the user to boot the module even if current BIOS settings have corrupted the system.

Under the management of the BMC chip (Board Management Controller), the SEMA utility (Smart Embedded Management Agent) provides system control, security, and failure protection—counting, monitoring, and measuring hardware and software events, and using the SMBus to send corrective commands to the SoC. The optional SEMA Cloud utility not only controls local events on the module but system client events on the IoT.

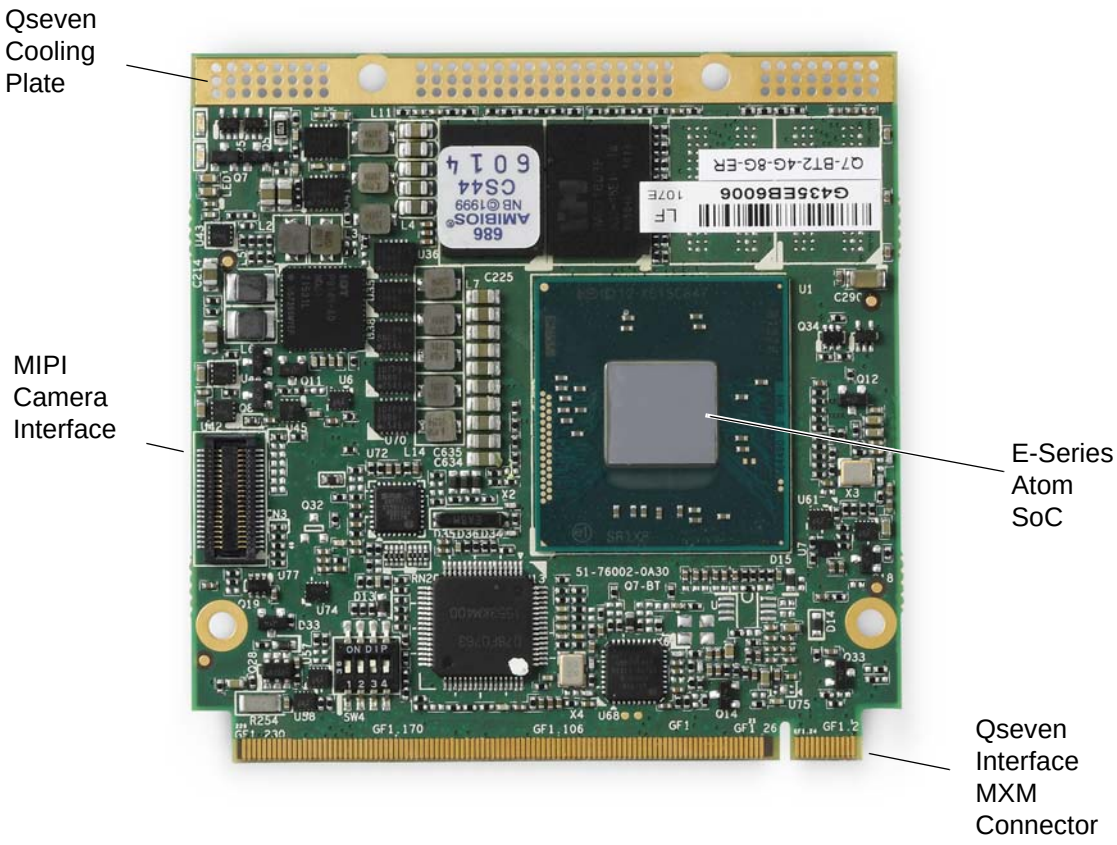


Figure 1-1: Overview of Q7-BT with Intel E-Series SoC

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1.2 Features

- CPU
  Intel® Atom™ E3800 Series, single, dual, or quad-core SoC (System-on-Chip) with integrated memory, graphics, and I/O. See the E3800 data sheet at the Intel website.
  - E3845 10W TDP, 1.91GHz Quad-Core/1333 MT/s with Gfx 542/792 MHz, Turbo
  - E3826 7W TDP, 1.46GHz Dual-Core/1066 MT/s with Gfx 533/667 MHz, Turbo
  - E3825 6W TDP, 1.33GHz Dual-Core/1066 MT/s with GFx 533/533 MHz, Turbo
  - E3815 5W TDP, 1.46GHz Single-Core/1066 MT/s with Gfx 400MHz, Non-Turbo
  - E3805 3W TDP, 1.33GHz Dual-Core/1066 MT/s without GFx
- Memory
  - Up to 4GB non-ECC, unbuffered soldered, DDR3L
  - 1066/1333MHz
  - Single channel
- Expansion
  - QSeven, board-to-board, Rev 2.0
- SATA
  - Two 3Gb/s, Gen 2 ports
  - Advanced Host Controller Interface (AHCI)
- USB
  - Six USB 2.0 ports (one as device port)
  - One USB 3.0 port
- Ethernet
  - Single-port, gigabit Ethernet controller
  - Integrated GbE MAC, PHY, and SGMII/SerDes ports
  - 10T/100TX/1000T signals using the PCIe x1 bus
- Serial UART
  - One high-speed, 4-wire port
  - Base frequency 50MHz
- I2C
  - One I2C bus
  - One SMBus
- SPI
  - Two internal SPI controllers
  - Two SPI flash devices for BIOS storage
- Video
  - Display Port/HDMI
  - LVDS
- Audio
  - One HDA (High Definition Audio) interface
- CSI/MIPI Camera
  - One front-end interface for 3 sensors
  - Capacity for acquiring 1 stream simultaneously from each sensor
- Storage
  - One optional eMMC NAND
  - One optional SATA SSD

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1.3 Block Diagram

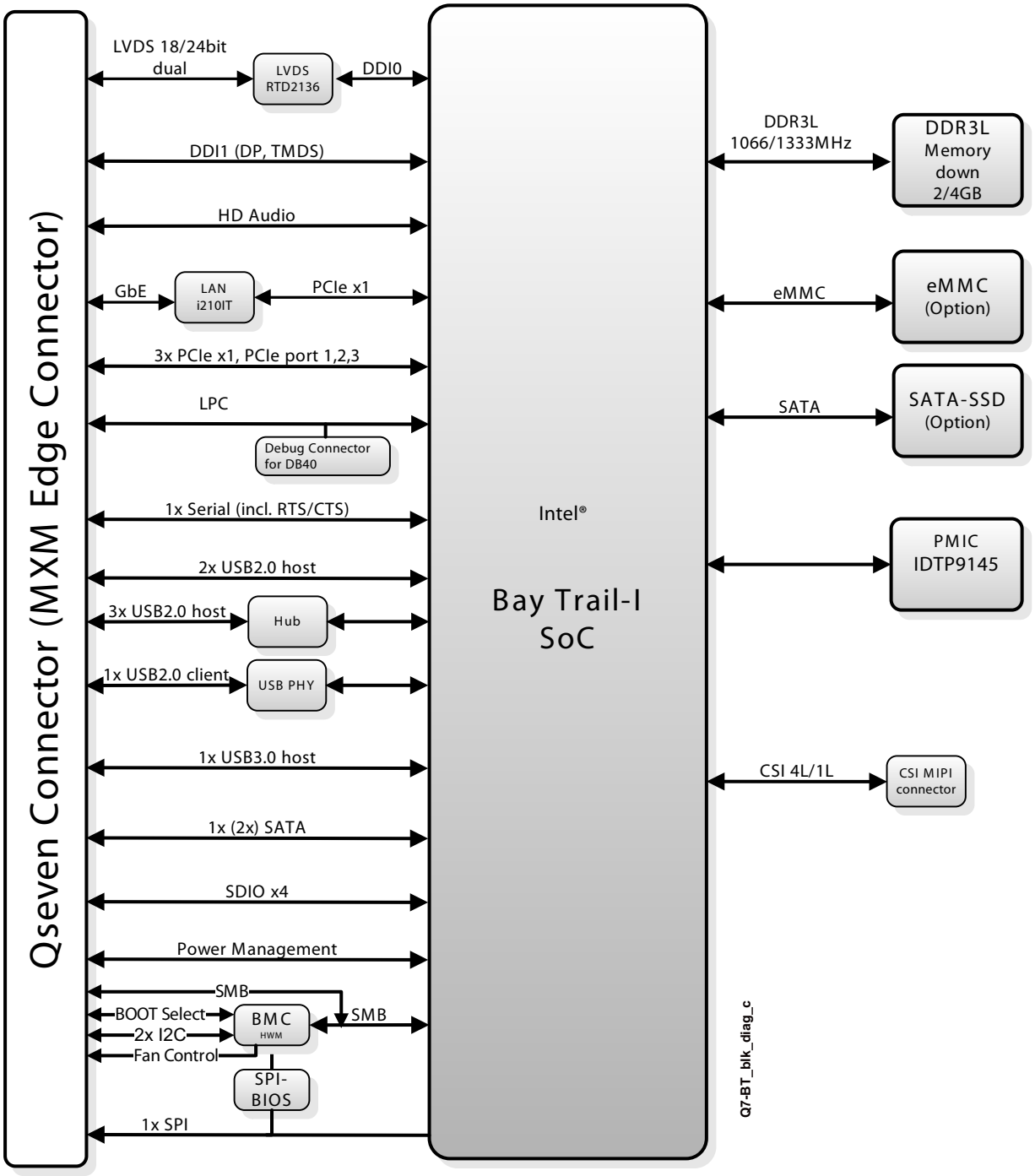


Figure 1-2: Module functional block diagram

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1.4 Specifications

1.4.1 Physical

Table 1-1 lists the physical dimensions of the module.

Table 1-1: Weight and Footprint Dimensions

Dimension	Measurement	
Weight	0.025 kg [0.09 kg with heat spreader]	Overall height is measured from the upper board surface to the top of the highest permanent component on the upper board surface. This measurement does not include the cooling solution.
Height (overall)	2.29mm	
Board thickness	1.27mm	
Width	70.00mm	
Length	70.00mm	

1.4.2 Electrical

Table 1-2 specifies the electrical characteristics of the module.

Table 1-2: Electrical Specifications

Parameter	Value
Voltage Input	
Standard	▶ +5 V DC, +/-5%, =/- mV ripple
Standby	▶ +5 V standby +/-5%, =/- mV ripple (only needed for suspend mode)
RTC	▶ 3.0V, 2.0V to 3.3V (battery), +/-20mV ripple
Power States	▶ C1-C6, S0, S1, S4, S3, S5, S5 ECO mode (wake on USB S3/S4, WOL S3/S4/S5)

1.4.3 Environmental

Table 1-3 defines the environmental conditions under which the module is qualified to operate and to be stored.

Table 1-3: Temperature, Humidity, and Pressure

Parameter	Temperature
Temperature	
Standard	▶ 0°C to +60°C
Extended	▶ -40°C to 85°C
Storage	▶ -55°C to 85°C
Humidity	
Operating	▶ 5% to 90% relative humidity, non-condensing
Non-operating	▶ 5% to 95% relative humidity, non-condensing

Table 1-4 presents the average times between system failures.

Table 1-4: Mean Time Between Failures

Parameter	Value
MTBF at 40°C	278,930 hrs (according to MIL calculation)
MTBF at 85°C	70,119 hrs (according to MIL calculation)

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1.4.4 Mechanical

Figure 1-3 provides the mechanical dimensions of the Q7-BT.

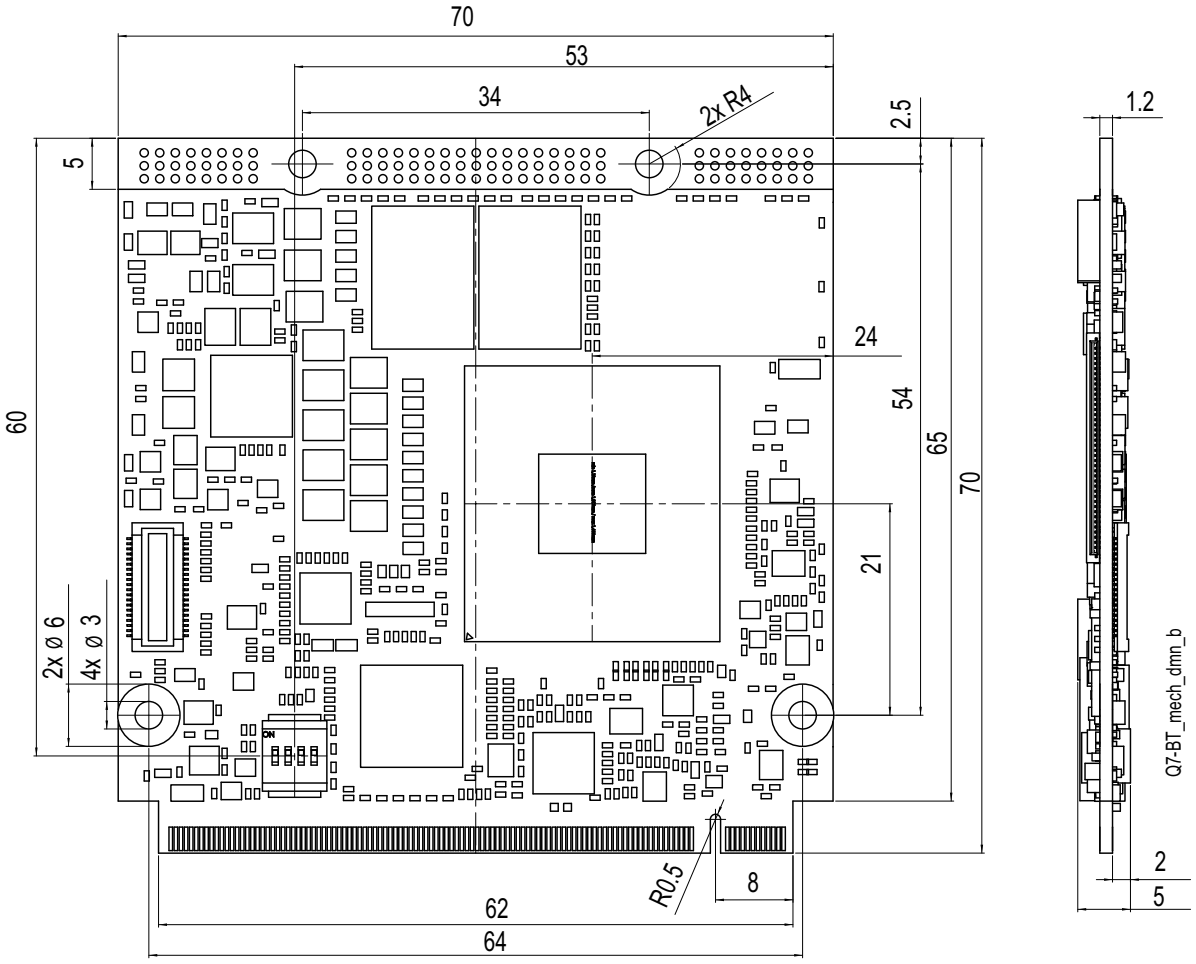


Figure 1-3: Mechanical dimensions (top side)

NOTE:

ADLINK strongly recommends plastic spacers instead of metal spacers for mounting the board. Metal spacers create the possibilities of short circuits with the components located around the mounting holes, which can ruin the board.

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1.4.5 Power

Table 1-5 provides the power requirements for this module under certain load configurations.

Table 1-5: Power Supply Requirements

Parameter	10W, E3845 SoC Characteristics	7W, E3826 SoC Characteristics	5W, E3815 SoC Characteristics
Input Type	Regulated DC voltage	Regulated DC voltage	Regulated DC voltage
In-rush Peak Current and Duration	5V / 1.75A (8.75W)	5V / 1.60A (8.00W)	5V / 1.05A (5.25W)
Typical Idle Current and Power	5V / 0.86A (4.30W)	5V / 0.79A (3.95W)	5V / 0.62A (3.10W)
BIT Current and Power	5V / 2.71A (13.55W)	5V / 1.70A (8.95W)	5V / 1.20A (6.00W)

Operating configurations:

- In-rush operating configuration - Windows 8.1
- Idle operating configuration - Windows 8.1
- BIT (Burn-In Test) operating configuration - Windows 8.1; Intel TAT tool

1.4.6 Cooling

The Q7-BT is designed to operate at its maximum CPU speeds of 1.46GHz and 1.91GHz and requires a thermal solution to cool the SoC. ADLINK offers a heat spreader as one part of the cooling solution. Refer to Figure 1-5 for diagram of heat spreader dimensions.

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The Q7-BT supports two separate heat spreaders—one for board revision A2 and one for board revision A3. The two versions of the heat spreader require different order numbers, respectively.

The heat spreader plate requires another form of cooling, such as a heatsink with a fan. A heat spreader plate is not a complete thermal solution for the Q7-BT.

The overall system design must keep the ICs within their operating temperature specifications.

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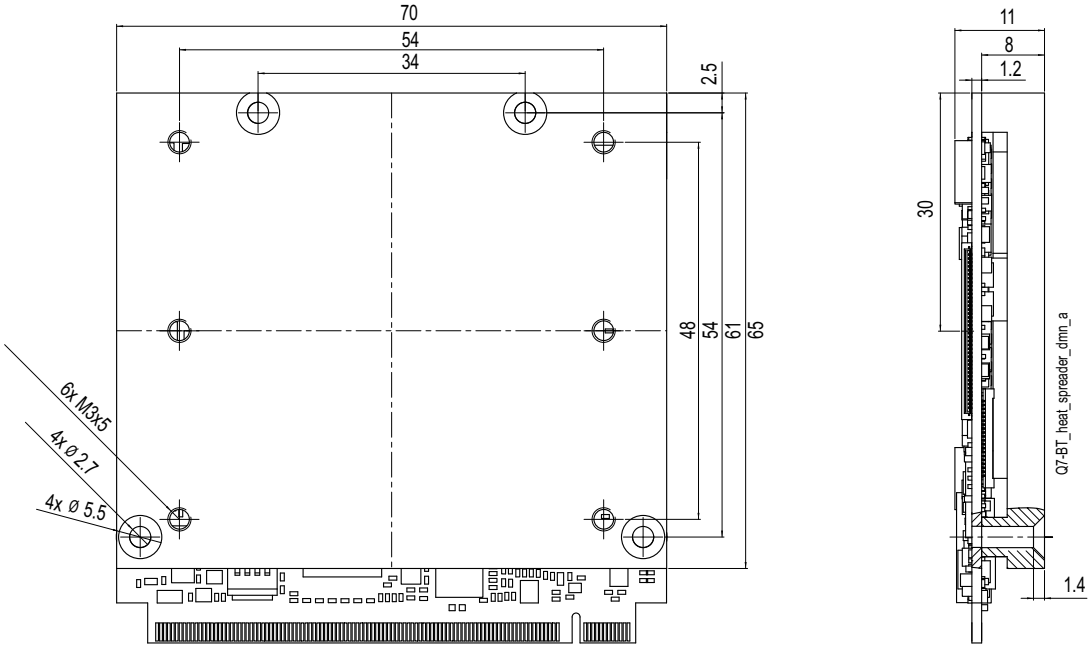


Figure 1-4: Heat Spreader mounting dimensions (top side)

1.5 Getting Started

Mount the Q7-BT to the carrier as illustrated in Figure 1-5, which provides a profile view of the module mounted to the carrier with dimensions.

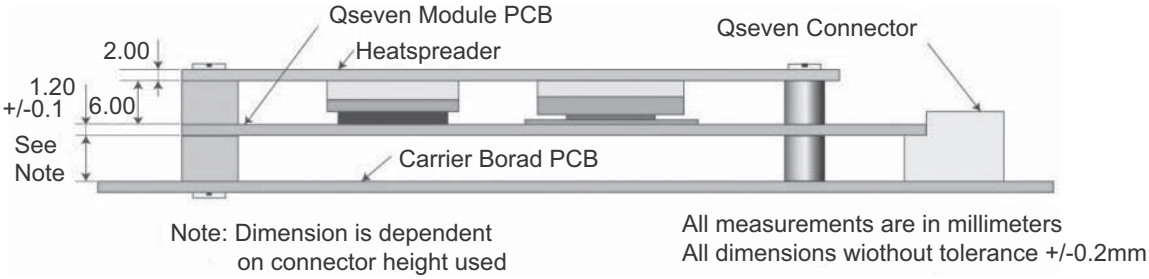


Figure 1-5: Qseven module mounting dimensions (profile)

NOTE:

ADLINK strongly recommends plastic spacers instead of metal spacers for mounting the board. Metal spacers create the possibilities of short circuits with the components located around the mounting holes, which can ruin the board

CAUTION:

Be sure to observe the EMC security measures. Make sure you are always at the same potential as the module.

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CAUTION:

Never connect or disconnect peripherals like HDDs while the power supply is connected and switched on.

Use a commercial, high-quality display cable to connect an HDMI display. Connect a USB keyboard or mouse to the carrier. Use the SATA cable to connect the hard disk. Make sure that the pins match their counterparts correctly and are not twisted. If you plan to use additional peripherals, connect them to the appropriate headers or connectors on the carrier.

Connect a power supply to the power connector on the carrier and switch on the power.


NOTE:

Observe the minimum voltage values for the standard peripherals mentioned. For additional peripherals, make sure enough power is available. The system will not work if there is not enough supply current for all your devices.

The display shows the BIOS messages. If you want to change the standard BIOS settings, press the <DEL> key to enter the BIOS setup menus. See Chapter 4 for setup details.

If you need to load the BIOS default values, they can be automatically loaded at boot time.

The Q7-BT boots from CD drives, USB sticks, hard disks, or µSD-Cards. Provided that any of these is connected and contains a valid operating system image, the display then shows the boot screen of your operating system.

The Q7-BT needs adequate cooling measures depending on the desired operating temperature range. Using the board without cooling could damage the board permanently.

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2 Hardware

This chapter describes the major integrated circuits (ICs) and interface connectors and headers on the module. The third section of this chapter further describes the major ICs on the board including a table of the SMBus slave device addresses on the board.

2.1 Major Components (ICs)

Table 2-1 lists the major integrated circuits on the Q7-BT, including a brief description of each IC. Figure 2-1 and Figure 2-2 show the locations of the major ICs.

Table 2-1:Major Integrated Circuit Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	Intel	E3805 (dual core, 3W, headless, 1.33GHz) E3815 (single core, 5W, 1.46GHz) E3825 (dual core, 6W, 1.33GHz) E3826 (dual core, 7W, 1.46GHz) E3845 (quad core, 10W, 1.91GHz)	Atom, 22nm SoC (System on Chip) with Intel 64 architecture	Integrates Processor Core, Graphics and Memory Hub, and I/O Hub
Gb Ethernet Controller (U9 on bottom side; see Figure 2-2)	Intel	WGI210IT SLIXT	Single-port Gigabit Ethernet controller	Integrates GbE MAC, PHY, and SGMII/SerDes to enable 10T/ 100TX/1000T Ethernet signals using the PCIe x1 bus
BMC [Board Management Controller] (U13)	Renesas	UDP78F0763GB-GAH-AX	Micro controller for board functions including Watchdog Timer and system control and failure protection	Controls dual BIOS and SEMA API through the I^2C bus
SPI Flash (U19 and U20 on bottom side; see Figure 2-2)	Winbond	W25Q64FVSSIG TR	Serial Peripheral Interface Flash Memory chip (for firmware)	Stores BIOS 0 and BIOS 1 in Flash Memory

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Table 2-1:Major Integrated Circuit Descriptions and Functions (Continued)

Chip Type	Mfg.	Model	Description	Function
DDR3L SDRAM (U24, U25, U26, U27 [U24 and U27 on bottom side; see Figure 2-2])	Micron	• MT41K128M16 (1GB board configuration) • MT41K256M16 (2GB board configuration)	On-board DDR3L, 1.35V, 4Gb, 32Mx16x8, non-ECC System Memory • 4Gb, 4x 128Mx16 • 4Gb, 4x 256Mx16	Provides high-speed data transfer
	I'M Intelligent	• IM8G16D3FBBG-15EI (4GB board configuration)	On-board DDR3L, 1.35V, 8Gb, 64Mx16x8, non-ECC System Memory • 8Gb, 4x 512Mx16	
eMMC, NAND Flash (U48 on bottom side; see Figure 2-2)	Micron	MTFC8GLVEA-4M-IT	MultiMediaCard Controller and NAND Flash Memory up to 64GB	Provides communication and mass data storage capabilities
SATA NAND SSD (U73 on bottom side; see Figure 2-2) [**Optional**]	Greenliant	GLS85LS1008B	Industrial-grade soldered solid-state storage module	Provides solid state storage through SATA 1 port

Key:
U1 - CPU
U13 - BMC
U25 - DDR3L SDRAM
U26 - DDR3L SDRAM

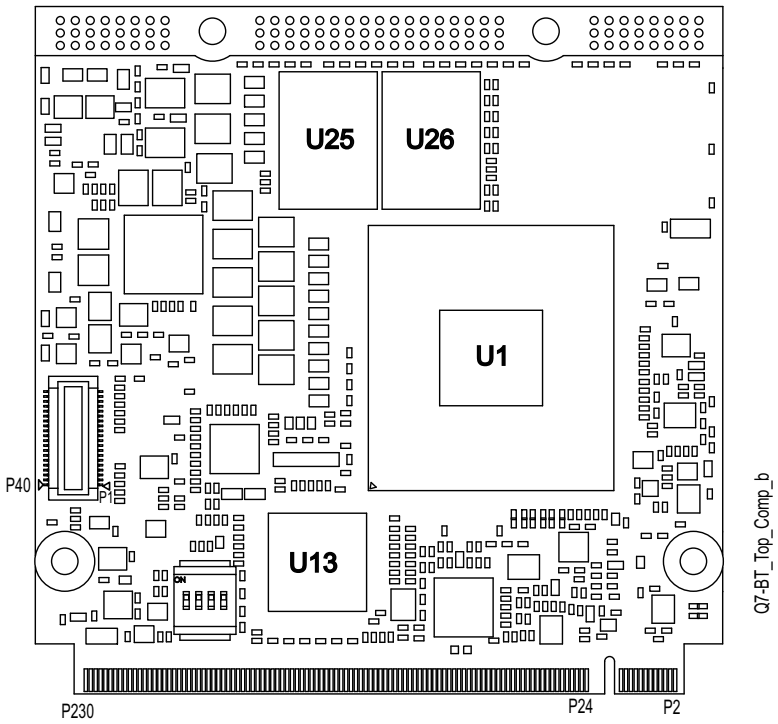


Figure 2-1: Component Locations (Top Side)

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Key:
U9 - GbE Controller
U19 - BIOS 0
U20 - BIOS 1
U24 - DDR3L SDRAM
U27 - DDR3L SDRAM
U48 - eMMC NAND Flash
U73 - SSD NAND, SATA

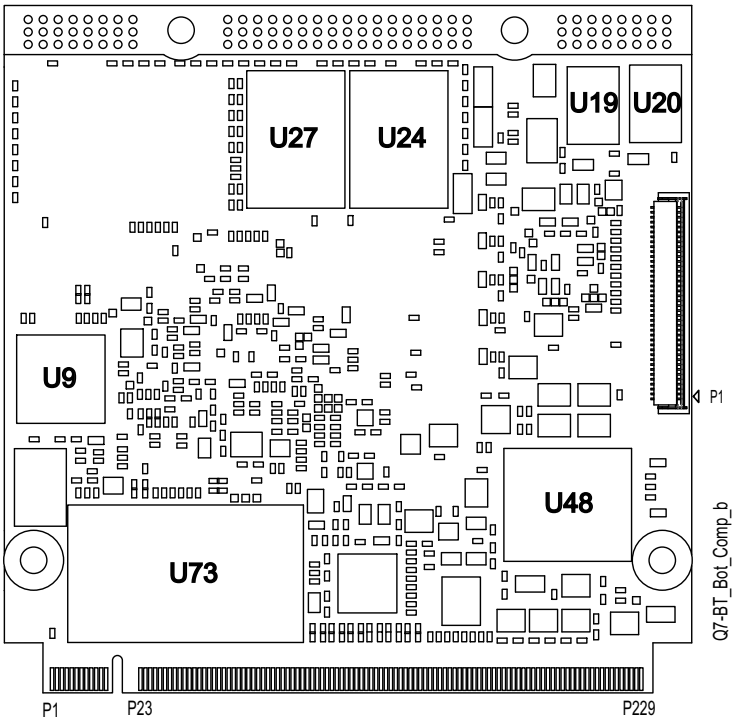


Figure 2-2: Component Locations (Bottom Side)

2.2 Connectors, Switches, and LEDs

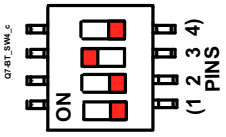
Table 2-2 describes the connectors, switches, and LEDs shown in Figure 2-3 and Figure 2-4.

Table 2-2: Module Connector Description

Connector#	Board Access	Description
CN1	Bottom	40-pin, DB40 Front-Flip connector for debug card (Molex, 502790-4091)
CN3	Top	40-pin, board-to-FPC connector for MIPI camera interface (Hirose, DF23C-40DS-0.5V)
GF1 - Q7 Primary and Secondary	Top/ Bottom	230-pin, MXM edge connector for Memory, Video, and I/O functions
LED1	Top	Blue LED indicating system status activities for HW Reset, SW Reset, Power Up, Power Down, Reset Button, and Power Button
LED2	Top	Green LED for Power On

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Table 2-2: Module Connector Description (Continued)

Connector#	Board Access	Description
SW4	Top	4-pin dip switch for the following BIOS control functions. (Diptronics, DHNF-04-T-Q-T/R) • Pin 1 = Loading BIOS setup defaults at Boot Up (OFF - default) • Pin 2 = Enabling WDT (OFF - default) • Pin 3 = Selecting BIOS (OFF - Fail-safe BIOS1; ON - Standard BIOS0 [default]) **Note**: The BIOS_DISABLE# signal on the Q7 connector must be pulled low before Pin 3 can be used to select Fail-Safe BIOS1. • Pin 4 = Selecting 18/24 bit LVDS modes (OFF - 18bit [default]; ON - 24bit) Switch Default Settings 

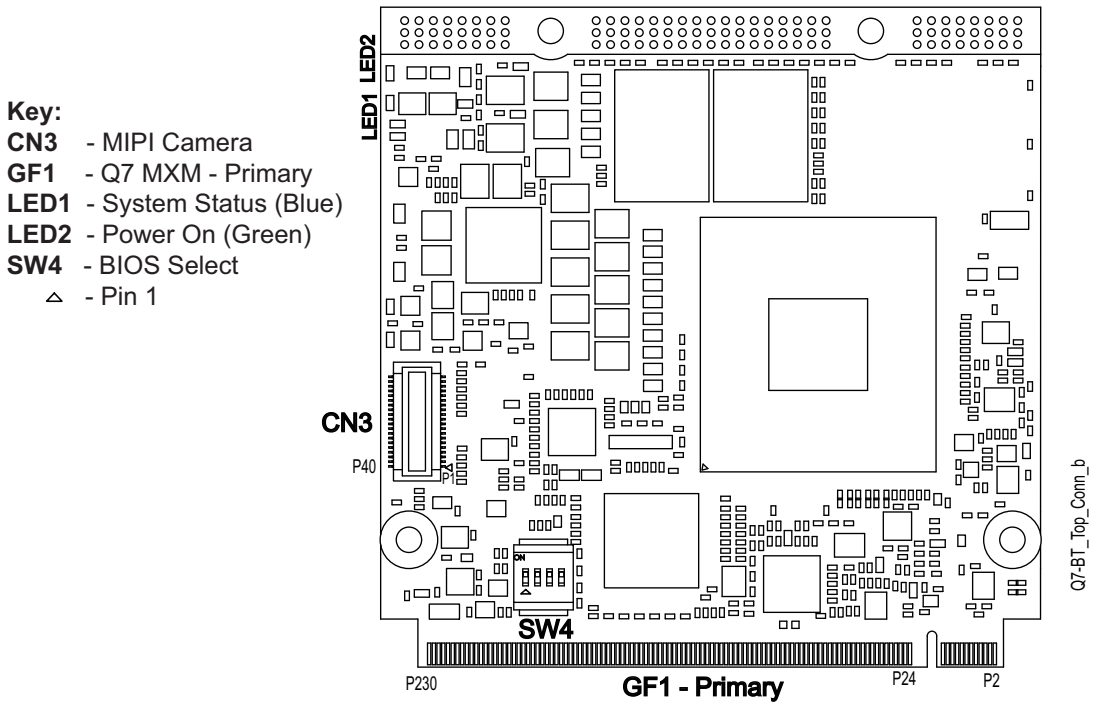


Figure 2-3: Connector Locations (Top Side)

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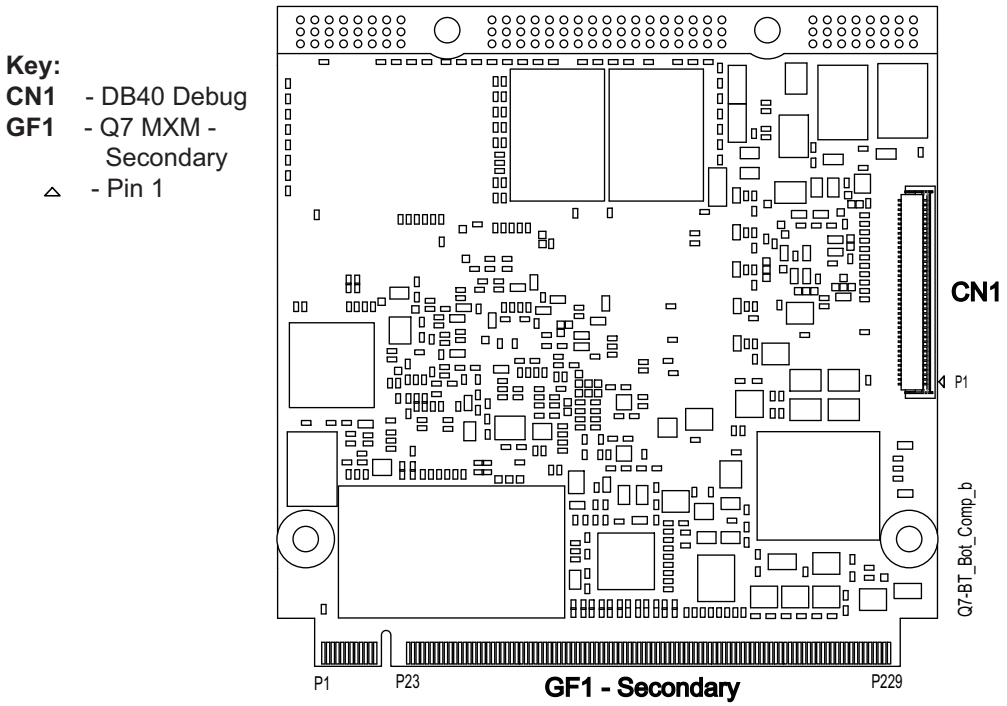


Figure 2-4: Connector Locations (Bottom Side)

2.3 Component Features

This section further describes the supported features of the Q7-BT major on-board components.

2.3.1 CPU

The Q7-BT product family offers multiple versions of the Intel Atom E3800 Series CPU, System-on-Chip (SoC): the E3815 (Single Core), the E3825 (Dual Core), the E3826 (Dual Core), and the E3845 (Quad Core). E3800 CPUs feature the Intel 64 Architecture and are manufactured based on Intel's 22-nanometer technology. Refer to the E3800 data sheet at the Intel website.

2.3.2 Memory

The Q7-BT employs one channel of 64-bit DDR3L on-board memory. Four SDRAM memory chips provide up to 16Gb of low-voltage non-ECC, unbuffered system memory. Refer to the SDRAM data sheets at the Micron and IM Intelligent websites. Depending on the SDRAM chips featured on the module, the following total SDRAM capacities are supported:

- 4x 128M16 = 1 GB
- 4x 256M16 = 2 GB
- 4x 512M16 = 4 GB

2.3.3 eMMC NAND Flash

The module supports an optional, on-board eMMC (Multi-Media Card) NAND chip with capacity up to 64GB. The data signals are routed from the NAND chip through the SDIO pins on the Q7 connector. Refer to the MTFC8GLDEA-4M-IT NAND Flash data sheet at the Micron website.

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2.3.4 SATA SSD (Solid State Drive)

The Q7-BT features an optional SATA SSD, soldered directly to the board and routed through the SATA1 port. For more information, refer to the SSD data sheet at the Greenliant website.

2.3.5 SMBus Slave Addresses

Figure 2-1 lists the corresponding slave addresses of the devices on the SMBus.

Table 2-1: SMBus Slave Addresses

Address (HEX)	Function	Device
(50)	BMC/SEMA	BMC
(6A)	DP to LVDS	RTD2136R
(2C)[7]	USB-Hub	USB2514Bi

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3 Interfaces

This section provides descriptions of the interfaces and signals within the Q7-BT P-S (Primary-Secondary) Qseven connector. Refer to the Qseven specification at: http://www.sget.org/standards/qseven.html for complete definitions of all the Qseven interfaces. The Q7-BT P-S (Primary-Secondary) Qseven connector provides the following interfaces:

- LVDS
- HDMI
- Camera MIPI-CSI
- Audio
- PCI Express (PCIe)
- Gb Ethernet
- USB 2.0
- USB 3.0
- SATA
- I2C
- SPI
- Serial UART
- SD/SDIO
- eMMC
- Debug



NOTE:

ADLINK Technology, Inc. only supports the features/ options tested and listed in this manual. The main chips used in the Q7-BT may provide more features or options than are listed for the Q7-BT, but some of these features or options are not supported on the module and will not function as specified in the chip documentation.

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3.1 18/24-Bit LVDS LCD

The LVDS interface is connected to the DDI0 interface of the CPU, while the translations of the DDI signals are made by a DisplayPort™-to-LVDS converter. The Realtek RTD2136R-CG, DisplayPort-to-LVDS converter receives one lane of DisplayPort signals and generates one port of LVDS output. The interface supports resolutions up to 1920x1200 at 60Hz (for 18-bit color depth.) The backlight enable, display enable, and PWMOUT functions originate from the BMC and the CPU and can be controlled from the BIOS setup utility.

3.2 HDMI or Display Port (DP)

The default setup defines the DDI1 port as HDMI (TMDS) or DP and provides the following features:

- 1 Clock pair
- 3 Data pairs
- Service signals
- HDMI resolutions up to 1920x1200 at 60Hz
- DP resolutions up to 2560x1600 at 60Hz

Select between DisplayPort and HDMI in the Advanced Graphics menu of the BIOS setup utility. The HDMI interface is compliant with the HDMI 1.4 specification.

3.3 Camera MIPI-CSI

The Q7-BT provides a 40-pin, on-board MIPI-CSI 2.0 (serial) camera connector with two clock lanes and five data lanes supporting up to 800 Mbit/s of actual pixels.

3.4 Audio (HDA)

The CPU provides an HDA controller, which communicates with internal or external CODECs over the Intel HDA serial link. HDA signals are brought out through pins 59, 61, 63, 65, 67 on the Qseven connector.


NOTE:

One audio link can be routed through the DDI1 interface and one link can be routed to the audio CODEC on the base board. Consequently, audio over DisplayPort/HDMI and the use of an audio CODEC can be implemented at the same time.

3.5 PCI Express (PCIe)

The CPU features four PCIe x1 ports, and the Q7-BT module uses three of them for the PCIe interface and one of them for the Gigabit Ethernet interface. The PCIe interface supports the PCIe Base Specification 2.0 with a maximum signal rate of 5 GT/s and can be configured to support PCIe edge cards or Express Cards.

3.6 Gigabit Ethernet

The on-board Intel I210IT Ethernet controller uses PCIe x1 (v2.1) bus signals from the CPU to enable 10T/100TX/1000T operation through integrated MAC, PHY, and SGMII/SerDes interfaces.

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3.7 USB Ports

The USB interface provides five USB 2.0 host ports, one USB 2.0 client port, and one USB 3.0 host port.


NOTE:

For the USB 3.0 port to support a full super-speed connector, it must use one of the USB 2.0 host ports, leaving four 2.0 ports available.

3.8 SATA

The SATA interface provides two ports through the SATA0 and SATA1 pins on the Q7-BT connector. The interface supports 1.5Gb/s and 3.0Gb/s. One of the SATA ports is shared with the PCIe Mini Card socket on the baseboard.

3.9 I2C Bus

The Q7-BT provides two interfaces through the I2C bus for General Purpose and LCD video with operating speeds up to 400kHz. All I2C interfaces have 3.3V pull ups with 2.2k resistors.

3.10 SPI

The CPU implements an SPI controller, which supports two SPI Flash devices on the module for BIOS storage.

3.11 Serial (UART)

The Q7-BT provides one serial interface: one high-speed, 4-wire port with TX/RX and RTS#/CTS# signals.

3.12 SD/SDIO Interface

Four parallel data lines comprise the SD/SDIO interface, supporting SD Card sockets.

3.13 eMMC Interface

The Q7-BT provides one 8-bit eMMC interface port, brought out from the CPU through the SDIO pins on the Qseven connector. If the optional eMMC NAND chip is present on the module, the eMMC interface will not be available for the baseboard on the Qseven connector.

3.14 LPC Debug Interface

A 40-pin, front flip, DB40 connector allows access to the system to debug and update the BIOS, BMC, and OS code. (Refer to “Debug (DB40) Connector Signals” on page 25.)

3.15 MIPI CSI Camera Interface

A 40-pin, board-to-FPC connector provides MCSI signals for MIPI CSI camera devices. (Refer to “MIPI CSI Camera Connector Signals” on page 26.)

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3.16 Qseven Interface Signals

Table 3-1 provides the pin signals for the Qseven connector. Refer to the Qseven specification at http://www.sget.org/standards/qseven.html for further definitions of the Qseven signals.

Table 3-1: Q7 Interface (GF1) Signal Descriptions

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
1	GND	2	GND
3	GBE_MDI3- (Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/ sec Gigabit Ethernet mode.)	4	GBE_MDI2- (Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/ sec Gigabit Ethernet mode.)
5	GBE_MDI3+ (Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/ sec Gigabit Ethernet mode.)	6	GBE_MDI2+ (Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/ sec Gigabit Ethernet mode.)
7	GBE_LINK100# (Ethernet controller 0 100Mbit/sec link indicator, active low.)	8	GBE_LINK1000# (Ethernet controller 0 1000Mbit/sec link indicator, active low.)
9	GBE_MDI1- (Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.)	10	GBE_MDI0- (Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.)
11	GBE_MDI1+ (Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.)	12	GBE_MDI0+ (Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.)
13	GBE_LINK# (Ethernet controller 0 link indicator, active low.)	14	GBE_ACT# (Ethernet controller 0 activity indicator, active low.)
15	GBE_CTREF (Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less.)	16	SUS_S5# (S5 State: This signal indicates S4 or S5 [Soft Off] state.)
17	WAKE# (External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.)	18	SUS_S3# (S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.)
19	SUS_STAT# (Suspend Status: indicates that the system will be entering a low power state soon.)	20	PWRBTN# (Power Button: Low active power button input. This signal is triggered on the falling edge.)

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Table 3-1: Q7 Interface (GF1) Signal Descriptions (Continued)

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
21	SLP_BTN# (Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.)	22	LID_BTN# (LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. Open/ Close state may be software configurable.)
23	GND	24	GND
	KEY		KEY
25	GND	26	PWGIN
27	BATLOW# (Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.)	28	RSTBTN# (High active input for the Qseven module indicates that all power rails located on the carrier board are ready for use.)
29	SATA0_TX+ (Serial ATA channel 0, Transmit Output differential pair.)	30	SATA1_TX+ (Serial ATA channel 1, Transmit Output differential pair; not available if optional SATA SSD is installed)
31	SATA0_TX- (Serial ATA channel 0, Transmit Output differential pair.)	32	SATA1_TX- (Serial ATA channel 1, Transmit Output differential pair; not available if optional SATA SSD is installed)
33	SATA_ACT# (Serial ATA Led. Open collector output pin driven during SATA command activity.)	34	GND
35	SATA0_RX+ (Serial ATA channel 0, Receive Input differential pair.)	36	SATA1_RX+ (not available if optional SATA SSD is installed)
37	SATA0_RX- (Serial ATA channel 0, Receive Input differential pair.)	38	SATA1_RX- (Serial ATA channel 1, Receive Input differential pair; not available if optional SATA SSD is installed)
39	GND	40	GND
41	BIOS_DISABLE# (Module BIOS disable input signal. Pull low to disable module's on-board BIOS. Allows off-module BIOS implementations.)	42	SDIO_CLK# (SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.)
43	SDIO_CD# (SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.)	44	SDIO_LED (SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.)
45	SDIO_CMD (SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.)	46	SDIO_WP (SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.)
47	SDIO_PWR# (SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.)	48	SDIO_DAT1 (These signals operate in push-pull mode.)
49	SDIO_DAT0 (These signals operate in push-pull mode.)	50	SDIO_DAT3 (These signals operate in push-pull mode.)
51	SDIO_DAT2 (These signals operate in push-pull mode.)	52	Not Connected
53	Not Connected	54	Not Connected

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Table 3-1: Q7 Interface (GF1) Signal Descriptions (Continued)

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
55	Not Connected	56	RSVD
57	GND	58	GND
59	HDA_SYNC (Serial Bus Audio Synchronization.)	60	SMB_CLK (Clock line of System Management Bus.)
61	HDA_RST#(HD Audio/AC'97 Codec Reset.)	62	SMB_DAT (Data line of System Management Bus.)
63	HDA_BITCLK (HD Audio/AC'97 24 MHz Serial Bit Clock from Codec)	64	SMB_ALERT# (System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.)
65	HDA_SDI (HD Audio/AC'97 Serial Data Input from Codec)	66	GPO_I2C_CLK (General Purpose I²C bus #0 clock line.)
67	HDA_SDO (HD Audio/AC'97 Serial Data Output to Codec)	68	GPO_I2C_DAT (General Purpose I²C bus #0 data line.)
69	THRM# (Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.)	70	WDTRIG# (Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven module on the falling edge of a low active pulse.)
71	THRMTRIP# (Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active, the system immediately transitions to the S5 State [Soft Off].)	72	WDOUT (Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.)
73	GND	74	GND
75	USB_SSTX0- [USB 3.0] (Multiplexed with transmit signal differential pairs for the Superspeed USB data path.)	76	USB_SSRX0- [USB 3.0] (Receive signal differential pair for the Superspeed USB data path.)
77	USB_SSTX0+ [USB 3.0] (Multiplexed with transmit signal differential pairs for the Superspeed USB data path.)	78	USB_SSRX0+ [USB 3.0] (Receive signal differential pair for the Superspeed USB data path.)
79	USB_6_7_OC# (Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.)	80	USB_4_5_OC# (Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.)
81	USB_P5- (Universal Serial Bus Port 5 differential pair.)	82	USB_P4- (Universal Serial Bus Port 4 differential pair.)
83	USB_P5+ (Universal Serial Bus Port 5 differential pair.)	84	USB_P4+ (Universal Serial Bus Port 4 differential pair.)
85	USB_2_3_OC# (Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.)	86	USB_0_1_OC# (Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.)
87	USB_P3- (Universal Serial Bus Port 3 differential pair.)	88	USB_P2- (Universal Serial Bus Port 2 differential pair.)
89	USB_P3+ (Universal Serial Bus Port 3 differential pair.)	90	USB_P2+ (Universal Serial Bus Port 2 differential pair.)

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Table 3-1: Q7 Interface (GF1) Signal Descriptions (Continued)

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
91	USB_CC (USB Client Connect pin. If USB Port 1 is configured for client mode, then an externally connected USB host should set this signal to high-active in order to properly make the connection with the module's internal USB client controller. If the external USB host is disconnected, this signal should be set to low-active in order to inform the USB client controller that the external host has been disconnected. A level shifter/ protection circuitry should be implemented on.)	92	USB_ID (USB ID pin. Configures the mode of the USB Port 1. If the signal is detected as being 'high active' the BIOS will automatically configure USB Port 1 as USB Client and enable USB Client support. This signal should be driven as OC signal by external circuitry.)
93	USB_OTG- (USB client)	94	USB_P0- (Universal Serial Bus Port 0 differential pair.)
95	USB_OTG+(USB client)	96	USB_P0+ (Universal Serial Bus Port 0 differential pair.)
97	GND	98	GND
99	eDP0_TX0+ (option) / LVDS_A0+ (LVDS primary channel differential pair 0. Embedded Display Port primary channel differential pair 0.)	100	LVDS_B0+ (LVDS secondary channel differential pair 0.)
101	eDP0_TX0- (option) / LVDS_A0- (LVDS primary channel differential pair 0. Embedded Display Port primary channel differential pair 0.)	102	LVDS_B0- (LVDS secondary channel differential pair 0.)
103	eDP0_TX1+ (option) / LVDS_A1+ (LVDS primary channel differential pair 1. Embedded Display Port primary channel differential pair 1.)	104	LVDS_B1+ (LVDS secondary channel differential pair 1.)
105	eDP0_TX1- (option) / LVDS_A1- (LVDS primary channel differential pair 1. Embedded Display Port primary channel differential pair 1.)	106	LVDS_B1- (LVDS secondary channel differential pair 1.)
107	eDP0_TX2+ (option) / LVDS_A2+ (LVDS primary channel differential pair 2. Embedded Display Port primary channel differential pair 2.)	108	LVDS_B2+ (LVDS secondary channel differential pair 2.)
109	eDP0_TX2- (option) / LVDS_A2- (LVDS primary channel differential pair 2. Embedded Display Port primary channel differential pair 2.)	110	LVDS_B2- (LVDS secondary channel differential pair 2.)
111	LVDS_PPEN (Controls panel power enable.)	112	LVDS_BLEN (Controls panel backlight enable.)
113	eDP0_TX3+ (option) / LVDS_A3+ (LVDS primary channel differential pair 3. Embedded Display Port primary channel differential pair 3.)	114	LVDS_B3+ (LVDS secondary channel differential pair 3.)

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Table 3-1: Q7 Interface (GF1) Signal Descriptions (Continued)

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
115	eDP0_TX3- (option) / LVDS_A3- (LVDS primary channel differential pair 3. Embedded Display Port primary channel differential pair 3.)	116	LVDS_B3- (LVDS secondary channel differential pair 3.)
117	GND	118	GND
119	eDP0_AUX+ (option) / LVDS_A_CLK+ (LVDS primary channel differential pair clock lines. Embedded Display Port primary auxiliary channel.)	120	LVDS_B_CLK+ (LVDS secondary channel differential pair clock lines.)
121	eDP0_AUX- (option) / LVDS_A_CLK- (LVDS primary channel differential pair clock lines. Embedded Display Port primary auxiliary channel.)	122	LVDS_B_CLK- (LVDS secondary channel differential pair clock lines.)
123	LVDS_BLT_CTRL (Primary functionality is to control the panel backlight brightness via pulse width modulation [PWM].)	124	GP_1-Wire Bus (General Purpose 1-Wire bus interface. Can be used for consumer electronics control bus (CEC) of HDMI)
125	LVDS_DID_DAT (Primary functionality DisplayID DDC data line used for LVDS flat panel detection.)	126	LVDS_BLC_DAT (Control data signal for external SSC clock chip.)
127	LVDS_DID_CLK (Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection.)	128	LVDS_BLC_CLK (Control clock signal for external SSC clock chip.)
129	Not Connected	130	Not Connected
131	DP_LANE3+/TMDS_CLK+ (DisplayPort differential pair lines lane 3, shared with TMDS differential pair clock lines.)	132	Not Connected
133	DP_LANE3-/TMDS_CLK- (DisplayPort differential pair lines lane 3, shared with TMDS differential pair clock lines.)	134	Not Connected
135	GND	136	GND
137	DP_LANE1+/TMDS_LANE1+ (DisplayPort differential pair lines lane 1, shared with TMDS differential pair lines lane 1.)	138	DDI1_AUX+ (Auxiliary channel used for link management and device control. Differential pair lines.)
139	DP_LANE1-/TMDS_LANE1- (DisplayPort differential pair lines lane 1, shared with TMDS differential pair lines lane 1.)	140	DDI1_AUX- (Auxiliary channel used for link management and device control. Differential pair lines.)
141	GND	142	GND
143	DP_LANE2+/TMDS_LANE0+ (DisplayPort differential pair lines lane 2, shared with TMDS differential pair lines lane 0.)	144	Not Connected
145	DP_LANE2-/TMDS_LANE0- (DisplayPort differential pair lines lane 2, shared with TMDS differential pair lines lane 0.)	146	Not Connected

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Table 3-1: Q7 Interface (GF1) Signal Descriptions (Continued)

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
147	GND	148	GND
149	DP_LANE0+/TMDS_LANE2+ (DisplayPort differential pair lines lane 0, shared with TMDS differential pair lines lane 2.)	150	HDMI_CTRL_DAT (DDC based control signal [data] for HDMI device. ***Note:*** *Level shifters must be implemented* on the carrier board for this signal in order to be compliant with the HDMI Specification.)
151	DP_LANE0-/TMDS_LANE2- (DisplayPort differential pair lines lane 0, shared with TMDS differential pair lines lane 2.)	152	HDMI_CTRL_CLK (DDC based control signal [clock] for HDMI device. ***Note:*** *Level shifters must be implemented* on the carrier board for this signal in order to be compliant with the HDMI Specification.)
153	DP_HDMI_HPD# (Hot plug detection signal that serves as an interrupt request.)	154	RSVD
155	PCIE_CLK_REF+ (PCI Express Reference Clock for Lanes 0 to 3.)	156	PCIE_WAKE# (PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.)
157	PCIE_CLK_REF- (PCI Express Reference Clock for Lanes 0 to 3.)	158	PCIE_RST# (Reset Signal for external devices.)
159	GND	160	GND
161	PCIE3_TX+ (PCI Express channel 3, Transmit Output differential pair.)	162	PCIE3_RX+ (PCI Express channel 3, Receive Input differential pair.)
163	PCIE3_TX- (PCI Express channel 3, Transmit Output differential pair.)	164	PCIE3_RX- (PCI Express channel 3, Receive Input differential pair.)
165	GND	166	GND
167	PCIE2_TX+ (PCI Express channel 2, Transmit Output differential pair.)	168	PCIE2_RX+ (PCI Express channel 2, Receive Input differential pair.)
169	PCIE2_TX- (PCI Express channel 2, Transmit Output differential pair.)	170	PCIE2_RX- (PCI Express channel 2, Receive Input differential pair.)
171	UART0_TX (Serial Data Transmitter)	172	UART0_RTS# (Handshake signal, ready to receive data)
173	PCIE1_TX+ (PCI Express channel 1, Transmit Output differential pair.)	174	PCIE1_RX+ (PCI Express channel 1, Receive Input differential pair.)
175	PCIE1_TX- (PCI Express channel 1, Transmit Output differential pair.)	176	PCIE1_RX- (PCI Express channel 1, Receive Input differential pair.)
177	UART0_RX (Serial Data Receiver)	178	UART0_CTS# (Handshake signal, ready to send data)
179	PCIE0_TX+ (PCI Express channel 0, Transmit Output differential pair.)	180	PCIE0_RX+ (PCI Express channel 0, Receive Input differential pair.)
181	PCIE0_TX- (PCI Express channel 0, Transmit Output differential pair.)	182	PCIE0_RX- (PCI Express channel 0, Receive Input differential pair.)
183	GND	184	GND
185	LPC_AD0 (Command, Address and Data 0 signal.)	186	LPC_AD1 (Command, Address and Data 1 signal.)
187	LPC_AD2 (Command, Address and Data 2 signal.)	188	LPC_AD3 (Command, Address and Data 3 signal.)
189	LPC_CLK (LPC clock.)	190	LPC_FRAME# (LPC frame indicates the start of a new cycle or the termination of a broken cycle.)

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Table 3-1: Q7 Interface (GF1) Signal Descriptions (Continued)

Pin #	Primary (Top Side)	Pin #	Secondary (Bottom Side)
191	SERIRQ (Serialized Interrupt.)	192	Not Connected
193	VCC_RTC (3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. [VCC_RTC = 2.4 - 3.3 V].)	194	SPKR (Output for audio enunciator, the “speaker” in PC AT systems.)
195	FAN_TACHOIN (Fan tachometer input.)	196	FAN_PWMOUT (Fan speed control. Uses the Pulse Width Modulation [PWM] technique to control the Fan's RPM based on the CPU's die temperature.)
197	GND	198	GND
199	SPI_MOSI (Master serial output/Slave serial input signal. SPI serial output data from Qseven module to the SPI device.)	200	SPI_CS0# (SPI Chip Select 0 output.)
201	SPI_MISO (Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven module.)	202	SPI_CS1# (SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.)
203	SPI_SCK (SPI clock output.)	204	Not Connected
205	VCC_5V_SB (Standby Power Supply +5VDC ±5%.)	206	VCC_5V_SB(Standby Power Supply +5VDC ±5%.)
207	Not connected	208	Not connected
209	Not connected	210	Not connected
211	VCC (Power Supply +5VDC ±5%.)	212	VCC (Power Supply +5VDC ±5%.)
213	VCC (Power Supply +5VDC ±5%.)	214	VCC (Power Supply +5VDC ±5%.)
215	VCC (Power Supply +5VDC ±5%.)	216	VCC (Power Supply +5VDC ±5%.)
217	VCC (Power Supply +5VDC ±5%.)	218	VCC (Power Supply +5VDC ±5%.)
219	VCC (Power Supply +5VDC ±5%.)	220	VCC (Power Supply +5VDC ±5%.)
221	VCC (Power Supply +5VDC ±5%.)	222	VCC (Power Supply +5VDC ±5%.)
223	VCC (Power Supply +5VDC ±5%.)	224	VCC (Power Supply +5VDC ±5%.)
225	VCC (Power Supply +5VDC ±5%.)	226	VCC (Power Supply +5VDC ±5%.)
227	VCC (Power Supply +5VDC ±5%.)	228	VCC (Power Supply +5VDC ±5%.)
229	VCC (Power Supply +5VDC ±5%.)	230	VCC (Power Supply +5VDC ±5%.)

NOTE: The # symbol indicates the signal is Active Low.

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3.17 Debug (DB40) Connector Signals

Table 3-1 lists the pin signals of the CN1 connector, which provides 40 pins, 1 row, consecutive sequence with 0.02" (0.50mm) pitch.

Table 3-1: Debug Interface Signals (CN2701)

Pin #	Interface	Signal
1	**NC**	RESVD
2	**For SMC Debug**	SMC_STATUS
3		BIOS_MODE
4		SEL_BIOS
5		POSTWDT_DIS#
6	**Test Point**	SUS_S5#
7		SUS_S4#
8		SUS_S3#
9		CB_PWROK
10		CB_RESET#
11		SYS_RESET#
12		PWRBTN#
13	**SMC Program Interface**	SMC_OCD0B
14		SMC_OCD0A
15		SMC_CLK
16		SMC_DATA
17		SMC_RESET_IN#
18		SMC_FLMD0
19		SMC_RXD6
20		SMC_TXD6
21		GND3
22		3V3_DUAL
23		3V3_SMC1
24	**LPC Debug Card Interface**	LPC_AD0
25		LPC_AD1
26		LPC_AD2
27		LPC_AD3
28		LPC_FRAME#
29		CLK33_LPC
30		RST#
31		BIOS_DIS0
32		GND2
33		LPC_3V3
34	**SPI Program Interface**	SPI_BIOS_CLK
35		SPI_BIOS_MOSI
36		SPI_BIOS_MISO
37		SPI_BIOS_CS1#
38		SPI_BIOS_CS0#
39		GND1
40		VCC_SPI_IN (SPI power input from flash tool to module)

NOTE: The gray table cells denote ground. The # symbol indicates the signal is Active Low.

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3.18 MIPI CSI Camera Connector Signals

Table 3-2 lists the pin signals of the CN3 connector, which provides 40 pins, 2 rows, consecutive sequence with 0.02" (0.50mm) pitch.

Table 3-2: MIPI CSI Camera Interface Signals (CN3)

Pin #	Signal	Pin #	Signal
1	MCSI_CAM0PWR#	40	MCSI_CAM1PWR#
2	MCSI_CAM0RST#	39	MCSI_CAM1RST#
3	GND	38	GND
4	Not Connected	37	CN_I2C_CAM_CK
5	V1P8S	36	CN_I2C_CAM_DAT
6	Not Connected	35	Not Connected
7	MCSI1_CLK_P	34	MCSI2_CLK_P
8	MCSI1_CLK_N	33	MCSI2_CLK_N
9	GND	32	GND
10	MCSI1_D0_P	31	MCSI2_D0_P
11	MCSI1_D0_N	30	MCSI2_D0_N
12	GND	29	GND
13	MCSI1_D1_P	28	MCSI3_CLK_P
14	MCSI1_D1_N	27	MCSI3_CLK_N
15	GND	26	Not Connected
16	MCSI1_D2_P	25	Not Connected
17	MCSI1_D2_N	24	GND
18	GND	23	V3P3S
19	MCSI1_D3_P	22	GND
20	MCSI1_D3_N	21	V5P0A

NOTE: The gray table cells denote ground or power. The # symbol indicates the signal is Active Low.

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4 Utilities

This chapter provides information on how to read information from and configure the BIOS Setup utility, the SEMA utility, the Watchdog Timer utility, and the board temperature sensors on the Q7-BT.

4.1 BIOS

The Q7-BT features an AMI BIOS. The default settings provide a “ready to run” system, even without a BIOS setup backup battery.

The BIOS is located in flash memory and can be easily updated with software under DOS.

All setup changes of the BIOS are stored in the CMOS RAM.

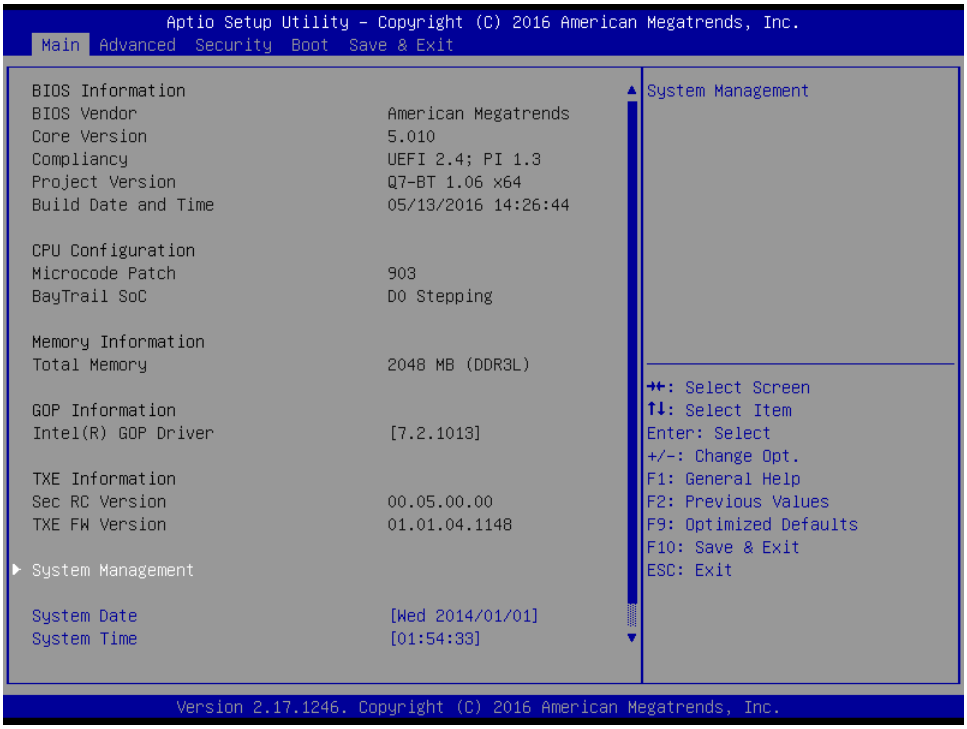
The soldered battery will provide power to store that information for over two years without board activation.

4.1.1 Configuring the BIOS

- Pressing <DEL> during power up starts the BIOS setup utility.
- Pressing <F11> during power up starts the boot menu.
- Pressing <END> during power up returns settings to default.

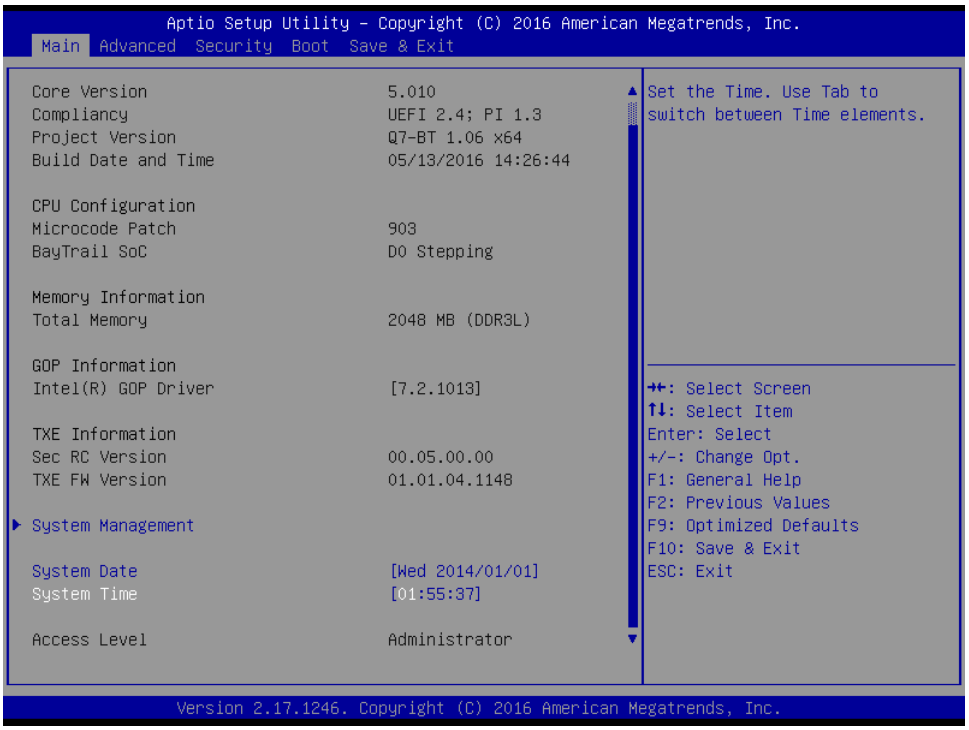
4.1.2 Main screen of the BIOS

The main screen of the BIOS SETUP UTILITY provides an overview of the BIOS version, the clock speed, installed memory, memory speed, date and time, and other system information. The date and time can be configured by the user.



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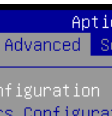
Main Screen > (Scrolled to Bottom)



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4.1.3 Advanced Settings screen

The main screen of “Advanced Settings” provides configuration settings for CPU, Graphics, SATA, USB, SDIO, Network, Audio, PCI/PCIe, Devices, ACPI, Serial, Thermal, Security, Miscellaneous, and SIO.


CAUTION:

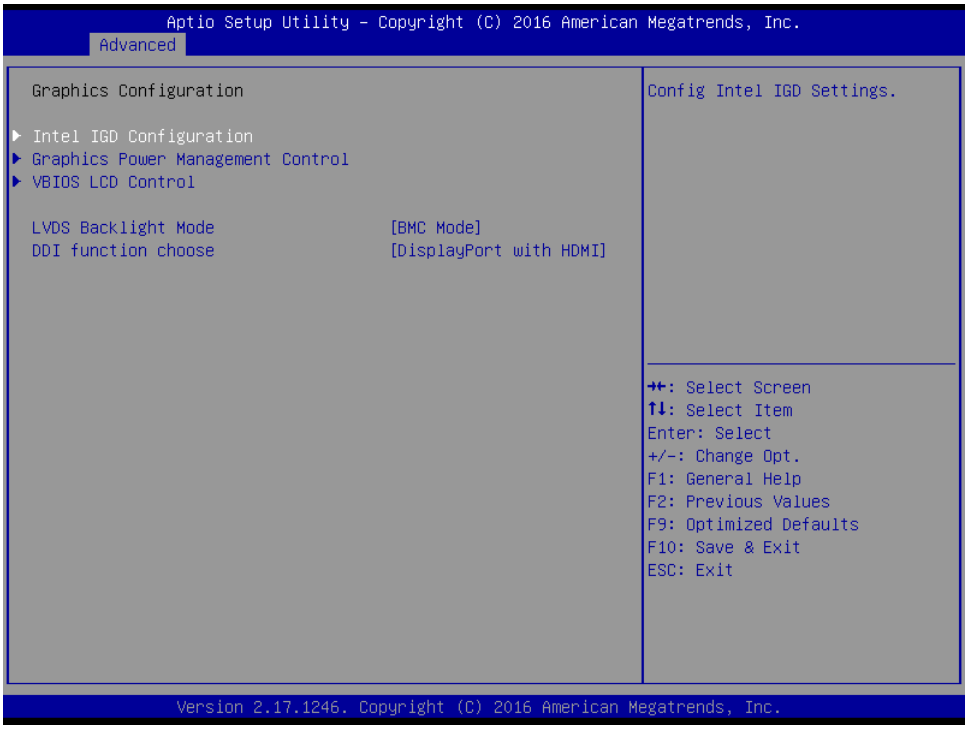
Inappropriate values for any of the following advanced settings below may cause the system to malfunction.

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Advanced > CPU

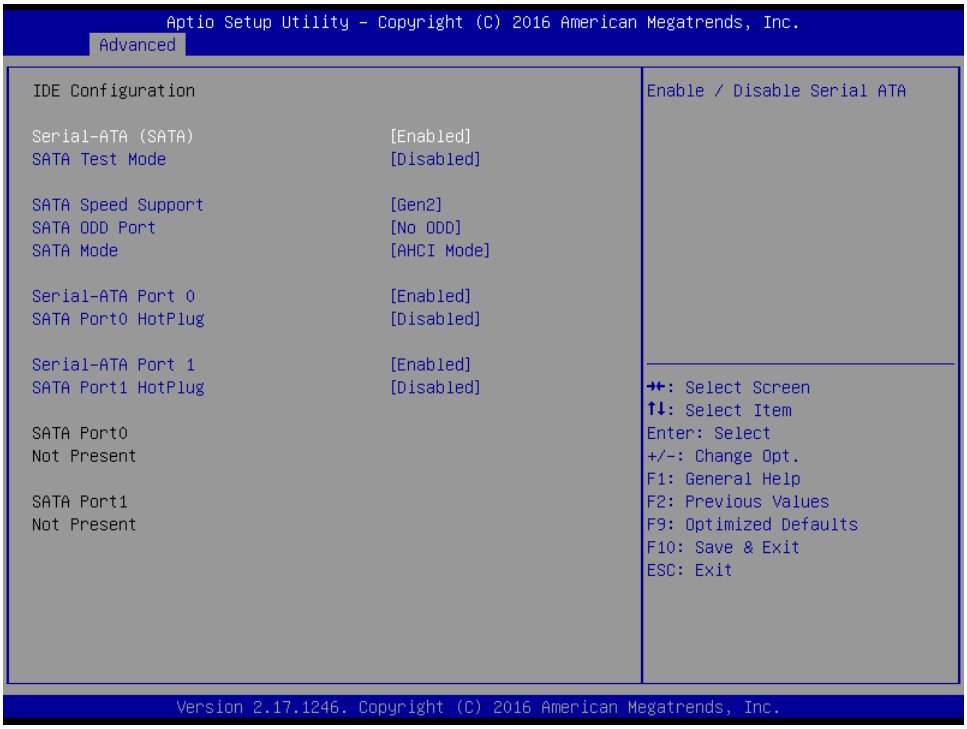


Advanced > Graphics

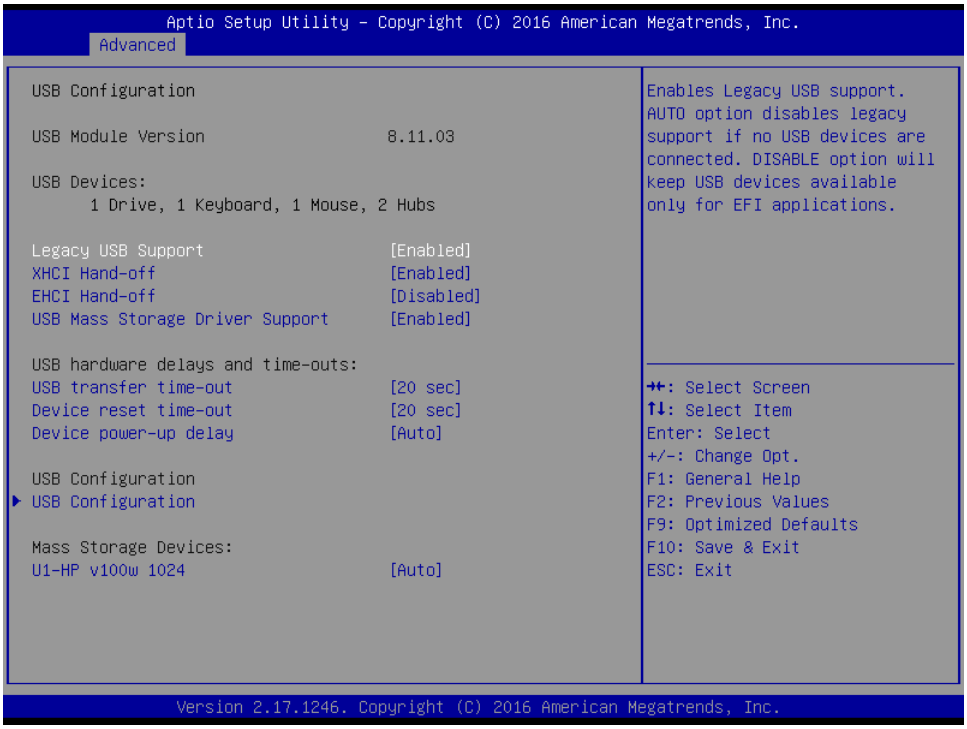


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Advanced > SATA

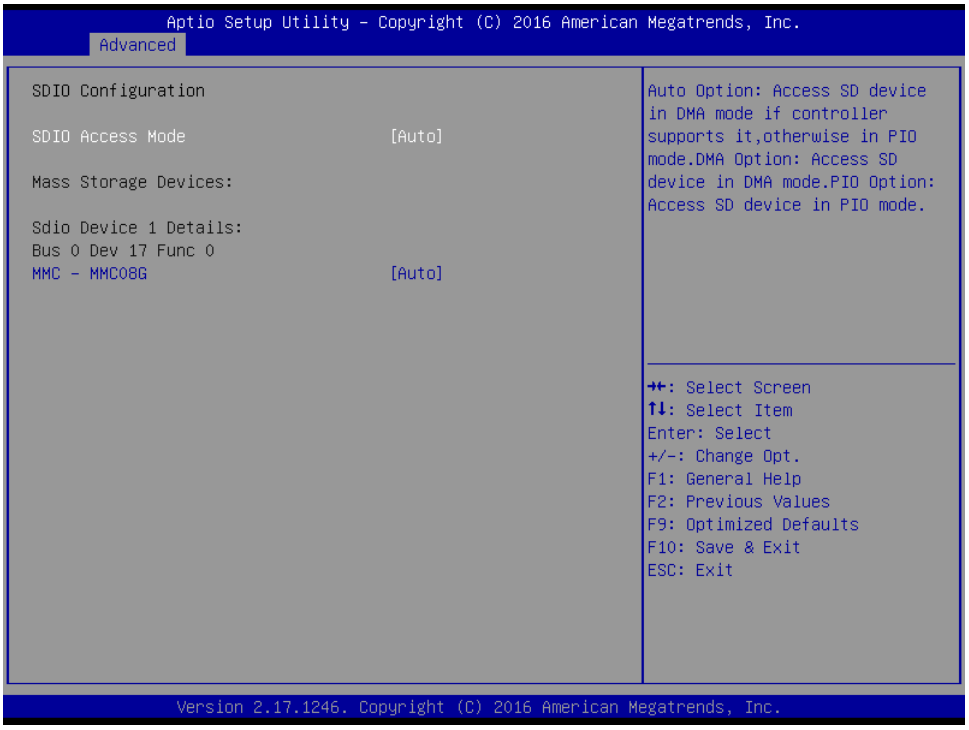


Advanced > USB

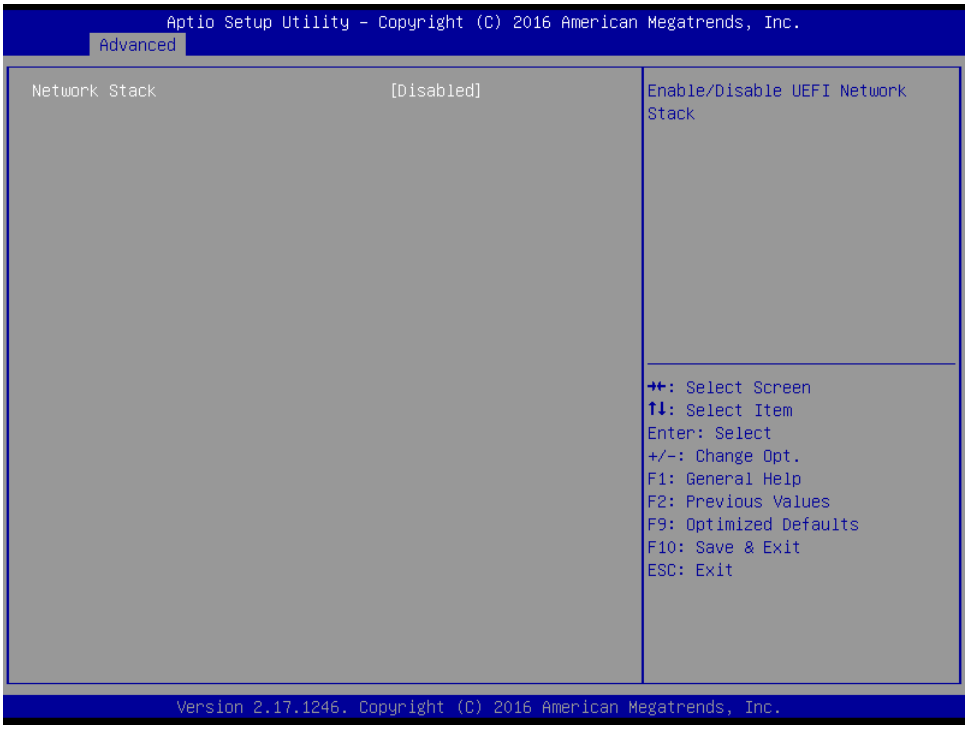


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Advanced > SDIO

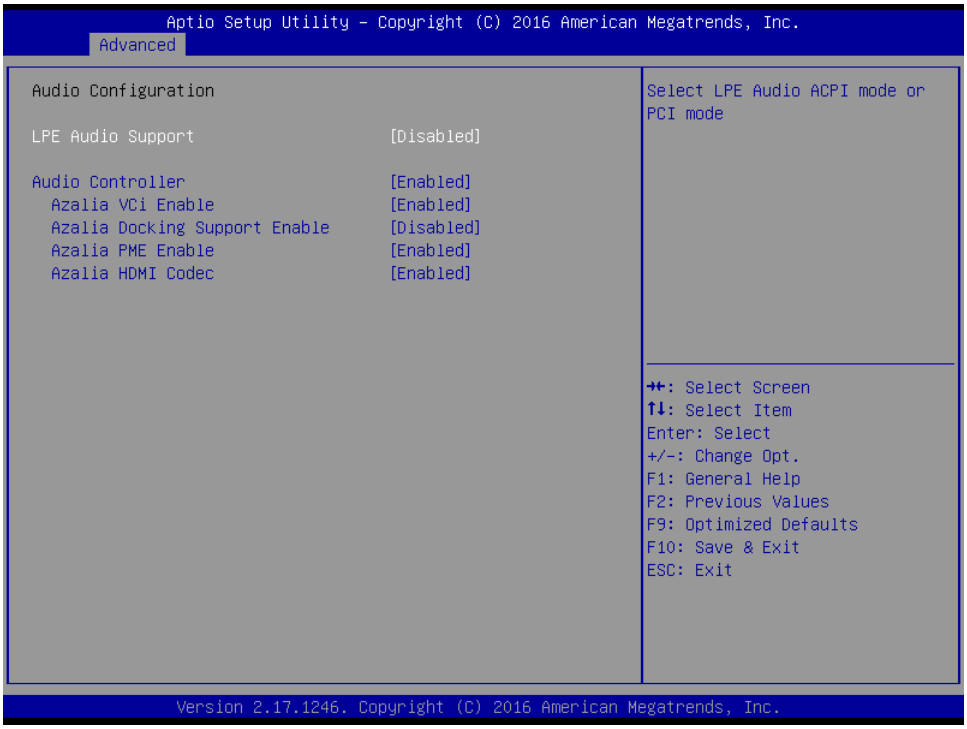


Advanced > Network

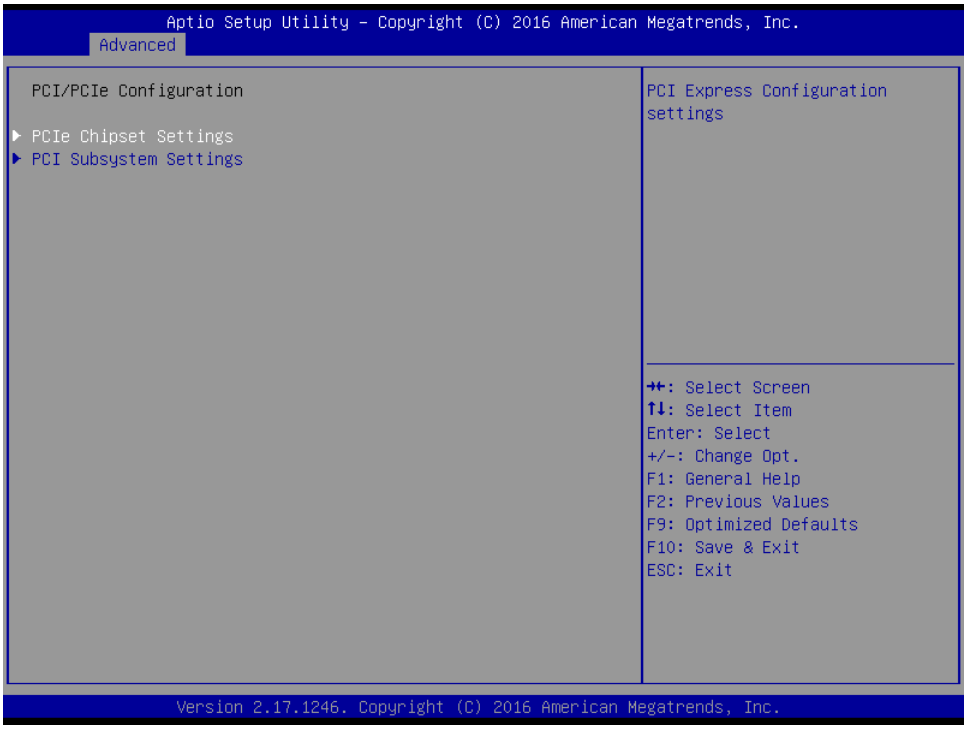


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Advanced > Audio

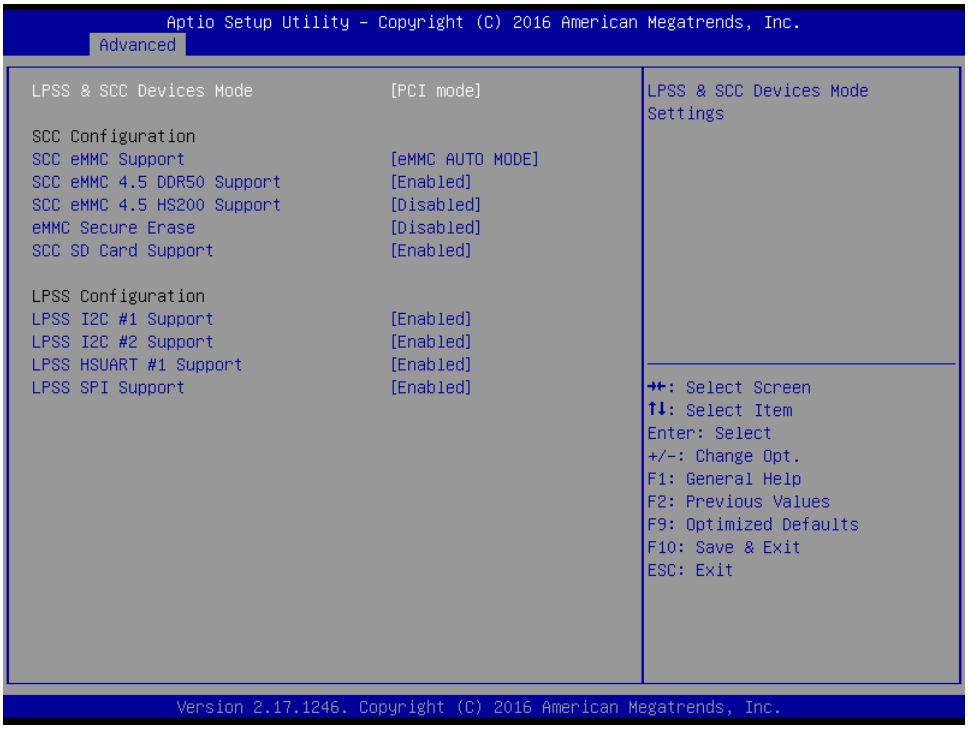


Advanced > PCI-PCIe

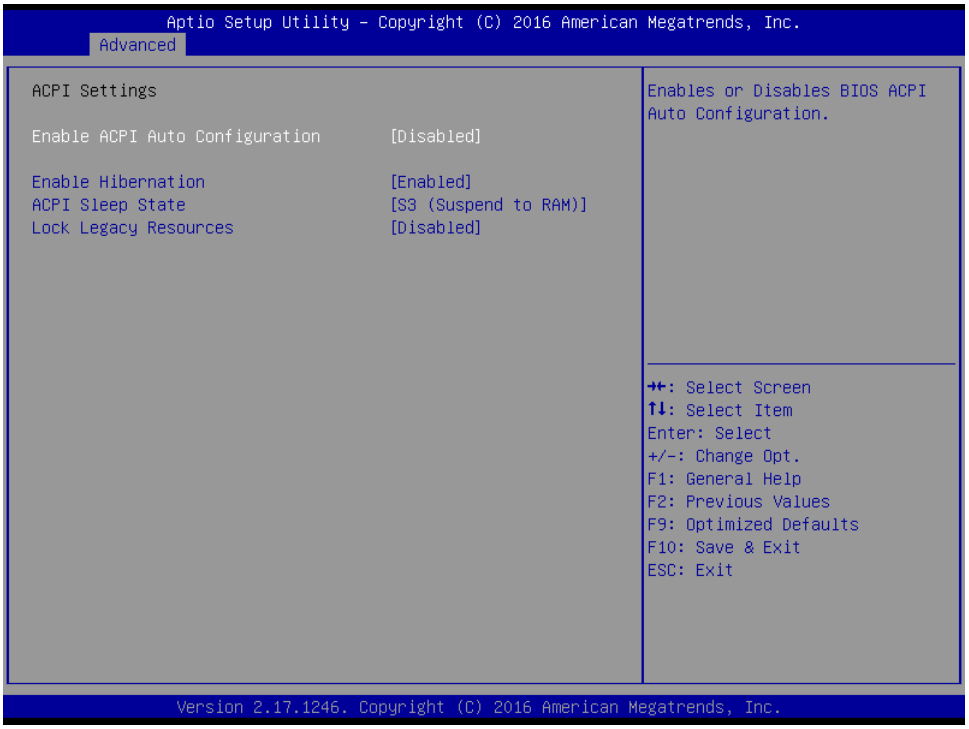


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Advanced > Devices

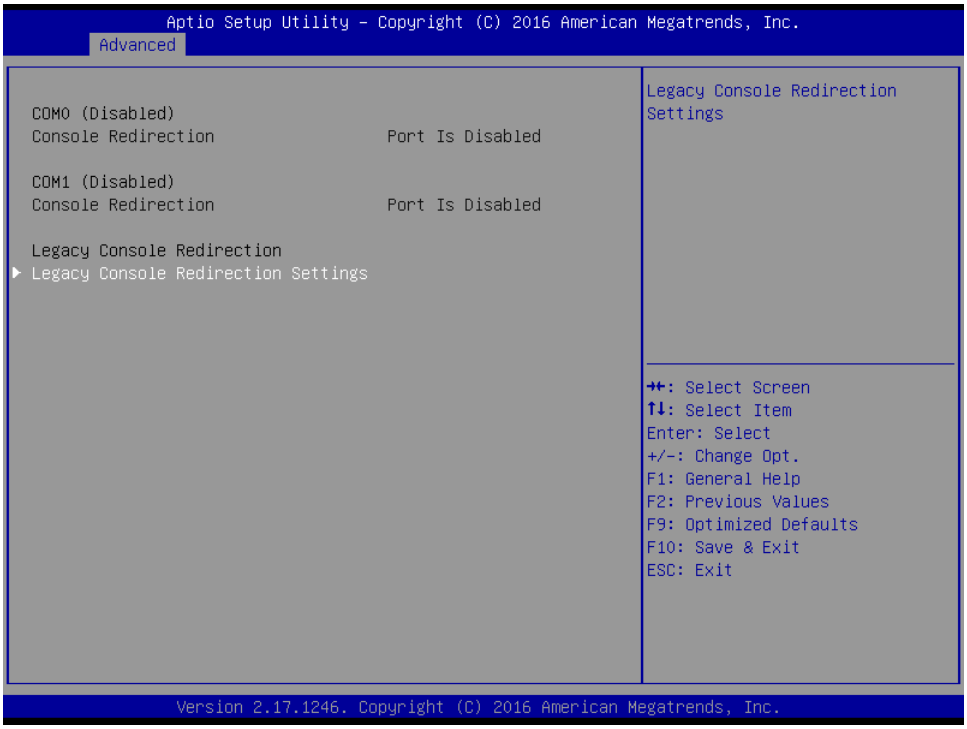


Advanced > ACPI



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Advanced > Serial

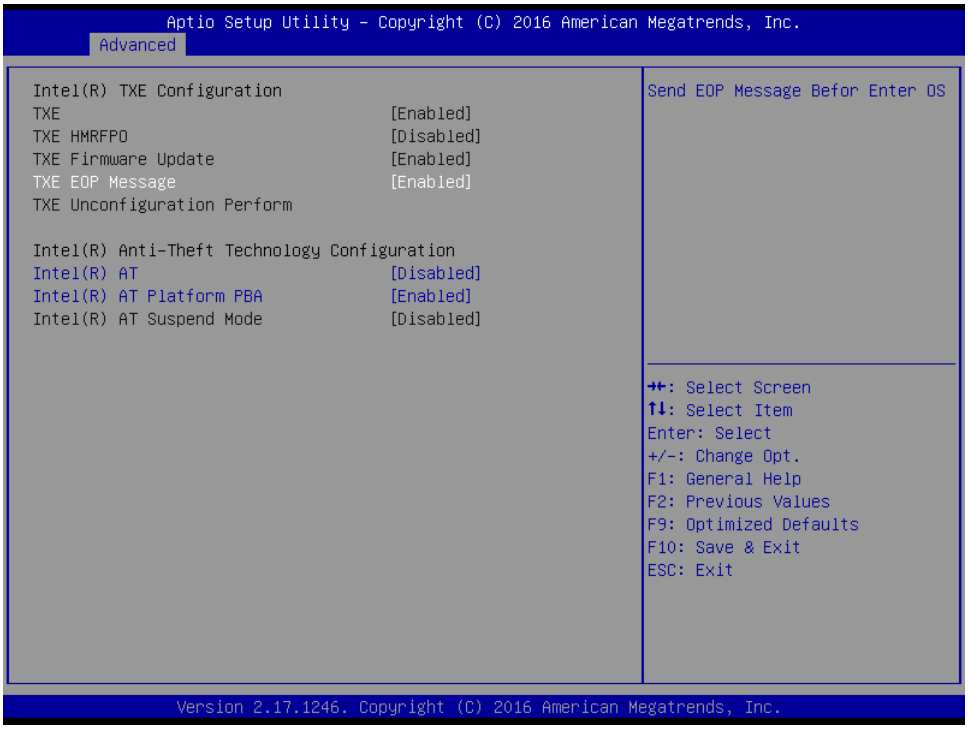


Advanced > Thermal

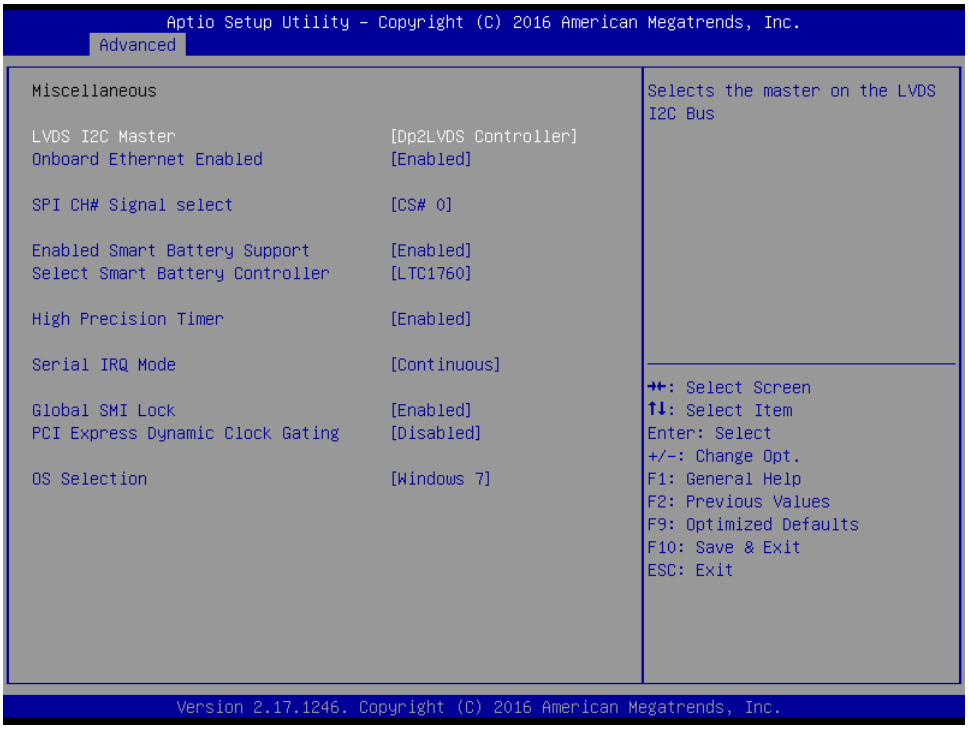


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Advanced > Security

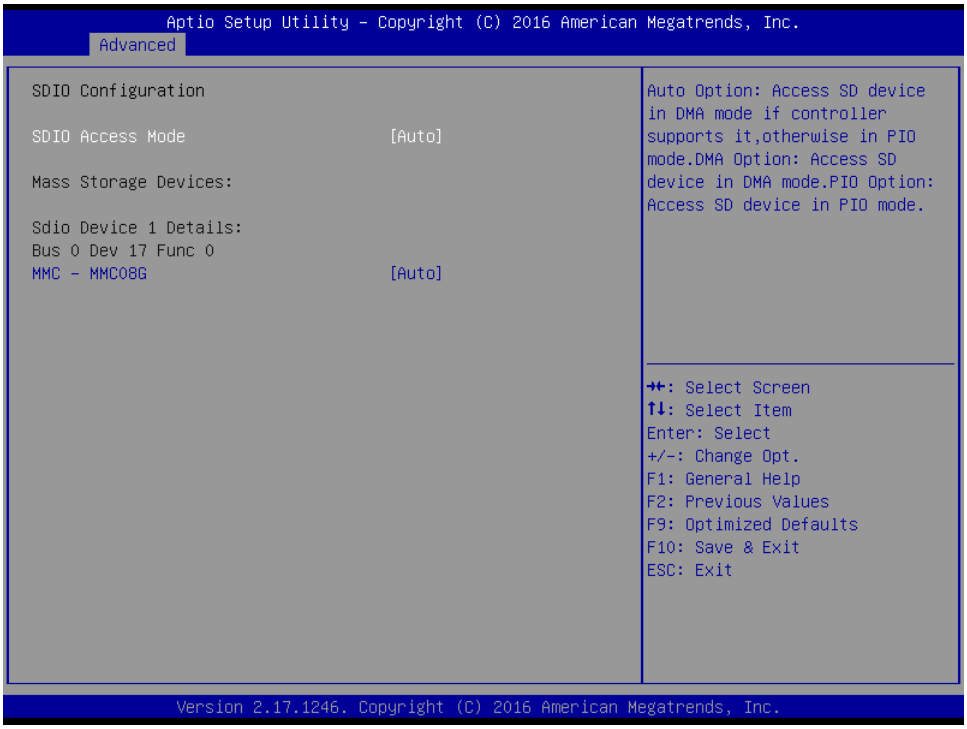


Advanced > Miscellaneous

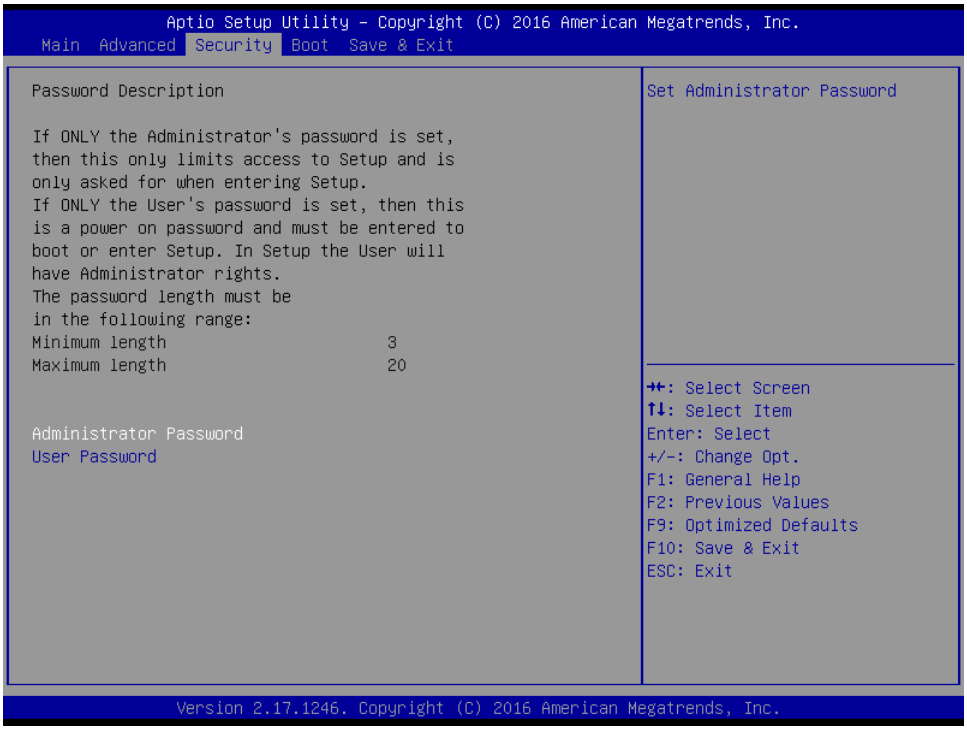


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Advanced > SIO



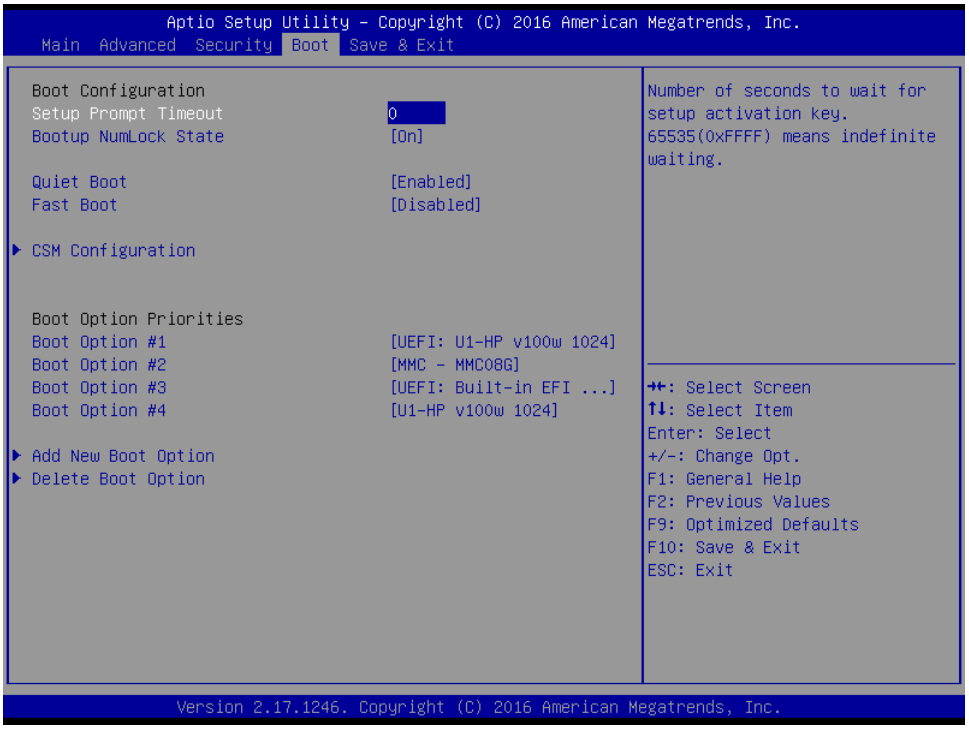
4.1.4 Security screen



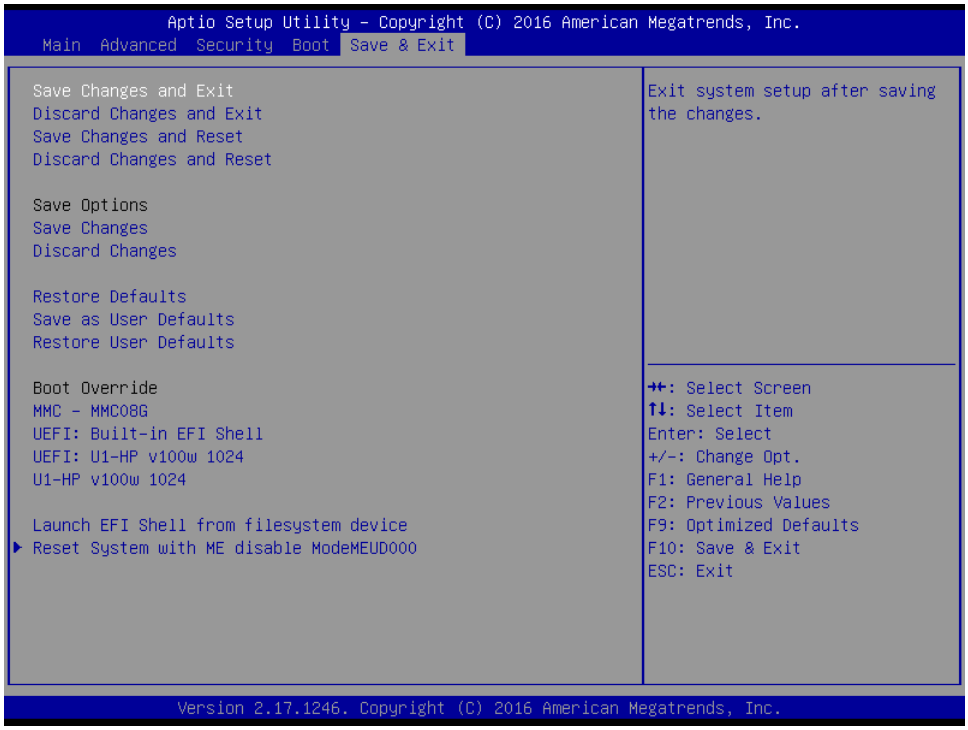
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4.1.5 Boot screen

If more than one drive is attached to the Q7-BT, you can select from the first “Boot Configuration” screen the boot order in which the drives are scanned for a bootable OS image.



4.1.6 Save & Exit screen



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4.2 SEMA functions

Under the management of the BMC chip (Board Management Controller), the SEMA utility (Smart Embedded Management Agent) provides system control and failure protection—counting, monitoring, and measuring hardware and software events, from which the SoC can trigger corrective commands. The optional SEMA Cloud utility not only controls local events on the module but system client events on the Internet of Things (IoT.) Refer to the following bullets for a list of SEMA functions.

- Total operating hours counter
  Counts the time the module has been run in minutes.
- On-time minutes counter
  Counts the seconds since last system start.
- Temperature monitoring of CPU and Board temperature
  Minimum and maximum temperature values of CPU and board are stored in flash.
- Power monitor
  Reads the current drawn by the board and reports the nominal operating voltage.
- Power cycles counter
- Boot counter
  Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
- Watchdog Timer
  Set / Reset / Disable Watchdog Timer.
- System Restart Cause
  Power loss / Watchdog / External Reset.
- Flash area
  1kB Flash area for customer data
- Protected Flash area
  128 Bytes for Keys, ID's, etc. can be stored in a write- and clear-protectable region.
- Board Identify
  Vendor / Board / Serial number

The SEMA Tools are available for Windows and Linux. SEMA functionality can also be used in applications. Refer to the SEMA software manual and technical manual on the ADLINK web site for more information.

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4.2.1 Board Specific SEMA functions

Voltages

The BMC of the Q7-BT implements a Voltage Monitor and samples several Onboard Voltages. The Voltages can be read by calling the SEMA function, “Get Voltages”. The function returns a 16-bit value divided in Hi-Byte (MSB) and Lo-Byte (LSB).

Table 4-1: BMC Voltage Monitor Values

ADC Channel	Voltage Name	Voltage Formula [V]
0	---	---
1	+V1.0S	(MSB<<8 + LSB) * 3.3 / 1024
2	+V1.2S	(MSB<<8 + LSB) * 3.3 / 1024
3	+V1.8S	(MSB<<8 + LSB) * 3.3 / 1024
4	+V3.3S	(MSB<<8 + LSB) * 1.100 * 3.3 / 1024
5	+V1.5S	(MSB<<8 + LSB) * 3.3 / 1024
6	+V5.0A	(MSB<<8 + LSB) * 1.833 * 3.3 / 1024
7	(MAINCURRENT)	Use Main Current Function

Main Current

The BMC of the Q7-BT implements a Current Monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in Hi-Byte (MSB) and Lo-Byte (LSB). These four values represent the last four currents drawn by the board. The values are sampled every 250ms. The order of the four values is NOT in relationship to time. The access to the BMC may increase the drawn current of the whole system. In this case, you still have three samples without the influence of the read access.

Main Current = (MSB_n<<8 + LSB_n) * 8.06mA

TS#-Events

TS# is activated by a temperature sensor when a device reaches its critical temperature and released when the device is back in its normal temperature range. This counter gives the user information about temperature or cooling issues. This counter is cleared when the system is removed from power. The Q7-BT only monitors the board temperature and does not support TS#-Events.

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Exception Blink Codes

In the case of an error, the BMC shows a blink code on the STATUS-LED (LED1). This error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash storage and is cleared when the power is removed. Therefore, the “Clear Exception Code”-Command is not supported.

Table 4-2: Blink Codes

Exception Blink Code	Error Message
0	NOERROR
2	NO_SUSCLK
3	NO_POWERUP
4	NO_SLP_S4
5	NO_SLP_S3
6	BIOS_FAIL
7	RESET_FAIL
8	POWER_FAIL
9	NO_PWGIN
10	BMC_VCC_S
11	BMC_VNN_S
12	BMC_V1P0A
13	BMC_VDDQ
14	BMC_V1P8A
18	LOW_VIN
19	RESETIN_FAIL
20	THERMTRIP_ACTIVE

BMC Flags

The BMC Flags register returns the last detected exception code since power up.

4.3 Watchdog Timer

The Q7-BT features three separate Watchdog Timers. One of them is integrated in the SoC and two are provided by the BMC (managed by the SEMA).

The SoC Watchdog can be configured in the BIOS or by programming the Watchdog registers. If this function is used by user application, the application has to provide all logging functionality if desired.

The BMC Watchdog activations are caused by under voltage protection. The Watchdog LED flashes after restart but only if the power supply reaches 4.2V.

4.4 Temperature Sensors

The Q7-BT provides three temperature sensors. One is offered from the SoC, one from the BMC (managed by the SEMA), and one from a dedicated chip on the board.

The SoC temperature sensor can be configured by programming the appropriate registers. This is usually done with a user application.

4.5 Programming Examples

Programming examples can be provided based on a Linux operating system, upon request.

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Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in Table A-1 below. Requests for support through Ask an Expert are given the highest priorities, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the ADLINK web site at http://askanexpert.adlinktech.com. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called “My ADLINK”, unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the My Question area where you can check status, update your request, and access other features.
- Download Service – This service is also free and available 24 hours a day using the web site link shown in Table A-1. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1: Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://askanexpert.adlinktech.com
Web Site	https://emb.adlinktech.com
Standard Mail	**ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110 San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

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Table A-1: Technical Support Contact Information (Continued)

	ADLINK Technology GmbH Address: Hans-Thoma-Strasse 11 D-68163 Mannheim, Germany Tel: +49-621-43214-0 Fax: +49-621 43214-30 Email: emea@adlinktech.com Please visit the contact page using the web site link shown above for information on how to contact the ADLINK regional office nearest you.

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