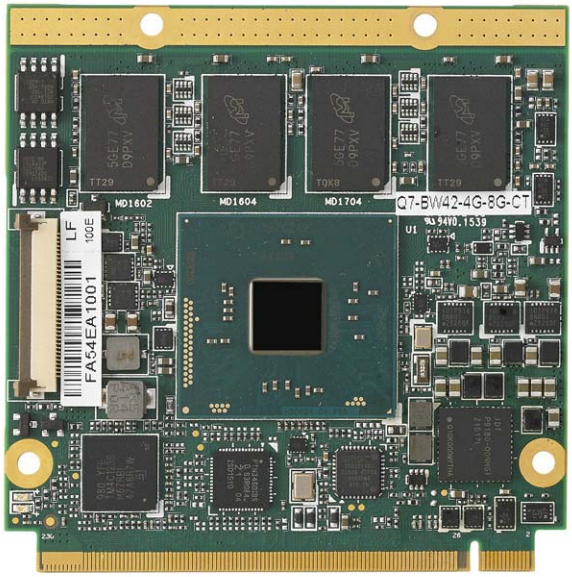
Q7-BW

(Computer On Module)

Technical Reference
P/N 50-1Z207-1000
Rev 1.00



STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

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Preface

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Revision History

Revision	Date	Description of Change(s)
1.00	06/22/2016	Initial Release

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Audience

This manual provides reference only for computer design engineers, including but not limited to hardware and software designers and applications engineers. ADLINK Technology, Inc. assumes you are qualified to design and implement prototype computer equipment.

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Important Safety Instructions

For user safety, please read and follow all **Instructions**, **WARNINGs**, **CAUTIONs,** and **NOTEs** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

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Conventions

The following conventions may be used throughout this manual, denoting special levels of information.



This information adds clarity or specifics to text and illustrations.



This information indicates the possibility of ***minor*** physical injury, component damage, data loss, and/or program corruption.



This information warns of possible ***serious*** physical injury, component damage, data loss, and/or program corruption.

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1 Product Overview

1.1 Description

The Q7-BW Computer-On-Module (COM) combines the Qseven® 2.0 standard with the Intel® Pentium® and Celeron® N-3000 series System-on-Chip (SoC), providing an ideal solution for low power consumption and high, pin/area density requirements. The module provides the high integration, high performance, low power, and ruggedness favored by Internet-of-Things (IoT) applications such as retail transactional clients, digital signage, and in-vehicle infotainment systems.

The Qseven form factor affords a more compact profile and footprint than the other COM platforms. Mechanical dimensions of 70mm width and 70mm length with 2.3mm of overall height ranks Qseven as the smallest COM standard currently available.

The Q7-BW module utilizes the Intel N3000 series SoC, which is based on the new Intel Architecture and is manufactured on Intel's industry-leading, tri-gate 14nm process. The module primarily targets entry-level 2-in-1 devices, laptops, desktops, and all-in-one PCs and supports contemporary, high-bandwidth interfaces such as Ultra HD HDMI, PCI Express Gen2, Gigabit Ethernet, USB 3.0, SATA Gen3, and a state-of-the-art HD Audio interface. The module generates its own LVDS (18/24bit), TMDS, and Display Port video signals using DDI output from the SoC.

A series of optional eMMC devices offers up to 64GB of on-board NAND Flash storage with an MMC interface, and an optional SATA, Solid State Drive (SSD) provides up to 64GB of on-board NAND Flash storage. Two SPI Flash chips implement a fail-safe BIOS, allowing the user to boot the module even if current BIOS settings have corrupted the system.

Under the management of the BMC chip (Board Management Controller), the SEMA utility (Smart Embedded Management Agent) provides system control, security, and failure protection—counting, monitoring, and measuring hardware and software events, and using the SMBus to send corrective commands to the SoC. The optional SEMA Cloud utility not only controls local events on the module but system client events on the IoT.

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1.2 Features

- CPU
  Intel® Pentium® and Celeron® N3000 Series, x86 dual-core or quad-core SoC (System On Chip) with integrated memory, graphics, and I/O. See website: http://www.intel.com
  - N3710 6W TDP, Pentium Quad-Core/2.56GHz burst freq./1600 MT/s /Gfx 700MHz
  - N3160 6W TDP, Celeron Quad-Core/2.24GHz burst freq./1600 MT/s /Gfx 640MHz
  - N3060 6W TDP, Celeron Dual-Core/2.48GHz burst freq./1600 MT/s /Gfx 600MHz
  - N3010 4W TDP, Celeron Dual-Core/2.24GHz burst freq./1600 MT/s /Gfx 600MHz
  - x5-E8000 5W TDP, Atom Quad-Core/2.00GHz burst freq./1600 MT/s /Gfx 320MHz
  - NOTE: Other CPU SKUs can be made available on request.
- Memory
  - Up to 8GB non-ECC, unbuffered soldered, DDR3L
  - 1600MHz
  - Dual channel
- Interface Standard
  - QSeven, board-to-board, Rev 2.0
- Expansion
  - PCI Express, Rev 2.0 supporting up to three x1 root ports at up to 5GT/s
- SATA
  - Two 6Gb/s, Gen 3 ports
  - Advanced Host Controller Interface (AHCI)
- USB
  - Six USB 2.0 host ports
  - One USB 3.0 host port
- Ethernet
  - Single-port, gigabit Ethernet controller
  - Integrated GbE MAC, PHY, and MDI ports
  - 10T/100TX/1000T signals using the PCIe x1 bus
- Serial UART
  - One high-speed, 4-wire port
  - Base frequency 50MHz
- I2C
  - One I2C bus
  - One SMBus
- SPI
  - One internal SPI controller
  - Two SPI flash devices for BIOS storage
  - One SPI interface on the Q7 connector
- Video
  - Display Port/HDMI
  - LVDS
- Audio
  - One HDA (High Definition Audio) interface
- CSI/MIPI Camera
  - One MIPI-CSI feature connector
  - Two MIPI-CSI camera interfaces
  - Camera, CSI1 (4 lanes)

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- Camera, CSI2 (2 lanes)

- Storage
  - One optional eMMC NAND (available in 4GB to 64GB capacities)
  - One optional SATA SSD (available in 8GB capacity; other capacities on request)
  - Two SPI flash devices for BIOS storage

1.3 Block Diagram

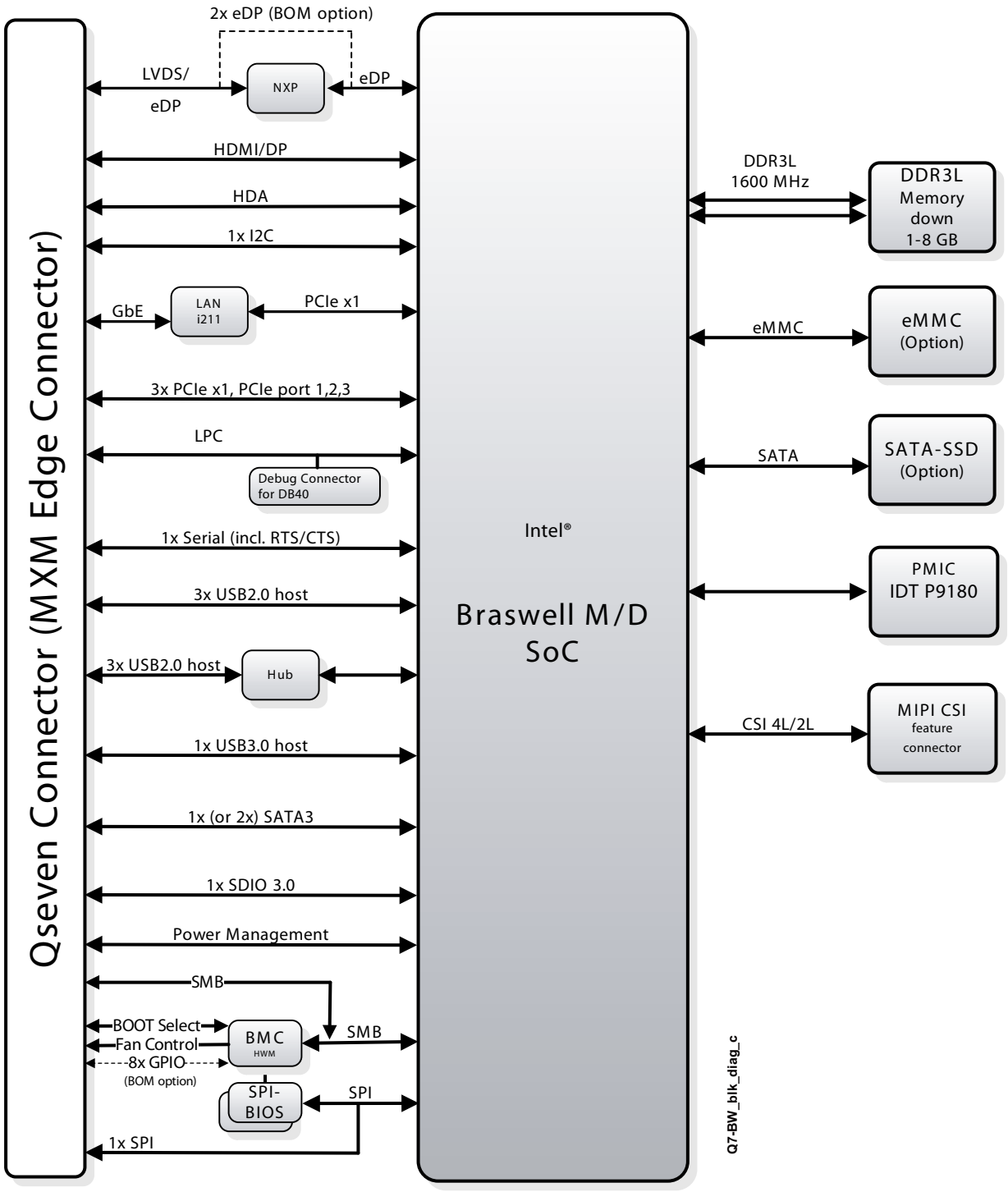


Figure 1-1: Module functional block diagram

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1.4 Specifications

1.4.1 Physical

Table 1-1 lists the physical dimensions of the module.

Table 1-1: Weight and Footprint Dimensions

Dimension	Measurement	
Weight	0.025 kg [0.09 kg with heat spreader]	Overall height is measured from the upper board surface to the top of the highest permanent component on the upper board surface. This measurement does not include the cooling solution.
Height (overall)	2.29mm	
Board thickness	1.27mm	
Width	70.00mm	
Length	70.00mm	

1.4.2 Electrical

Table 1-2 specifies the electrical characteristics of the module.

Table 1-2: Electrical Specifications

Parameter	Value
Voltage Input	
Modes	▶ AT and ATX (AT mode start controlled by BMC)
Standard	▶ +5V DC, +/-5%, =/- 50mV ripple
Standby	▶ +5V standby +/-5%, =/- 50mV ripple (only needed for suspend mode)
RTC	▶ 3.0V, 2.0V to 3.3V (battery), +/-20mV ripple
Power States	▶ C0, C1, C1E, C6C, C6, C7, S0, S3, S4, S5, S5 ECO mode (wake on USB S3/S4, WOL S3/S4/S5)
Power Management	▶ ACPI 5.0 compliant; smart battery support

1.4.3 Environmental

Table 1-3 defines the environmental conditions under which the module is qualified to operate and to be stored.

Table 1-3: Temperature, Humidity, and Pressure

Parameter	Temperature
Temperature	
Standard	▶ 0°C to +60°C
Storage	▶ -55°C to 85°C
Humidity	
Operating	▶ 5% to 90% relative humidity, non-condensing
Non-operating	▶ 5% to 95% relative humidity, non-condensing

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Table 1-4 provides shock and vibration tests performed on the board.

Table 1-4: Shock and Vibration

Parameter	Standard
Shock Test	MIL-STD-202F, Method 213B, Table 213-I, Condition A
Random Vibration Test	MIL-STD-202F, Method 214A, Table 214-I, Condition D

Table 1-5 presents the average times between system failures.

Table 1-5: Mean Time Between Failures

Parameter	Value
MTBF at 60°C, ground benign Bellcore	200,000 hrs (according to MIL calculation)

Table 1-6 presents the EMI test standard performed on the board.

Table 1-6: EMI Testing

Parameter	Standard
EMI	EN55022 & 24 Class A

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1.4.4 Mechanical

Figure 1-2 provides the mechanical dimensions of the Q7-BW.

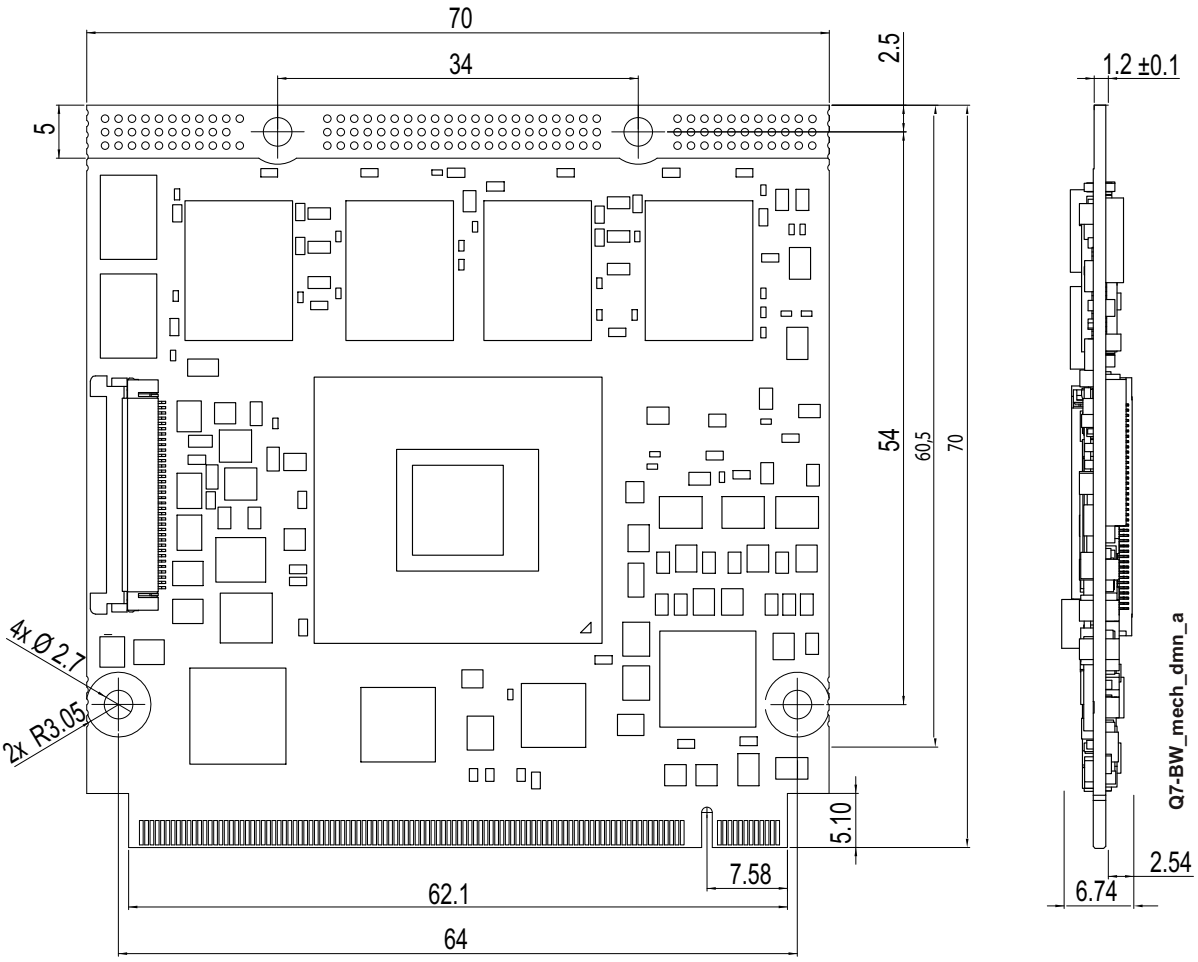


Figure 1-2: Mechanical dimensions (top side)

NOTE:

ADLINK strongly recommends plastic spacers instead of metal spacers for mounting the board. Metal spacers create the possibilities of short circuits with the components located around the mounting holes, which can ruin the board.

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1.4.5 Power

Table 1-7 Provides power consumption values for the module under certain load configurations.

Table 1-7: Power Supply Requirements

Parameter	6W, N3710 SoC with 4GB SDRAM, 2M cache up to 2.56 GHz	6W, N3160 SoC with 4GB SDRAM, 2M cache up to 2.24 GHz	6W, N3060 SoC with 2GB SDRAM, 2M cache up to 2.48 GHz	4W, N3010 SoC with 2GB SDRAM, 2M cache up to 2.24 GHz	5W, x5-E8000 Atom SoC with 4GB SDRAM, 2M cache up to 2.00 GHz
Input Type	Regulated DC voltage	Regulated DC voltage	Regulated DC voltage	Regulated DC voltage	Regulated DC voltage
Typical Idle Current and Power (EIST enabled; 500GB SSD; 8GB eMMC; under Windows 7)	0.52A (2.60W) @ 5V	0.52A (2.60W) @ 5V	0.46A (2.30W) @ 5V	0.48A (2.40W) @ 5V	0.52A (2.60W) @ 5V
Typical Operating Mode Current and Power (EIST enabled; 500GB SSD; 8GB eMMC; under Windows 7)	1.60A (8.00W) @ 5V	1.43A (7.15W) @ 5V	1.00A (5.00W) @ 5V	0.93A (4.65W) @ 5V	1.35A (6.75W) @ 5V
Maximum Operating Mode Current and Power (EIST enabled; 500GB SSD; 8GB eMMC; under Windows 7; Intel TAT tool v5.0.1022)	5.01A (25.50W) @ 5V	3.48A (17.40W) @ 5V	2.60A (13.00W) @ 5V	2.41A (12.05W) @ 5V	2.23A (11.15W) @ 5V
System S3 mode (EIST enabled; 500GB SSD; 8GB eMMC; under Windows 7)	0.17A (0.85W) @ 5VSB	0.17A (0.85W) @ 5VSB	0.16A (0.80W) @ 5VSB	0.17A (0.85W) @ 5VSB	0.17A (0.85W) @ 5VSB
System S4 mode (EIST enabled; 500GB SSD; 8GB eMMC; under Windows 7)	0.16A (0.80W) @ 5VSB	0.16A (0.80W) @ 5VSB	0.15A (0.75W) @ 5VSB	0.16A (0.80W) @ 5VSB	0.16A (0.80W) @ 5VSB
System S5 mode with ECO enabled (EIST enabled; 500GB SSD; 8GB eMMC; under Windows 7)	0.16A (0.80W) @ 5VSB	0.16A (0.80W) @ 5VSB	0.15A (0.75W) @ 5VSB	0.16A (0.80W) @ 5VSB	0.16A (0.80W) @ 5VSB

1.4.6 Cooling

The Q7-BW is designed to operate at its maximum CPU speeds and requires a thermal solution to cool the SoC. ADLINK offers a heat spreader as one part of the cooling solution and a passive heatsink (separate order numbers) for cooling. The heatsink can be used for module evaluation. If a custom heatsink is used, it is recommended to connect it to the ADLINK heat spreader. This facilitates future module upgrades without the need to re-design the custom heatsink.

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1.5 Getting Started

Mount the Q7-BW to the carrier as illustrated in Figure 1-3, which provides a profile view of the module mounted to the carrier with dimensions.

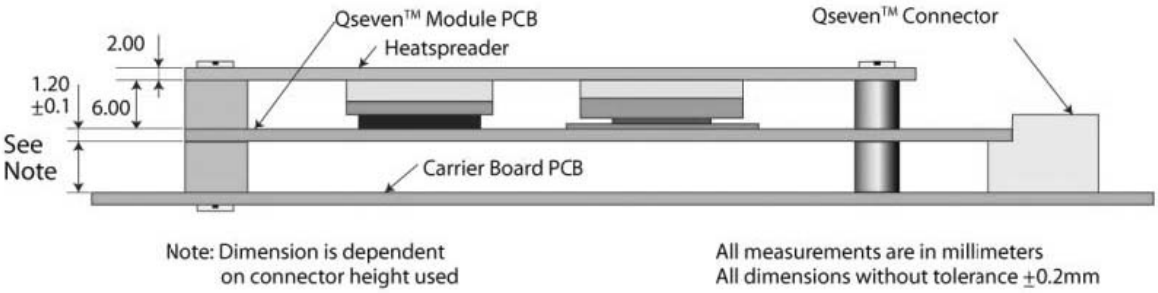


Figure 1-3: Qseven module mounting dimensions (profile)

NOTE:

ADLINK strongly recommends plastic spacers instead of metal spacers for mounting the board. Metal spacers create the possibilities of short circuits with the components located around the mounting holes, which can ruin the board.

CAUTION:

Be sure to observe the EMC security measures. Make sure you are always at the same potential as the module.

CAUTION:

Never connect or disconnect peripherals like HDDs while the power supply is connected and switched on.

Use a commercial, high-quality display cable to connect an HDMI display. Connect a USB keyboard or mouse to the carrier. Use the SATA cable to connect the hard disk. Make sure that the pins match their counterparts correctly and are not twisted. If you plan to use additional peripherals, connect them to the appropriate headers or connectors on the carrier.

Connect a power supply to the power connector on the carrier and switch on the power.

NOTE:

Observe the minimum voltage values for the standard peripherals mentioned. For additional peripherals, make sure enough power is available. The system will not work if there is not enough supply current for all your devices.

The display shows the BIOS messages. If you want to change the standard BIOS settings, press the <DEL> key to enter the BIOS setup menus. See Chapter 4 for setup details.

If you need to load the BIOS default values, they can be automatically loaded at boot time.

The Q7-BW boots from CD drives, USB sticks, hard disks, or µSD-Cards. Provided that any of these is connected and contains a valid operating system image, the display then shows the boot screen of your operating system.

The Q7-BW needs adequate cooling measures depending on the desired operating temperature range. Using the board without cooling could damage the board permanently.

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2 Hardware

This chapter describes the major integrated circuits (ICs) and interface connectors and headers on the module. The third section of this chapter further describes the major ICs, including web links to the chip manufacturers' data sheets.

2.1 Major Components (ICs)

Table 2-1 lists the major integrated circuits on the Q7-BW, including a brief description of each IC. Figure 2-1 and Figure 2-2 show the locations of the major ICs.

Table 2-1: Major Integrated Circuit Descriptions and Functions

Chip Type	Mfg.	Model	Description	Function
CPU (U1)	Intel	• N3710 Pentium (quad-core, 6W, 2.56GHz burst frequency) • N3160 Celeron (quad-core, 6W, 2.24GHz burst frequency) • N3060 Celeron (dual-core, 6W, 2.48GHz burst frequency) • N3010 Celeron (dual-core, 6W, 2.24GHz burst frequency) • x5-E8000 Atom, (quad-core, 5W, 2.00GHz burst frequency)	N3000 series, 14nm SoC (System on Chip) with Intel Architecture	Integrates Processor Core, Graphics/ Memory Hub, and I/ O Hub
Gigabit Ethernet (GbE) Controller (LU1 on bottom side; see Figure 2-2)	Intel	WGI211AT SLJXZ	Single-port Gigabit Ethernet controller	Integrates GbE MAC, PHY, and MDI for standard 10T/ 100TX/1000T Ethernet signals using the PCIe x1 bus
BMC [Board Management Controller] (BU1)	Texas Instruments	TM4C123BH6ZRB	Micro controller for board functions including Watchdog Timer, LVDS control, system control, and failure protection	Controls dual BIOS and SEMA API through the SMBus bus
SPI Flash [BIOS] (U2704 and U2705)	Macronix	MX25L6433FM2I-08G	Serial Peripheral Interface Flash Memory chip (for firmware)	Stores BIOS 0 and BIOS 1 in Flash Memory
USB 2.0 Hub Controller (U3101)	Microchip	USB2514BI-AEZG	Multi Transaction Translator (MTT)	Provides downstream ports for embedded USB 2.0 solutions with battery charging support on individual ports

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Table 2-1: Major Integrated Circuit Descriptions and Functions (Continued)

Embedded DisplayPort-to-LVDS Converter (GBU1)	NXP	PTN3460	Embedded DisplayPort (eDP) to LVDS bridge device that enables connectivity between an embedded DisplayPort (eDP) source and an LVDS display panel.	Processes the incoming embedded DisplayPort (eDP) stream, performs eDP to LVDS protocol conversion, and transmits processed stream in LVDS format.
DDR3L SDRAM (MD1602, MD1604, MD1702, MD1704, [MD1601, MD1603, MD1701, MD1703 on bottom side; see Figure 2-2])	Micron	• MT41K128M16 (1GB board model) • MT41K128M16 (2GB board model) • MT41K256M16 (2GB board model) • MT41K512M16 (4GB board model) • MT41K256M16 (4GB board model) • MT41K512M16 (8GB board model)	On-board DDR3L, 1.35V, non-ECC system memory • 4Gb, 4x 128Mx16 • 4Gb, 8x 128Mx16 • 4Gb, 4x 256Mx16 • 4Gb, 4x 512Mx16 • 4Gb, 8x 256Mx16 • 4Gb, 8x 512Mx16	Provides high-speed data transfer
PMIC (PU68)	IDT (Integrated Device Technology)	P9180	Multiple-channel power management IC	Supports power management requirements of 14nm processors
eMMC, NAND Flash (U2901 on bottom side; see Figure 2-2) [**Optional]**	Micron	MTFC8GLDEA-4M-IT	MultiMediaCard Controller and NAND Flash Memory up to 64GB	Provides communication and mass data storage capabilities
SATA NAND SSD (U3001 on bottom side; see Figure 2-2) [**Optional**]	Greenliant	GLS85LS1008	Industrial-grade soldered solid-state storage module	Provides up to 8GB solid state storage through standard SATA protocol

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Key:
U1 - CPU
U2704 - BIOS 0
U2705 - BIOS 1
U3101 - USB Hub Controller
BU1 - BMC
GBU1 - eDP-to-LVDS Converter
MD1602 - DDR3L SDRAM
MD1604 - DDR3L SDRAM
MD1702 - DDR3L SDRAM
MD1704 - DDR3L SDRAM
PU68 - PMIC

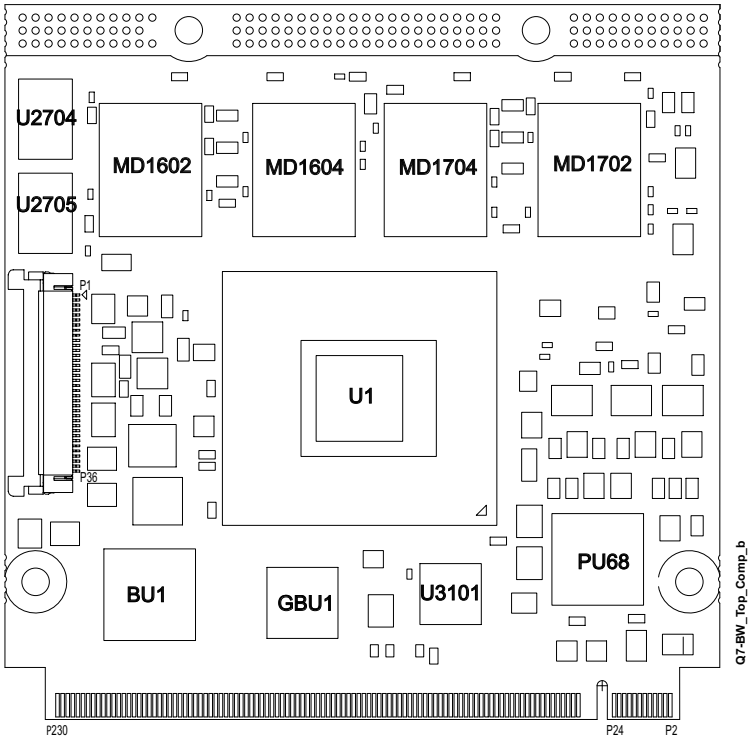


Figure 2-1: Component Locations (Top Side)

Key:
U2901 - eMMC NAND Flash
U3001 - SSD
LU1 - GbE Controller
MD1601 - DDR3L SDRAM
MD1603 - DDR3L SDRAM
MD1701 - DDR3L SDRAM
MD1703 - DDR3L SDRAM

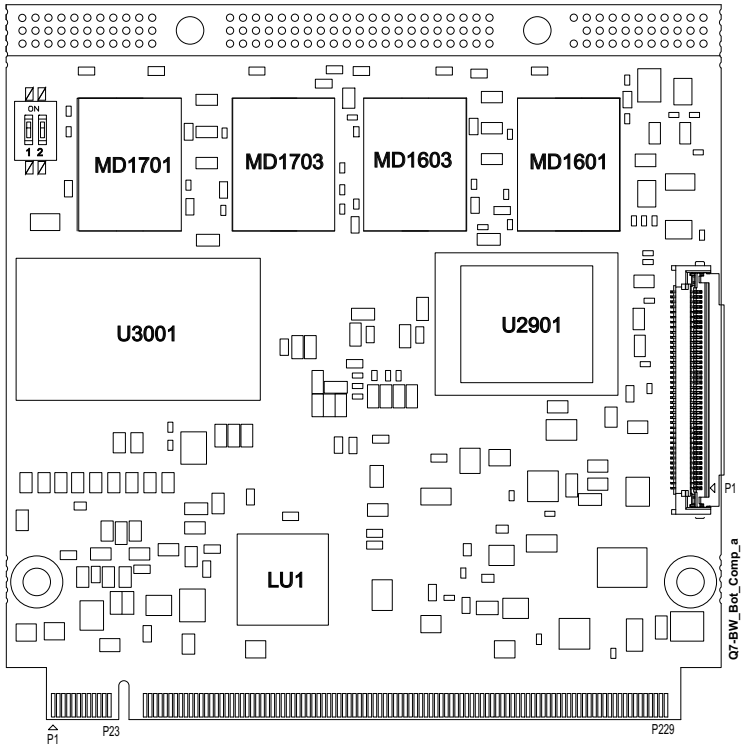


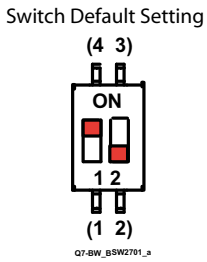
Figure 2-2: Component Locations (Bottom Side)

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2.2 Connectors, Switches, and LEDs

Table 2-2 describes the connectors, switches, and LEDs shown in Figure 2-3 and Figure 2-4.

Table 2-2: Module Connector Description

Connector#	Board Access	Description
CN2701	Bottom	40-pin, DB40 Front-Flip connector for debug card (Molex, 502790-4091)
CN3001	Top	36-pin, board-to-FPC connector for MIPI camera interface (Hirose, FH12A-36S-0.5SH(55)
GF1 - Q7 (Top and Bottom)	Top/ Bottom	230-pin, MXM edge connector for I/O functions
BLED1	Top	Blue LED indicating system status activities for HW Reset, SW Reset, Power Up, Power Down, Reset Button, and Power Button
BLED2	Top	Green LED for Power On
BSW2701	Bottom	4-pin dip switch for • Setting BIOS Boot (1=Boot from SPI1, 4=Boot from SPI0 [default]) • Selecting BIOS Mode (2=Failsafe BIOS [default], 3=Normal BIOS) 

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Key:
CN3001 - MIPI Camera
BLED1 - LED, System Status (Blue)
BLED2 - LED, Power On (Green)
GF1 (Top) - Q7 MXM (Top)

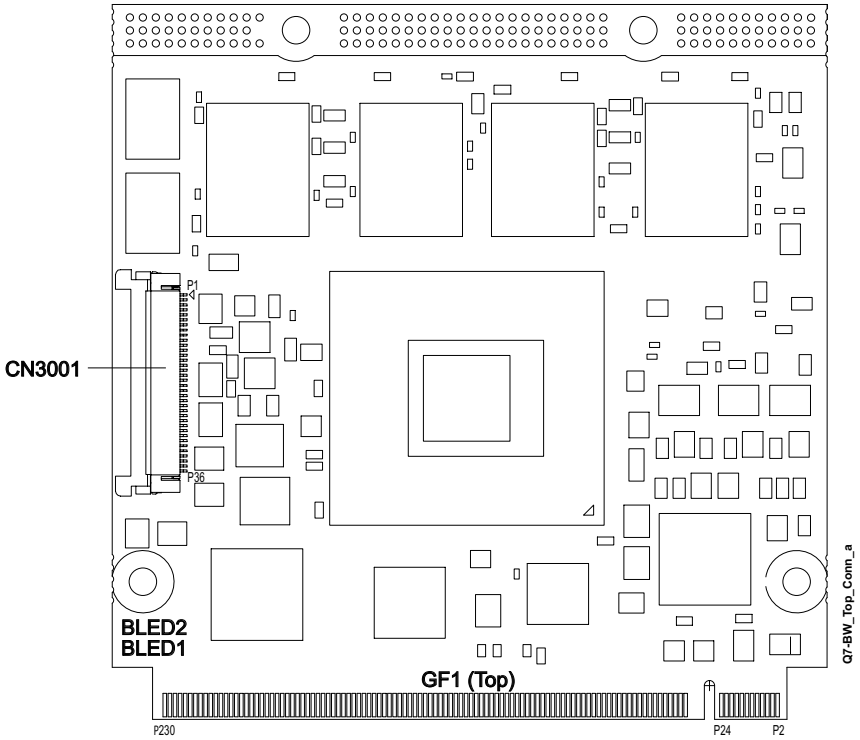


Figure 2-3: Connector Locations (Top Side)

Key:
CN2701 - DB40 Debug
BSW2701 - BIOS Select
GF1 (Bottom) - Q7 MXM (Bottom)

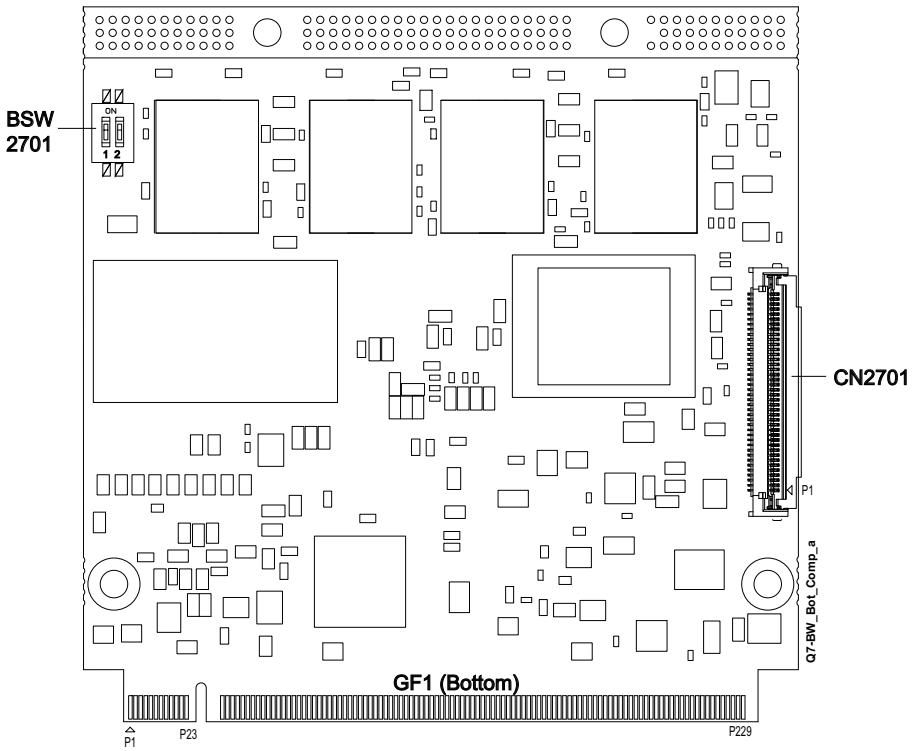


Figure 2-4: Connector Locations (Bottom Side)

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2.3 Component Features

This section further describes the supported features of the Q7-BW major on-board components.

2.3.1 CPU

The Q7-BW product family offers the following versions of the Intel Pentium and Celeron N3000 Series CPU, System-on-Chip (SoC): the N3710 Pentium (Quad Core with Gfx 700MHz), the N3160 Celeron (Quad Core with Gfx 640MHz), the N3060 Celeron (Dual Core with Gfx 600MHz), and the N3010 Celeron (Dual Core with Gfx 600MHz). The Q7-BW product family also includes a lower-cost alternative: the x5-E8000 Atom with Gfx 320MHz. N3000 Series CPUs feature the Intel Architecture and are manufactured based on Intel's 14-nanometer technology. N-series SoC data sheet at the Intel website. Other CPU SKUs are available on request.

2.3.2 I211 LAN Controller

The Intel I211 provides a single-port controller that supports GbE functionality using the high-speed PCIe standard, v2.1 (2.5GT/s). The I211 features an integrated PHY, which enables 1000BASE-T implementations such as rack-mounted or pedestal servers in add-on NIC or LAN-on-Motherboard (LOM) designs. Other implementations include blade servers such as LOMs or mezzanine cards as well as embedded applications such as switch add-on cards and network appliances. Refer to the Intel I211 Ethernet Controller data sheet at the Intel website.

2.3.3 PTN3460i eDP-to-LVDS Converter

The PTN3460i supports single-bus or dual-bus LVDS signalling with color depths of 18 bits per pixel or 24 bits per pixel and pixel clock frequency up to 112MHz. The LVDS data packing can be done either in VESA or JEIDA formats. Also, the DP AUX interface transports I@C-over-AUX commands and support EDID-DDC communication with LVDS panel. To support panels without EDID ROM, the PTN3460 can emulate EDID ROM behavior, avoiding specific changes in system video BIOS.

2.3.4 Memory

The Q7-BW employs up to two channels of 64-bit DDR3L on-board memory. Up to eight SDRAM memory chips provide up to 8GB of low-voltage non-ECC, unbuffered system memory. Two channels are used with an eight chip configuration. Only one channel is used with a four chip configuration. Refer to the SDRAM data sheet at the Micron website.

Depending on the SDRAM chips featured on the module, the following total SDRAM capacities are supported:

- 4x 128M16 = 1 GB
- 8x 128M16 = 2 GB
- 4x 256M16 = 2 GB
- 4x 512M16 = 4 GB
- 8x 256M16 = 4 GB
- 8x 512M16 = 8 GB

2.3.5 eMMC NAND Flash

The module supports an optional, on-board eMMC (Multi-Media Card) NAND chip with capacities options from 4GB to 64GB. Refer to the MTFC8GLDEA-4M-IT NAND Flash data sheet at the Micron website.

2.3.6 SATA SSD (Solid State Drive)

The Q7-BW supports an optional SATA SSD (standard size, 8GB), soldered directly to the board. For more information, refer to the SSD datasheet at the Greenliant web site.

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2.3.7 SMBus Slave Addresses

Figure 2-3 lists the corresponding slave addresses of the devices on the SMBus.

Table 2-3: SMBus Slave Addresses

Address (HEX)	Function	Device
(50)	BMC/SEMA	BMC
(C0)	eDP to LVDS	PTN3460i
(92)	Thermal Sensor	LM73

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3 Interfaces

This section provides descriptions of the interfaces and signals within the Qseven connector. Refer to the Qseven specification at: http://www.sget.org/standards/qseven.html for definitions of the Qseven interfaces. The Qseven connector provides the following interfaces:

- LVDS
- HDMI
- Audio
- PCI Express (PCIe)
- Gb Ethernet
- USB 2.0
- USB 3.0
- SATA
- I2C
- SPI
- LPC
- Serial UART
- SD/SDIO
- eMMC
- LPC Debug
- MIPI CSI Camera



ADLINK Technology, Inc. only supports the features/ options tested and listed in this manual. The main chips used in the Q7-BW may provide more features or options than are listed for the Q7-BW, but some of these features or options are not supported on the module and will not function as specified in the chip documentation.

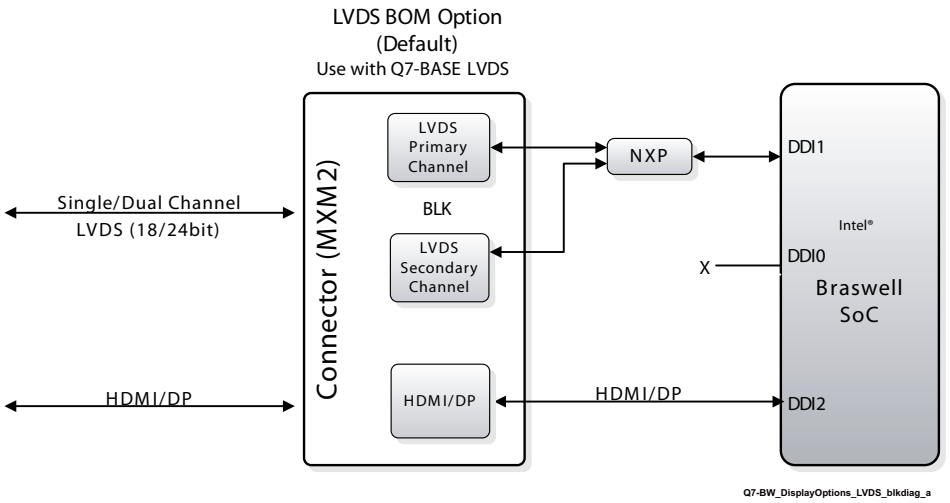
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3.1 Display Interfaces

The Q7-BW provides LVDS, eDP, and HDMI/DP display interfaces. Section 3.1.1 and Section 3.1.2 describe the two basic display configurations supported as separate BOM options. Sections 3.1.3 - 3.1.6 provide detailed descriptions of each display interface.

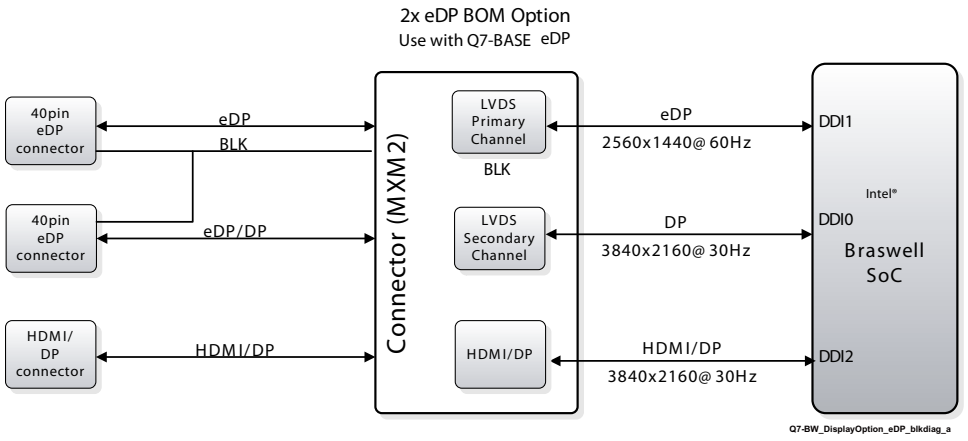
3.1.1 Default BOM Option

- 1x LVDS (single/dual channel, 18/24bit) through the eDP-to-LVDS converter
- 1x HDMI/DP
- Requires Q7-BASE LVDS carrier



3.1.2 Alternative BOM Option

- 1x eDP
- 1x DP
- 1x HDMI/DP
- Requires Q7-BASE eDP carrier



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3.1.3 LVDS (18/24-Bit LCD) from DDI1

The default configuration of the LVDS interface originates from the DDI1 port of the CPU, and a translation is made from embedded DisplayPort signals to LVDS signals by an eDP-to-LVDS converter. The standard interface supports two LVDS channels on the Qseven connector with resolutions up to 1920x1200 at 60Hz for 18/24-bit color depth. This configuration requires the Q7-BASE LVDS carrier. Refer to the NXP PTN3460, embedded DisplayPort-to-LVDS converter datasheet for more information on the signal translation.

3.1.4 HDMI or Display Port (DP) from DDI2

Both default and optional configurations, shown in sections 3.1.1 and 3.1.2, define the DDI2 port as HDMI (TMDS) or DP and provide the following features:

- 1 Clock pair
- 3 Data pairs
- Service signals
- HDMI resolutions up to 3840x2160 at 30Hz or 2560x1600 at 60Hz
- DP resolutions up to 3840x2160 at 30Hz or 2560x1600 at 60Hz
- Both Q7-BASE LVDS and Q7-BASE eDP carriers support this configuration
- The HDMI interface is compliant with the HDMI 1.4 specification.

3.1.5 eDP (embedded DisplayPort) from DDI1

When the NXP converter is removed, the Q7-BW supports the optional configuration (separate model order number) of one embedded DisplayPort (eDP) interface originating from DDI1 port of the CPU. The signals are routed through the primary and secondary LVDS pins on the Qseven connector, as shown in the previous diagram. The eDP interface supports the following features.

- eDP resolutions up to 2560x1140 at 60Hz
- This configuration requires the Q7-BASE eDP carrier

3.1.6 DP (DisplayPort) from DDI0

When the NXP converter is removed, the Q7-BW supports the optional configuration (separate model order number) of one DisplayPort (DP) interface originating from DDI0 port of the CPU. The signals are routed through the secondary LVDS pins on the Qseven connector, as shown in the previous diagram. The eDP interface supports the following features.

- DP resolutions up to 3840x2160 at 30Hz or 2560x1600 at 60Hz
- This configuration requires the Q7-BASE eDP carrier

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3.2 Audio (HDA)

The CPU provides an HDA controller, which communicates with internal or external CODECs over the Intel HDA serial link. HDA signals are brought out through pins 59, 61, 63, 65, 67 on the Qseven connector.



One audio link can be routed through the DDI1 interface and one link can be routed to the audio CODEC on the base board. Consequently, audio over DisplayPort/HDMI and the use of an audio CODEC can be implemented at the same time.

3.3 PCI Express (PCIe)

The CPU features four PCIe x1 ports, and the Q7-BW module uses three of them for the PCIe interface and one of them for the Gigabit Ethernet interface. The PCIe interface supports the PCIe Base Specification 2.0 with a maximum signal rate of 5 GT/s and can be configured to support PCIe edge cards or Express Cards.

3.4 Gigabit Ethernet

The on-board Intel I211IT Ethernet controller uses PCIe x1 (v2.1) bus signals from the CPU to enable 10T/100TX/1000T operation through integrated MAC, PHY, and MDI interfaces.

3.5 USB Ports

The USB interface provides six USB 2.0 host ports and one USB 3.0 host port.

3.6 SATA

The SATA interface provides two ports through the SATA0 and SATA1 pins on the Q7-BW connector. The interface supports up to 6Gb/s. The SATA1 port is shared with the on-board SSD option and is not available on the Qseven connector if the board provides the SSD option.

3.7 I2C Bus

The Q7-BW provides one interface through the I2C bus for General Purpose with operating speeds up to 400kHz. All I2C interfaces have 3.3V pull ups with 2.2k resistors.

3.8 SPI

The Q7-BW supports one SPI controller, which supports two SPI Flash devices on the module for BIOS storage, up to 16MB each. Additional SPI signals are routed to the DB40 debug connector and to the MXM2 SPI pins.

3.9 LPC (Low Pin Count)

The LPC interface is a cost-efficient, low-speed interface designed to support low-speed legacy devices such as a Super I/O controller or a firmware hub device.

3.10 Serial (UART)

The Q7-BW provides one serial interface: one high-speed, 4-wire port with TX/RX and RTS#/CTS# signals.

3.11 SD/SDIO Interface

Four parallel data lines and six function signals comprise the SD/SDIO interface, supporting SD Card sockets.

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3.12 eMMC Interface

The Q7-BW provides one 8-bit eMMC interface port, brought out from the CPU through the SDIO pins on the Qseven connector. If the optional eMMC NAND chip is present on the module, the eMMC interface will not be available for the baseboard on the Qseven connector.

3.13 Debug Interface

A 40-pin, front flip, DB40 connector allows access to the system to debug and update the BIOS, BMC, and OS code. (Refer to “Debug (DB40) Connector Signals” on page 28.)

3.14 MIPI CSI Camera Interface

A 36-pin, board-to-FPC connector provides signals for two MIPI CSI camera devices (one 2-lane and one 4-lane) supporting up to 800 Mbit/s of actual pixels. (Refer to “MIPI CSI Camera Connector Signals” on page 29.)

3.15 Qseven Interface Signals

Table 3-1 provides the pin signals for the Qseven connector. Refer to the Qseven specification at http://www.sget.org/standards/qseven.html for definitions of the Qseven signals.

Table 3-1: Q7 Interface (GF1) Signal Descriptions

Pin #	Bottom Side	Pin #	Top Side
1	GND	2	GND
3	GBE_MDI3- (Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/ sec Gigabit Ethernet mode.)	4	GBE_MDI2- (Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/ sec Gigabit Ethernet mode.)
5	GBE_MDI3+ (Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/ sec Gigabit Ethernet mode.)	6	GBE_MDI2+ (Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/ sec Gigabit Ethernet mode.)
7	GBE_LINK100# (Ethernet controller 0 100Mbit/sec link indicator, active low.)	8	GBE_LINK1000# (Ethernet controller 0 1000Mbit/sec link indicator, active low.)
9	GBE_MDI1- (Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.)	10	GBE_MDI0- (Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.)
11	GBE_MDI1+ (Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.)	12	GBE_MDI0+ (Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.)
13	GBE_LINK# (Ethernet controller 0 link indicator, active low.)	14	GBE_ACT# (Ethernet controller 0 activity indicator, active low.)

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Table 3-1: Q7 Interface (GF1) Signal Descriptions (Continued)

15	GBE_CTREF (Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less.)	16	SUS_S5# (S5 State: This signal indicates S4 or S5 (Soft Off) state.)
17	WAKE# (External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.)	18	SUS_S3# (S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.)
19	SUS_STAT# (Suspend Status: indicates that the system will be entering a low power state soon.)	20	PWRBTN# (Power Button: Low active power button input. This signal is triggered on the falling edge.)
21	SLP_BTN# (Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.)	22	LID_BTN# (LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. Open/ Close state may be software configurable.)
23	GND	24	GND
	KEY		KEY
25	GND	26	PWGIN (High active input for the Qseven module indicates that all power rails located on the carrier board are ready for use.)
27	BATLOW# (Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.)	28	RSTBTN# (Reset button input. This input may be driven active low by an external circuitry to reset the Qseven module.)
29	SATA0_TX+ (Serial ATA channel 0, Transmit Output differential pair.)	30	SATA1_TX+ (Serial ATA channel 1, Transmit Output differential pair; not available if optional SATA SSD is installed)
31	SATA0_TX- (Serial ATA channel 0, Transmit Output differential pair.)	32	SATA1_TX- (Serial ATA channel 1, Transmit Output differential pair; not available if optional SATA SSD is installed)
33	SATA_ACT# (Serial ATA Led. Open collector output pin driven during SATA command activity.)	34	GND
35	SATA0_RX+ (Serial ATA channel 0, Receive Input differential pair.)	36	SATA1_RX+ (Serial ATA channel 1, Receive Input differential pair; not available if optional SATA SSD is installed)
37	SATA0_RX- (Serial ATA channel 0, Receive Input differential pair.)	38	SATA1_RX- (Serial ATA channel 1, Receive Input differential pair; not available if optional SATA SSD is installed)
39	GND	40	GND

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Table 3-1: Q7 Interface (GF1) Signal Descriptions (Continued)

41	BIOS_DISABLE# (Module BIOS disable input signal. Pull low to disable module's on-board BIOS. Allows off-module BIOS implementations.)	42	SDIO_CLK# (SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.)
43	SDIO_CD# (SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.)	44	SDIO_LED (SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.)
45	SDIO_CMD (SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.)	46	SDIO_WP (SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.)
47	SDIO_PWR# (SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.)	48	SDIO_DAT1 (These signals operate in push-pull mode.)
49	SDIO_DAT0 (These signals operate in push-pull mode.)	50	SDIO_DAT3 (These signals operate in push-pull mode.)
51	SDIO_DAT2 (These signals operate in push-pull mode.)	52	Not Connected
53	Not Connected	54	Not Connected
55	Not Connected	56	Not Connected
57	GND	58	GND
59	HDA_SYNC (Serial Bus Audio Synchronization.)	60	SMB_CLK (Clock line of System Management Bus.)
61	HDA_RST# (HD Audio/AC'97 Codec Reset.)	62	SMB_DAT (Data line of System Management Bus.)
63	HDA_BITCLK (HD Audio/AC'97 24 MHz Serial Bit Clock from Codec.)	64	SMB_ALERT# (System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.)
65	HDA_SDI (HD Audio/AC'97 Serial Data Input from Codec.)	66	GP0_I2C_CLK (General Purpose I²C bus #0 clock line.)
67	HDA_SDO (HD Audio/AC'97 Serial Data Output to Codec.)	68	GP0_I2C_DAT (General Purpose I²C bus #0 data line.)
69	THRM# (Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.)	70	WDTRIG# (Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven module on the falling edge of a low active pulse.)
71	THRMTRIP# (Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active, the system immediately transitions to the S5 State [Soft Off].)	72	WDOUT (Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.)
73	GND	74	GND
75	USB_SSTX0- [USB 3.0] (Multiplexed with transmit signal differential pairs for the Superspeed USB data path.)	76	USB_SSRX0- [USB 3.0] (Receive signal differential pairs for the Superspeed USB data path.)
77	USB_SSTX0+ [USB 3.0] (Multiplexed with transmit signal differential pairs for the Superspeed USB data path.)	78	USB_SSRX0+ [USB 3.0] (Receive signal differential pairs for the Superspeed USB data path.)
79	USB_6_7_OC# (Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.)	80	USB_4_5_OC# (Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.)

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Table 3-1: Q7 Interface (GF1) Signal Descriptions (Continued)

81	USB_P5- (Universal Serial Bus Port 5 differential pair.)	82	USB_P4- (Universal Serial Bus Port 4 differential pair.)
83	USB_P5+ (Universal Serial Bus Port 5 differential pair.)	84	USB_P4+ (Universal Serial Bus Port 4 differential pair.)
85	USB_2_3_OC# (Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.)	86	USB_0_1_OC# (Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.)
87	USB_P3- (Universal Serial Bus Port 3 differential pair.)	88	USB_P2- (Universal Serial Bus Port 2 differential pair.)
89	USB_P3+ (Universal Serial Bus Port 3 differential pair.)	90	USB_P2+ (Universal Serial Bus Port 2 differential pair.)
91	USB_CC (USB Client Connect pin. If USB Port 1 is configured for client mode, then an externally connected USB host should set this signal to high-active in order to properly make the connection with the module's internal USB client controller. If the external USB host is disconnected, this signal should be set to low-active in order to inform the USB client controller that the external host has been disconnected. A level shifter/ protection circuitry should be implemented on.)	92	USB_ID (USB ID pin. Configures the mode of the USB Port 1. If the signal is detected as being 'high active' the BIOS will automatically configure USB Port 1 as USB Client and enable USB Client support. This signal should be driven as OC signal by external circuitry.)
93	USB_P1- (Universal Serial Bus Port 1 differential pair. This port may be optionally used as USB client port.)	94	USB_P0- (Universal Serial Bus Port 0 differential pair.)
95	USB_P1+ (Universal Serial Bus Port 1 differential pair. This port may be optionally used as USB client port.)	96	USB_P0+ (Universal Serial Bus Port 0 differential pair.)
97	GND	98	GND
99	LVDS_A0+ (LVDS primary channel differential pair 0.	100	LVDS_B0+ (LVDS secondary channel differential pair 0.)
101	LVDS_A0- (LVDS primary channel differential pair 0.	102	LVDS_B0- (LVDS secondary channel differential pair 0.)
103	LVDS_A1+ (LVDS primary channel differential pair 1.	104	LVDS_B1+ (LVDS secondary channel differential pair 1.)
105	LVDS_A1- (LVDS primary channel differential pair 1.	106	LVDS_B1- (LVDS secondary channel differential pair 1.)
107	LVDS_A2+ (LVDS primary channel differential pair 2.	108	LVDS_B2+ (LVDS secondary channel differential pair 2.)
109	LVDS_A2- (LVDS primary channel differential pair 2.	110	LVDS_B2- (LVDS secondary channel differential pair 2.)
111	LVDS_PPEN (Controls panel power enable.)	112	LVDS_BLEN (Controls panel backlight enable.)
113	LVDS_A3+ (LVDS primary channel differential pair 3.	114	LVDS_B3+ (LVDS secondary channel differential pair 3.)
115	LVDS_A3- (LVDS primary channel differential pair 3.	116	LVDS_B3- (LVDS secondary channel differential pair 3.)
117	GND	118	GND
119	LVDS_A_CLK+ (LVDS primary channel differential pair clock lines.	120	LVDS_B_CLK+ (LVDS secondary channel differential pair clock lines.)

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Table 3-1: Q7 Interface (GF1) Signal Descriptions (Continued)

121	LVDS_A_CLK- (LVDS primary channel differential pair clock lines.	122	LVDS_B_CLK- (LVDS secondary channel differential pair clock lines.)
123	LVDS_BLT_CTRL (Primary functionality is to control the panel backlight brightness via pulse width modulation [PWM].)	124	GP_1-Wire_Bus (General Purpose 1-Wire bus interface. Can be used for consumer electronics control bus (CEC) of HDMI)
125	LVDS_DID_DAT (Primary functionality DisplayID DDC data line used for LVDS flat panel detection.)	126	LVDS_BLC_DAT (Control data signal for external SSC clock chip.)
127	LVDS_DID_CLK (Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection.)	128	LVDS_BLC_CLK (Control clock signal for external SSC clock chip.)
129	Not Connected	130	Not Connected
131	DP_LANE3+ / TMDS_CLK+ (DisplayPort differential pair lines lane 3, shared with TMDS differential pair clock lines.)	132	Not Connected
133	DP_LANE3- / TMDS_CLK- (DisplayPort differential pair lines lane 3, shared with TMDS differential pair clock lines.)	134	Not Connected
135	GND	136	GND
137	DP_LANE1+ / TMDS_LANE1+ (DisplayPort differential pair lines lane 1, shared with TMDS differential pair lines lane 1.)	138	DP_AUX+ (Auxiliary channel used for link management and device control. Differential pair lines.)
139	DP_LANE1- / TMDS_LANE1- (DisplayPort differential pair lines lane 1, shared with TMDS differential pair lines lane 1.)	140	DP_AUX- (Auxiliary channel used for link management and device control. Differential pair lines.)
141	GND	142	GND
143	DP_LANE2+ / TMDS_LANE0+ (DisplayPort differential pair lines lane 2, shared with TMDS differential pair lines lane 0.)	144	Not Connected
145	DP_LANE2- / TMDS_LANE0- (DisplayPort differential pair lines lane 2, shared with TMDS differential pair lines lane 0.)	146	Not Connected
147	GND	148	GND
149	DP_LANE0+ / TMDS_LANE2+ (DisplayPort differential pair lines lane 0, shared with TMDS differential pair lines lane 2.)	150	HDMI_CTRL_DAT (DDC based control signal [data] for HDMI device. ***Note:*** *Level shifters must be implemented* on the carrier board for this signal in order to be compliant with the HDMI Specification.)
151	DP_LANE0- / TMDS_LANE2- (DisplayPort differential pair lines lane 0, shared with TMDS differential pair lines lane 2.)	152	HDMI_CTRL_CLK (DDC based control signal [clock] for HDMI device. ***Note:*** *Level shifters must be implemented* on the carrier board for this signal in order to be compliant with the HDMI Specification.)
153	DP_HDMI_HPD# (Hot plug detection signal that serves as an interrupt request.)	154	RSVD

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Table 3-1: Q7 Interface (GF1) Signal Descriptions (Continued)

155	PCIE_CLK_REF+ (PCI Express Reference Clock for Lanes 0 to 3.)	156	PCIE_WAKE# (PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.)
157	PCIE_CLK_REF- (PCI Express Reference Clock for Lanes 0 to 3.)	158	PCIE_RST# (Reset Signal for external devices.)
159	GND	160	GND
161	Not connected	162	Not connected
163	Not connected	164	Not connected
165	GND	166	GND
167	PCIE2_TX+ (PCI Express channel 2, Transmit Output differential pair.)	168	PCIE2_RX+ (PCI Express channel 2, Receive Input differential pair.)
169	PCIE2_TX- (PCI Express channel 2, Transmit Output differential pair.)	170	PCIE2_RX- (PCI Express channel 2, Receive Input differential pair.)
171	UART0_TX (Serial Data Transmitter)	172	UART0_RTS# (Handshake signal, ready to receive data)
173	PCIE1_TX+ (PCI Express channel 1, Transmit Output differential pair.)	174	PCIE1_RX+ (PCI Express channel 1, Receive Input differential pair.)
175	PCIE1_TX- (PCI Express channel 1, Transmit Output differential pair.)	176	PCIE1_RX- (PCI Express channel 1, Receive Input differential pair.)
177	UART0_RX (Serial Data Receiver)	178	UART0_CTS# (Handshake signal, ready to send data)
179	PCIE0_TX+ (PCI Express channel 0, Transmit Output differential pair.)	180	PCIE0_RX+ (PCI Express channel 0, Receive Input differential pair.)
181	PCIE0_TX- (PCI Express channel 0, Transmit Output differential pair.)	182	PCIE0_RX- (PCI Express channel 0, Receive Input differential pair.)
183	GND	184	GND
185	LPC_AD0 (Command, Address and Data 0 signal.)	186	LPC_AD1 (Command, Address and Data 1 signal.)
187	LPC_AD2 (Command, Address and Data 2 signal.)	188	LPC_AD3 (Command, Address and Data 3 signal.)
189	LPC_CLK (LPC clock.)	190	LPC_FRAME# (LPC frame indicates the start of a new cycle or the termination of a broken cycle.)
191	SERIRQ (Serialized Interrupt.)	192	GPIO7 (General purpose input/output 7.)
193	VCC_RTC (3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. [VCC_RTC = 2.4 - 3.3 V].)	194	SPKR (Output for audio enunciator, the “speaker” in PC AT systems.)
195	FAN_TACHOIN (Fan tachometer input.)	196	FAN_PWMOUT (Fan speed control. Uses the Pulse Width Modulation [PWM] technique to control the Fan's RPM based on the CPU's die temperature.)
197	GND	198	GND
199	SPI_MOSI (Master serial output/Slave serial input signal. SPI serial output data from Qseven module to the SPI device.)	200	SPI_CS0# (SPI Chip Select 0 output.)
201	SPI_MISO (Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven module.)	202	SPI_CS1# (SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.)
203	SPI_SCK (SPI clock output.)	204	Not Connected
205	VCC_5V_SB (Standby Power Supply +5VDC ±5%.)	206	VCC_5V_SB (Standby Power Supply +5VDC ±5%.)

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Table 3-1: Q7 Interface (GF1) Signal Descriptions (Continued)

207	Not connected	208	Not connected
209	Not connected	210	Not connected
211	VCC (Power Supply +5VDC ±5%.)	212	VCC (Power Supply +5VDC ±5%.)
213	VCC (Power Supply +5VDC ±5%.)	214	VCC (Power Supply +5VDC ±5%.)
215	VCC (Power Supply +5VDC ±5%.)	216	VCC (Power Supply +5VDC ±5%.)
217	VCC (Power Supply +5VDC ±5%.)	218	VCC (Power Supply +5VDC ±5%.)
219	VCC (Power Supply +5VDC ±5%.)	220	VCC (Power Supply +5VDC ±5%.)
221	VCC (Power Supply +5VDC ±5%.)	222	VCC (Power Supply +5VDC ±5%.)
223	VCC (Power Supply +5VDC ±5%.)	224	VCC (Power Supply +5VDC ±5%.)
225	VCC (Power Supply +5VDC ±5%.)	226	VCC (Power Supply +5VDC ±5%.)
227	VCC (Power Supply +5VDC ±5%.)	228	VCC (Power Supply +5VDC ±5%.)
229	VCC (Power Supply +5VDC ±5%.)	230	VCC (Power Supply +5VDC ±5%.)

NOTE: The # symbol indicates the signal is Active Low.

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3.16 Debug (DB40) Connector Signals

Table 3-2 lists the pin signals of the CN2701 connector, which provides 40 pins, 1 row, consecutive sequence with 0.02" (0.50mm) pitch.

Table 3-2: Debug Interface Signals (CN2701)

Pin #	Interface	Signal
1	**NC**	RESVD
2	**For SMC Debug**	SMC_STATUS
3		BIOS_MODE
4		SEL_BIOS
5		POSTWDT_DIS#
6	**Test Point**	SUS_S5#
7		SUS_S4#
8		SUS_S3#
9		CB_PWROK
10		CB_RESET#
11		SYS_RESET#
12		PWRBTN#
13	**SMC Program Interface**	SMC_OCD0B
14		SMC_OCD0A
15		SMC_CLK
16		SMC_DATA
17		SMC_RESET_IN#
18		SMC_FLMD0
19		SMC_RXD6
20		SMC_TXD6
21		GND3
22		3V3_DUAL
23		3V3_SMC1
24	**LPC Debug Card Interface**	LPC_AD0
25		LPC_AD1
26		LPC_AD2
27		LPC_AD3
28		LPC_FRAME#
29		CLK33_LPC
30		RST#
31		BIOS_DIS0
32		GND2
33		LPC_3V3
34	**SPI Program Interface**	SPI_BIOS_CLK
35		SPI_BIOS_MOSI
36		SPI_BIOS_MISO
37		SPI_BIOS_CS1#
38		SPI_BIOS_CS0#
39		GND1
40		VCC_SPI_IN (SPI power input from flash tool to module)

NOTE: The gray table cells denote ground. The # symbol indicates the signal is Active Low.

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3.17 MIPI CSI Camera Connector Signals

Table 3-3 lists the pin signals of the CN3001 connector, which provides 36 pins, 1 row, consecutive sequence with 0.02" (0.50mm) pitch.

Table 3-3: MIPI CSI Camera Interface Signals (CN3001)

Pin #	Signal	Description
1	V3P3S	3.3 volts +/-5% to power the camera device (output)
2	V3P3S	3.3 volts +/-5% to power the camera device (output)
3	MCSI1_D0_P	CSI1 Camera 0 Data Lane 0+
4	MCSI1_D0_N	CSI1 Camera 0 Data Lane 0-
5	GND	Ground
6	MCSI1_D1_P	CSI1 Camera 0 Data Lane 1+
7	MCSI1_D1_N	CSI1 Camera 0 Data Lane 1-
8	GND	Ground
9	MCSI1_D2_P	CSI1 Camera 0 Data Lane 2+
10	MCSI1_D2_N	CSI1 Camera 0 Data Lane 2-
11	MCSI_CAM0RST#	Camera 0 Reset (active low; CMOS 1.8V; output)
12	MCSI1_D3_P	CSI1 Camera 0 Data Lane 3+
13	MCSI1_D3_N	CSI1 Camera 0 Data Lane 3-
14	GND	Ground
15	MCSI1_CLK_P	CSI1 Camera 0 Differential Clock+ (Strobe; D-PHY; input)
16	MCSI1_CLK_N	CSI1 Camera 0 Differential Clock- (Strobe; D-PHY; input)
17	GND	Ground
18	CN_I2C_CAM0_CK	Camera 0 Control Interface Clock (I2C-like interface; CMOS 1.8V OD; output)
19	CN_I2C_CAM0_DAT	Camera 0 Control Interface Data (I2C-like interface; CMOS 1.8V OD; input/output)
20	CAM0_ENA#	Camera 0 Enable (active low; CMOS 1.8V; output)
21	CAM_MCLK_R	Master Clock (may be used by cameras to drive internal PLL; frequency range: 6 - 27MHz; CMOS 1.8V; output)
22	CAM1_ENA#	Camera 1 Enable (active low; CMOS 1.8V OD; output)
23	CN_I2C_CAM1_CK	Camera 1 Control Interface Clock (I2C-like interface; CMOS 1.8V OD; input/output)
24	CN_I2C_CAM1_DAT	Camera 1 Control Interface Data (I2C-like interface; CMOS 1.8V OD; input/output)
25	GND	Ground
26	MCSI2_CLK_P	CSI2 Camera 1 Differential Clock+ (Strobe; D-PHY; input)
27	MCSI2_CLK_N	CSI2 Camera 1 Differential Clock- (Strobe; D-PHY; input)
28	GND	Ground
29	MCSI2_D0_P	CSI2 Camera 1 Data Lane 0+ (D-PHY; input)
30	MCSI2_D0_N	CSI2 Camera 1 Data Lane 0- (D-PHY; input)
31	MCSI_CAM1RST#	Camera 0 Reset (active low; CMOS 1.8V; output
32	MCSI2_D1_P	CSI2 Camera 1 Data Lane 1+ (D-PHY; input)
33	MCSI2_D1_N	CSI2 Camera 1 Data Lane 1- (D-PHY; input)
34	GND	
35	CAM0_GPIO	GPIO for Camera 0 (CMOS 1.8V; input/output)
36	CAM1_GPIO	GPIO for Camera 1 (CMOS 1.8V; input/output)

NOTE: The gray table cells denote ground or power. The # symbol indicates the signal is Active Low.

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4 Utilities

This chapter provides information on how to read information from and configure the BIOS Setup utility, the SEMA utility, the Watchdog Timer utility, and the board temperature sensors on the Q7-BW.

4.1 BIOS

The Q7-BW features an AMI BIOS. The default settings provide a “ready to run” system, even without a BIOS setup backup battery.

The BIOS is located in flash memory and can be easily updated with software under DOS.

All setup changes of the BIOS are stored in the CMOS RAM.

This section presents the five primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right hand column of the respective table.

Table 4-1: BIOS Setup Menu Structure

Main	Advanced	Security	Boot	Save & Exit
• System Information • Processor Information • VGA Firmware Version • Memory Information • SOC Information • System Management ► • System Date • System Time	• CPU► • Graphics► • Memory► • SATA► • USB► • Network ► • PCIe Configuration► • ACPI and Power Management► • Sound► • Serial Port Console► • Thermal► • Miscellaneous►	• Password Description► • Secure Boot Menu►	• Boot Configuration • CSM Configuration ►	• Reset Options ► • Save Options ►

Notes:
► indicates a submenu
Gray text indicates info only

4.1.1 Starting the BIOS Setup Utility

Use the following bullets to initiate start-up activity for the BIOS Setup Utility.

- ► Press <DEL> during power up to start the BIOS setup utility.
- ► Press <F11> during power up to start the Boot menu.
- ► Press <END> during power up to return BIOS settings to default.

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4.1.2 Main Menu

The Main Menu provides read-only information about your system and also allows you to set the System Date and Time. Refer to the tables below for details of the submenus and settings.

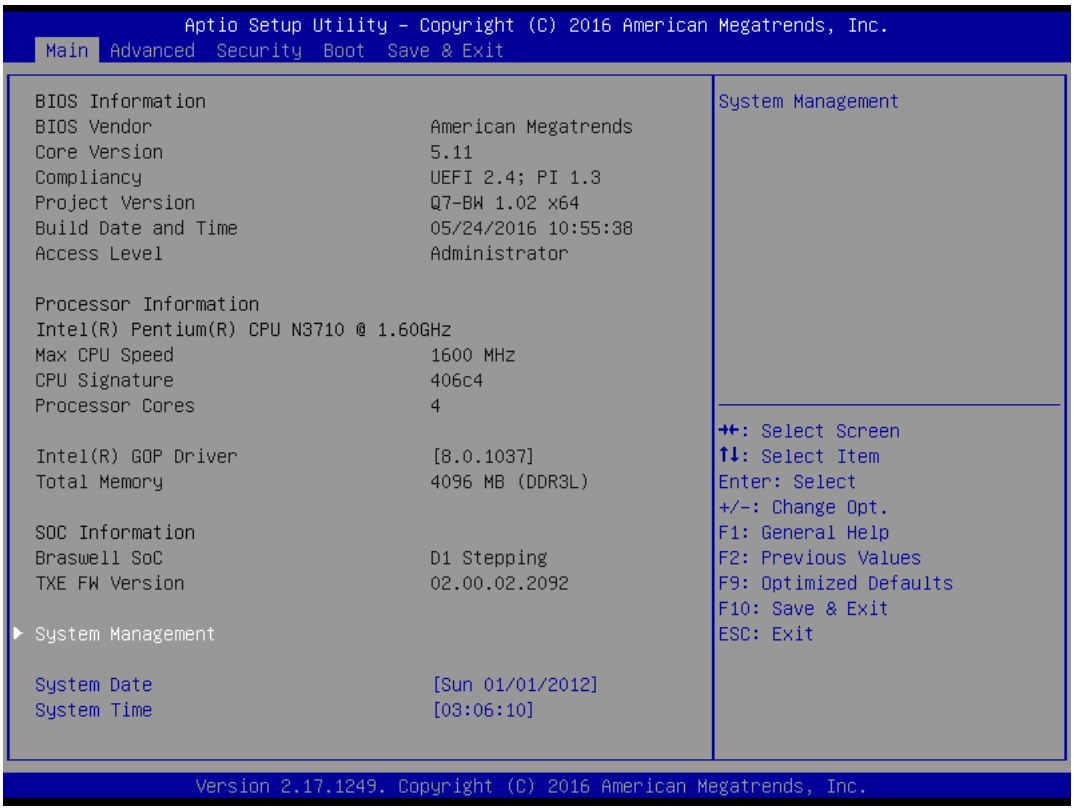


Figure 4-1: BIOS Setup Main Menu

Main Menu > System Information

Table 4-2: Main Menu > System Information

Feature	Options	Description
• Project Version	• Info only	• ADLINK BIOS version
• Build Date and Time	• Info only	• Date the BIOS was built

Main Menu > Processor Information

Table 4-3: Main Menu > Processor Information

Feature	Options	Description
• CPU Brand String	• Info only	• Display CPU brand name
• Max CPU Speed	• Info only	• Display CPU frequency
• CPU Signature	• Info only	• Display CPU ID
• Processors Cores	• Info only	• Display number of processors

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Main Menu > VGA Firmware Version

Table 4-4: Main Menu > VGA Firmware Version

Feature	Options	Description
• IGFX VBIOS Version • IGFX GOP Version	• Info only	• Display legacy VBIOS or GOP driver version

Main Menu > Memory Information

Table 4-5: Main Menu > Memory Information

Feature	Options	Description
• Total Memory	• Info only	• Display total memory information

Main Menu > SOC Information

Table 4-6: Main Menu Main Menu > SOC Information

Feature	Options	Description
• Braswell Soc	• Info only	• Display SOC stepping
• TXE FW Version	• Info only	• Display version of TXE

Main Menu > System Management

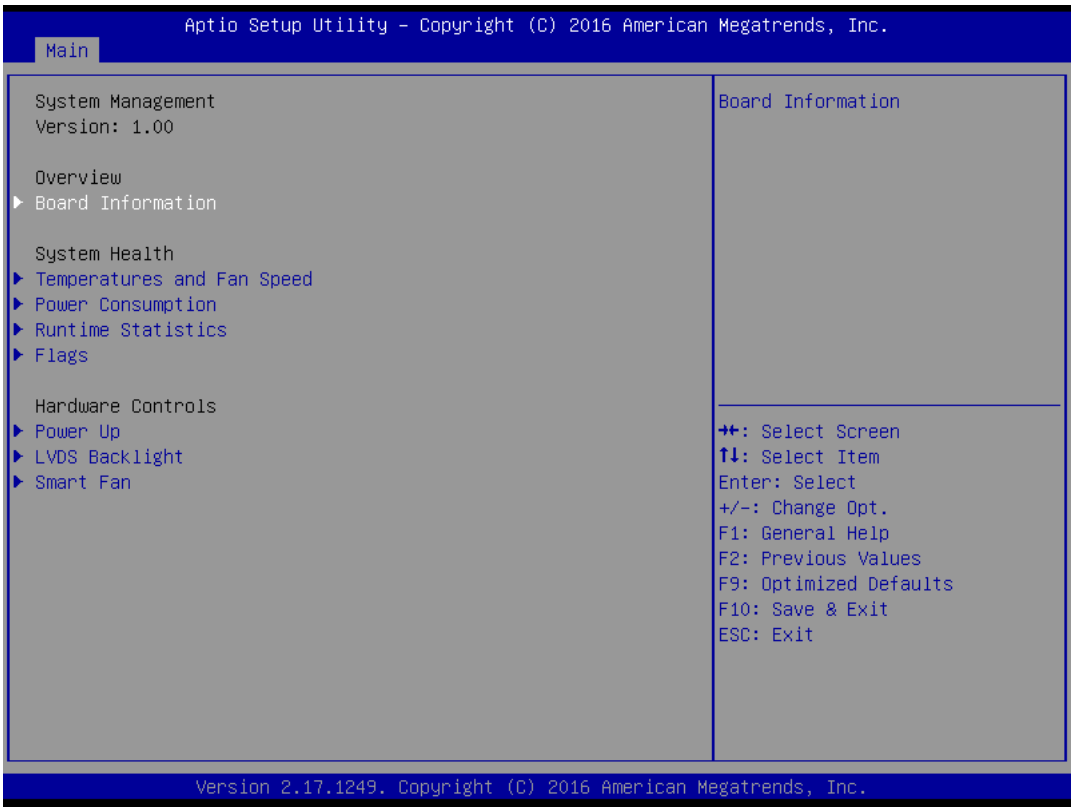


Figure 4-2: BIOS Setup Main Menu > System Management

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Main Menu > System Management > Board Information

Table 4-7: Main Menu> System Management > Board Information

Board Information	Options	Description
• SEMA Firmware	• Read only	• Display SMC firmware
Build Date	• Read only	• Display SMC firmware build date
• SEMA Boot loader	• Read only	• Display SMC boot loader
Build Date	• Read only	• Display SMC boot loader build date
• Hardware Version	• Read only	• Display SMC hardware version
• Serial Number	• Read only	• Display SMC serial number
• Manufacturing Date	• Read only	• Display SMC manufacturing date
• Last Repair Date	• Read only	• Display SMC last repair date
• MAC ID	• Read only	• Display SMC MAC ID
• SEMA Features:	• Read only	• Display SEMA features

Main Menu > System Management > Temperatures and Fan Speed

Table 4-8: Main Menu > System Management > Temperature and Fan Speed

Feature	Options	Description
• Temperatures and Fan	• Info only	
Board Temperatures	• Info only	
▷ Current	• Read only	• Display current board temperature
▷ Startup	• Read only	• Display board startup temperature
▷ Min	• Read only	• Display board min. temperature
▷ Max	• Read only	• Display board max. temperature
CPU Fan Speed	• Read only	• Display CPU fan speed

Main Menu > System Management > Power Consumption

Table 4-9: Main Menu > System Management > Power Consumption

Feature	Options	Description
• Power Consumption	• Info only	
▶ Current Input Current	• Read only	• Display input current
▶ Current Input Power	• Read only	• Display input power
▶ VCC_CORE	• Read only	• Display actual Core voltage
▶ VGG_S3	• Read only	• Display actual GFX Core voltage
▶ V1P05_A	• Read only	• Display actual V1.05 voltage
▶ VDDQ	• Read only	• Display actual Memory voltage
▶ VRTC	• Read only	• Display actual RTC voltage
▶ V3P3_S	• Read only	• Display actual System voltage
▶ V3P3_A	• Read only	• Display actual V3.30 voltage
▶ VNN_A	• Read only	• Display actual SOC voltage

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Table 4-9: Main Menu > System Management > Power Consumption (Continued)

▶ V1P15_S	• Read only	• Display actual V1.15 voltage
▶ V1P24_A	• Read only	• Display actual V1.24 voltage
▶ V1P8_A	• Read only	• Display actual V1.80 voltage
▶ V55VSB	• Read only	• Display actual V5.012 voltage
▶ Q7	• Read only	• Display actual 4.946 voltage

Main Menu > System Management > Runtime Statistics

Table 4-10: Main Menu > System Management > Runtime Statistics

Feature	Options	Description
• Runtime Statistics	• Info only	
▶ Total Runtime	• Read only	• The returned value specifies the total time in minutes the system is running in S0 state.
▶ Current Runtime	• Read only	• The returned value specifies the time in seconds the system is running in S0 state. • This counter is cleared when the system is removed from the external power supply.
▶ Power Cycles	• Read only	• The returned value specifies the number of times the external power supply has been shut down
▶ Boot Cycles	• Read only	• The Bootcounter is increased after a HW- or SW-Reset or after a successful power-up.
▶ Boot Reason	• Read only	• The boot reason is the event which causes the reboot of the system.

Main Menu > System Management > Flags

Table 4-11: Main Menu > System Management > Flags

Feature	Options	Description
• Flags	• Info only	
▶ BMC Flags	• Read only	
▷ BIOS Select	• Read only	• Display the selection of current BIOS ROM
▷ ATX/AT-Mode	• Read only	• Display ATX/AT-Mode
▷ Exception Code	• Read only	• System exception reason

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Main Menu > System Management > Power Up

Table 4-12: Main Menu > System Management > Power Up

Feature	Options	Description
• Power Up	• Info only	
▶ Power Up watchdog Note: F12 disables the Power Up Watchdog.	• Enabled • **Disabled**	• The Power-Up Watchdog resets the system after a certain amount of time after power-up.
▶ Power-up Mode Note: The Power-Up Mode only has affect, if the module is in ATX-Mode.	• **Turn on** • Remain off • Last State	• Turn On: The machine starts automatically when the power supply is turned on. • Remain Off: To start the machine the power button has to be pressed. • Last State: When powered on during a power failure the system will automatically power on when power is restored.

Main Menu > System Management > LVDS Backlight

Table 4-13: Main Menu > System Management > LVDS Backlight

Feature	Options	Description
• LVDS Backlight	• Info only	
▶ LVDS Backlight Bright	• 255	• The value range starts at 0 and ends at 255.

Main Menu > System Management > Smart Fan

Table 4-14: Main Menu > System Management > Smart Fan

Feature	Options	Description
• CPU Smart Fan Temperature Source	• **CPU Sensor** • System Sensor	• Select CPU smart fan source
• CPU Fan Mode	• **AUTO (Smart Fan)** • Fan Off • Fan On	• Select CPU fan mode
• CPU Trigger Point 1	• Read only	
▶ Trigger Temperature	• 40	• Specifies the temperature threshold at which the BMC turns on the CPU fan with the specified PWM level
▶ PWM Level	• 30	• Select PWM level
• CPU Trigger Point 2	• Read only	
▶ Trigger Temperature	• 50	• Specifies the temperature threshold at which the BMC turns on CPU fan the specified PWM level
▶ PWM Level	• 40	• Select PWM level
• CPU Trigger Point 3	• Read only	
▶ Trigger Temperature	• 60	• Specifies the temperature threshold at which the BMC turns on CPU fan the specified PWM level
▶ PWM Level	• 63	• Select PWM level
• CPU Trigger Point 4	• Read only	

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Table 4-14: Main Menu > System Management > Smart Fan (Continued)

▶ Trigger Temperature	• 70	• Specifies the temperature threshold at which the BMC turns on CPU fan the specified PWM level
▶ PWM Level	• 100	• Select PWM level

Main Menu > System Date and Time

Table 4-15: Main Menu > System Date and Time

Feature	Options	Description
• System Date	• Day of Week, MM/DD/YYYY	• Requires the alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)
• System Time	• HH/MM/SS	• Presented as a 24-hour clock setting in hours, minutes, and seconds

4.1.3 Advanced Menu

This menu contains the settings for most of the user interfaces in the system. The “Advanced” menu provides configuration settings for CPU, Memory, Graphics, SATA, USB, Network, Audio, PCIe Configuration, ACPI Power Management, Serial Console, Thermal, and Miscellaneous.



Inappropriate values for any of the following advanced settings below may cause system errors.

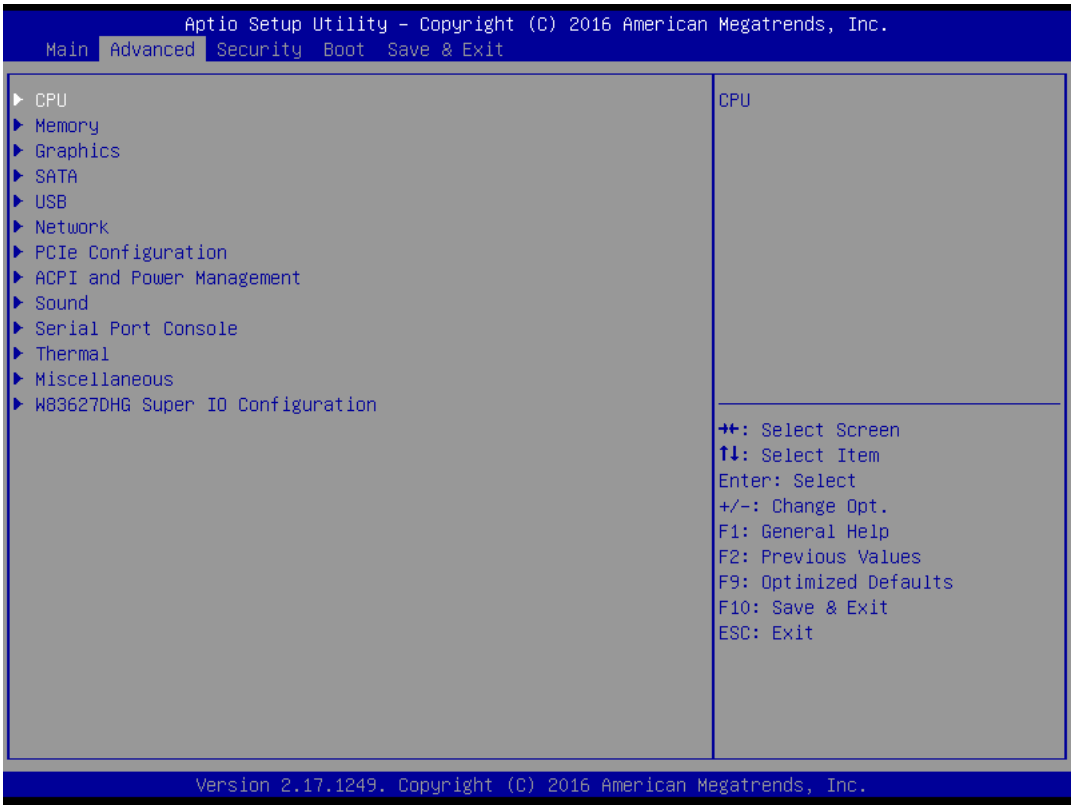


Figure 4-3: BIOS Setup Advanced Menu

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Advanced Menu > CPU

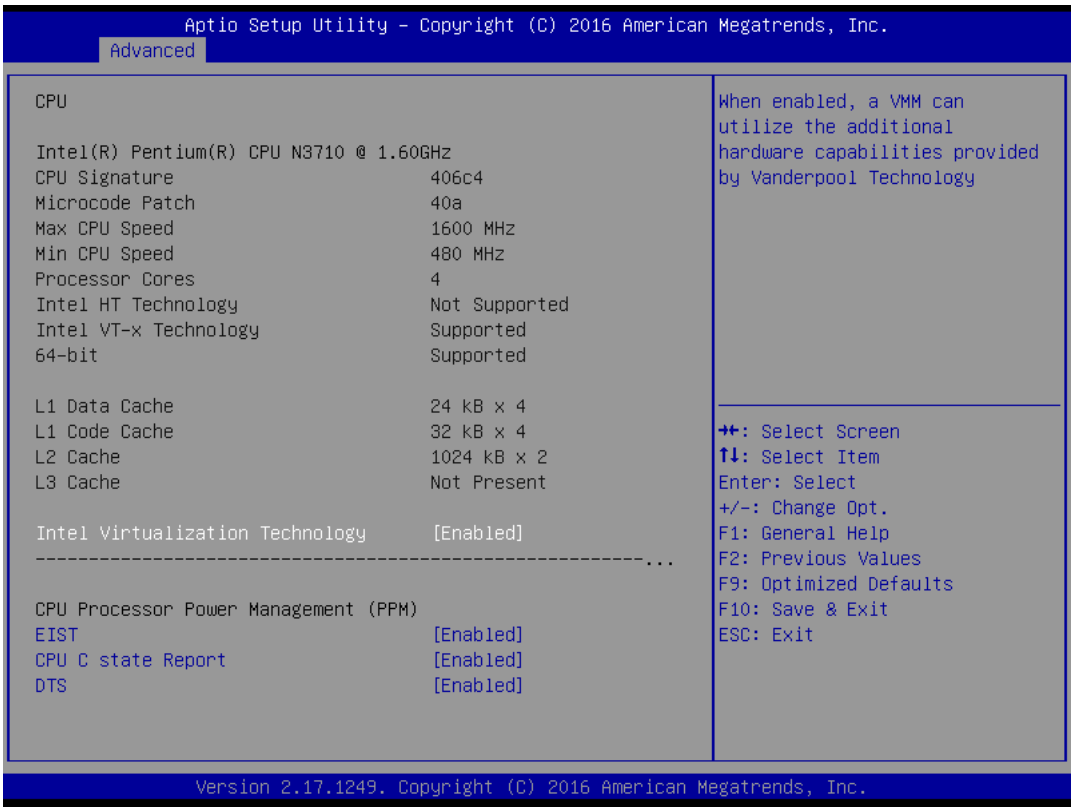


Figure 4-4: BIOS Setup Advanced Menu > CPU

Table 4-16: Advanced Menu > CPU

Feature	Options	Description
• CPU	• Info only	
• CPU Brand Name	• Info only	• Display CPU brand name
• CPU Signature	• Info only	• Display CPU signature
• Microcode Patch	• Info only	• Display microcode patch
• Max CPU speed	• Info only	• Display max. CPU speed
• Min CPU speed	• Info only	• Display min. CPU speed
• Processor Cores	• Info only	• Display number of processor cores
• Intel HT Technology	• Info only	• Display Intel HT Technology support
• Intel VT-x Technology	• Info only	• Display Intel VT-x Technology support
• 64-bit	• Info only	• Display 64-bit support
• L1 Data Cache	• Info only	• Display cache info
• L1 Code Cache	• Info only	• Display cache info
• L2 Cache	• Info only	• Display cache info
• L3 Cache	• Info only	• Display cache info
• Intel Virtualization Technology	• Disabled • **Enabled**	• When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

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Table 4-16: Advanced Menu > CPU (Continued)

• CPU Processor Power Management (PPM)	• Info only	
• EIST	• Disabled • **Enabled**	• Enable/Disable Intel SpeedStep
• CPU C state Report	• Disabled • **Enabled**	• Enable/Disable CPU C state report to OS
• DTS	• Disabled • **Enabled**	• Enabled/Disable digital thermal sensor

Advanced Menu > Memory

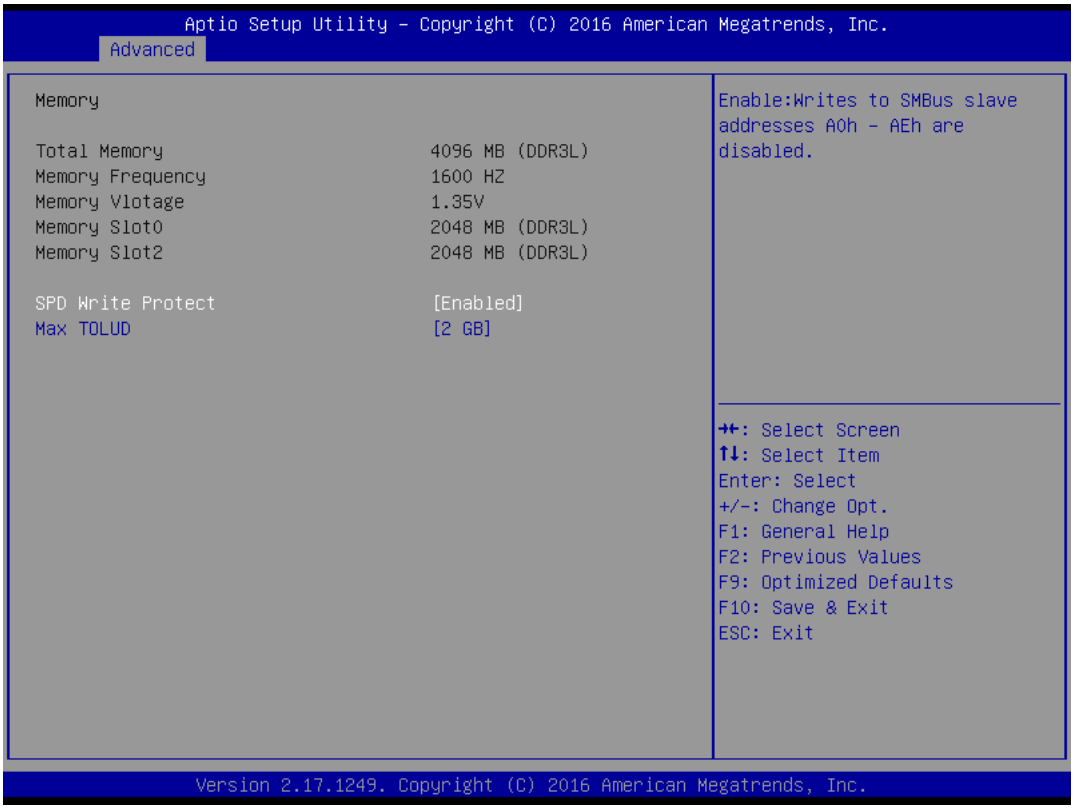


Figure 4-5: BIOS Setup Advanced Menu > Memory

Table 4-17: Advanced Menu > Memory

Feature	Options	Description
• Memory	• Info only	
• Total Memory	• Info only	• Display total memory
• Memory Frequency	• Info only	• Display memory frequency
• Memory Voltage	• Info only	• Display memory vlotage
• Memory Slot0	• Info only	• Display DIMM#0
• SPD Write Protect	• **Enabled** • Disabled	• Enabled: Writes to SMBus slave addresses A0h – Aeh are disabled

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Table 4-17: Advanced Menu > Memory (Continued)

• Max TOLUD	• **2 GB** • 2.25 GB • 2.5 GB • 2.75 GB • 3 GB	• Maximum value of TOLUD

Advanced Menu > Graphics

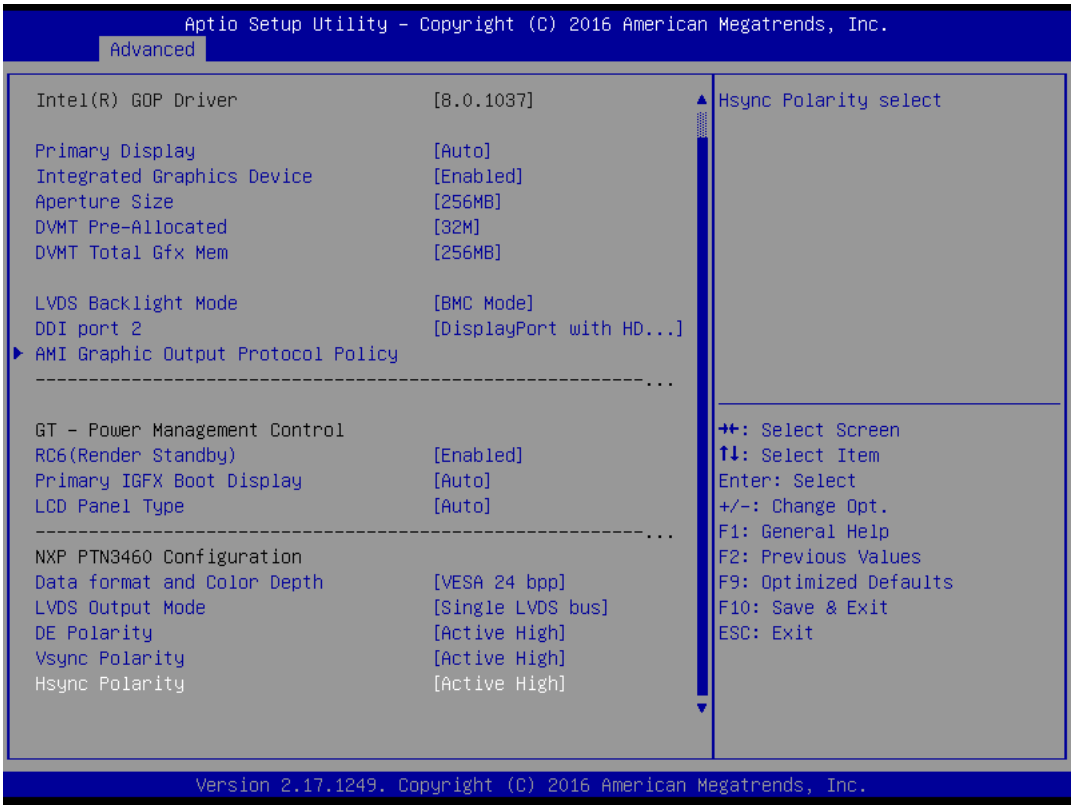


Figure 4-6: BIOS Setup Advanced Menu > Graphics

Table 4-18: Advanced Menu > Graphics

Feature	Options	Description
• Graphics	• Info only	
• IGFX VBIOS Version	• Info only	
• Primary Display	• **Auto** • IGD • PCIE	• Select which graphics device (IGD/PCI) should be primary display
• Integrated Graphics Device	• **Enabled** • Disabled	• Enabled: Enable Integrated Graphics Device (IGD) when selected as the primary display; Disabled: Always disable IGD
• Aperture Size	• **256MB**	• Select the aperture size
• DVMT Pre-Allocated	• **32M**	• Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.

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Table 4-18: Advanced Menu > Graphics (Continued)

• DVMT Total Gfx Mem	• **256MB**	• Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.
• LVDS Backlight Mode	• **BMC Mode** • GTT Mode	• Select LVDS backlight control function.
• DDI Port 2	• No Device • Display Port • HDMI • **DisplayPort with HDMI/DVI Compatible**	• DDI port 2 function to choose Display Port, HDMI, or DisplayPort with HDMI/DVI Compatible.
• AMI Graphics Output Protocol Policy • [UEFI GOP only]	• Submenu	• User select monitor output by graphics output protocol
• GT – Power Management Control	• Info only	
• RC6 (Render Standby)	• Enabled • **Disabled**	• Enable/Disable render standby support
• Primary IGFX Boot Display	• **Auto** • EFP • LFP • EFP2	• Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display
• LCD Panel Type	• **Auto**	• Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item.
• NXP PTN3460 Configuration	• Info only	
• Data format and Color Depth	• **VESA 24 bpp** • JEIDA 24 bpp • JEIDA/vesa 18 bpp	• Data format and Color Depth select
• LVDS Output Mode	• Dual LVDS bus • **Single LVDS bus**	• Single/Dual mode select
• DE Polarity	• **Active High** • Active Low	• DE Polarity select
• Vsync Polarity	• **Active High** • Active Low	• Vsync Polarity select
• Hsync Polarity	• **Active High** • Active Low	• Hsync Polarity select

Advanced Menu > Graphics > AMI Graphics Output Protocol Policy

Table 4-19: Advanced Menu > Graphics > AMI Graphics Output Protocol Policy

Feature	Options	Description
• Intel(R) Valley View Graphics Controller	• Info only	
• Intel(R) GOP Driver	• Info only	
• Output Select [List connect device]	• HDMI1	• Output Interface.
• Brightness Setting [LFP device connect only]	• 255	• Set GOP Brightness value.
• BIST Enable	• Enabled • **Disabled**	• Starts or stops the built-in self-test (BIST) on the integrated display panel.

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Advanced Menu > SATA

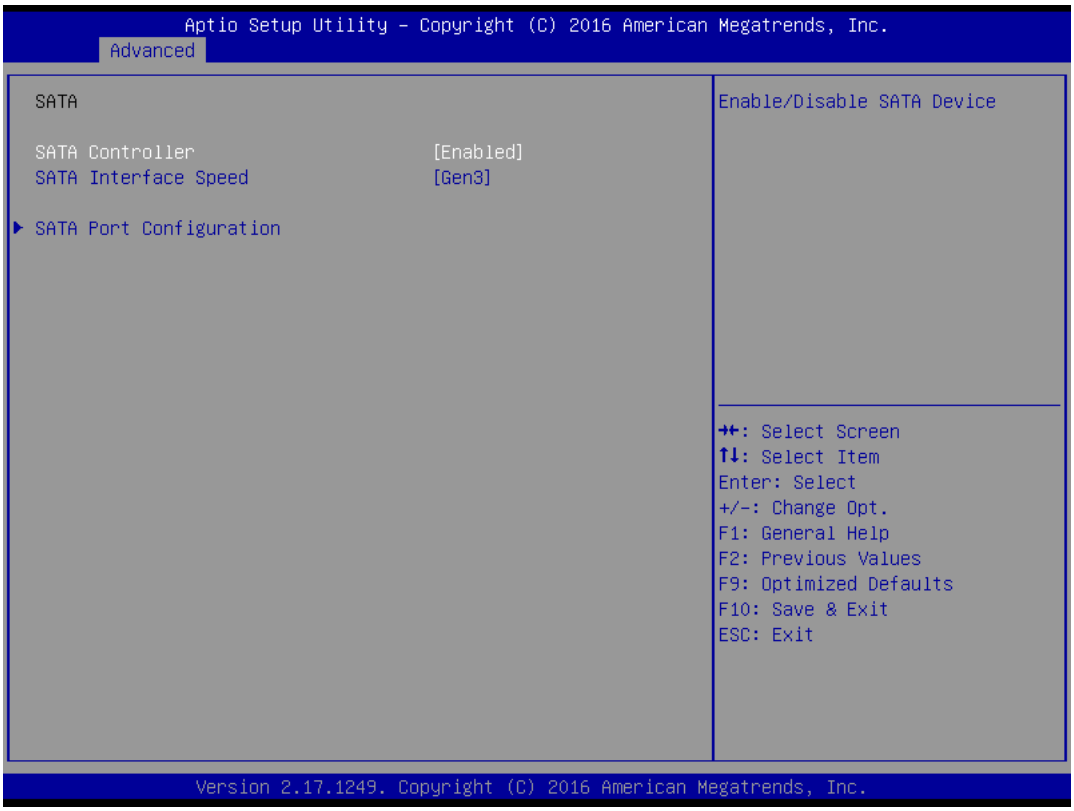


Figure 4-7: BIOS Setup Advanced Menu > SATA

Table 4-20: Advanced Menu > SATA

Feature	Options	Description
• SATA	• Info only	
• SATA Controller(s)	• **Enabled** • Disabled	• Enable/Disable SATA Device.
• SATA Interface Speed	• Gen1 • **Gen2** • Gen3	• Select SATA Interface speed, CHV A1 always with Gen1 Speed.
• SATA Port Configuration	• Submenu	

Advanced Menu > SATA > SATA Port Configuration

Table 4-21: Advanced Menu > SATA > SATA Port Configuration

Feature	Options	Description
• SATA Port Configuration	• Info only	
• Port X	• Disabled • **Enabled**	• Enable/Disable SATA port X.
• Spin Up Device	• Enabled • **Disabled**	• If enabled for any of ports, Staggerred Spin Up will be performed, and only the drives that have this option enabled will spin up at boot. Otherwise, all drives spin up at boot.

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Table 4-21: Advanced Menu > SATA > SATA Port Configuration (Continued)

• Device Sleep Support	• Enabled • **Disabled**	• Enable/Disable Device Sleep Support on that port.
• HotPlug	• Enabled • **Disabled**	• Enable/Disable SATA port X hotplug.

Advanced Menu > USB



Figure 4-8: BIOS Setup Advanced Menu > USB

Table 4-22: Advanced Menu > USB

Feature	Options	Description
• USB	• Info only	
• USB Module Version	• Info only	
• USB Devices	• Info only	• Drives, keyboards, mouse, hubs
• Legacy USB Support	• **Enabled** • Disabled • Auto	• Enables legacy USB support. • Auto option disables legacy support if no USB devices are connected. • Disable option will keep USB devices available only for EFI applications and setup.
• XHCI Hand-off	• **Enabled** • Disabled	• This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI OS driver.
• USB Mass Storage Driver Support	• **Enabled** • Disabled	• Enable/Disable USB mass storage driver support.

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Table 4-22: Advanced Menu > USB (Continued)

• USB Configuration	• Submenu	
• USB hardware delays and time-outs:	• Info only	
• USB transfer time-out	• 1 sec • 5 sec • 10 sec • **20 sec**	• The time-out value for control, bulk, and interrupt transfers
• Device reset time-out	• 10 sec • **20 sec** • 30 sec • 40 sec	• USB mass storage device Start Unit command time-out.
• Device power-up delay	• **Auto** • Manual	• Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.
• Mass Storage Devices	• Info only	• List current USB mass storage devices.

Advanced Menu > USB > USB Configuration

Table 4-23: Advanced Menu > USB > USB Configuration

Feature	Options	Description
• USB Configuration	• Info only	
• XHCI Mode	• **Enabled** • Disabled	• Mode of operation of xHCI controller.

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Advanced Menu > Network

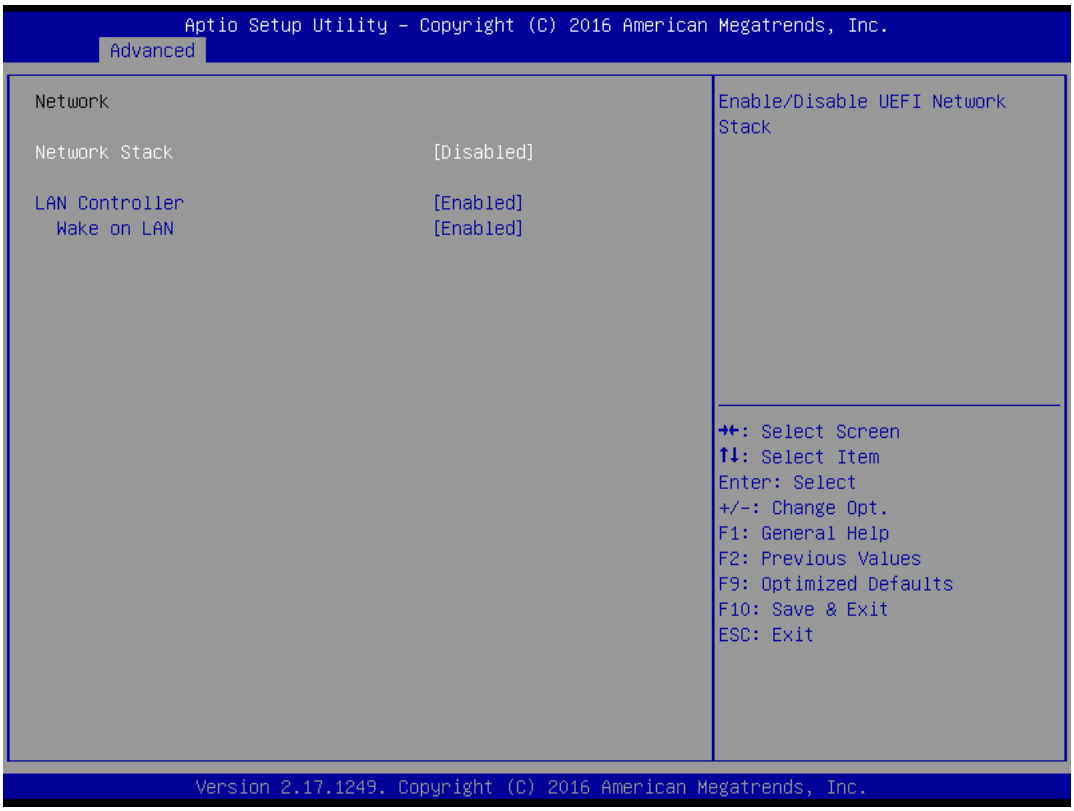


Figure 4-9: BIOS Setup Advanced Menu > Network

Table 4-24: Advanced Menu > Network

Feature	Options	Description
• Network	• Info only	
• Network Stack	• Enabled **Disabled**	• Enable/Disable UEFI network stack.
• LAN Controller	• **Enabled** Disabled	• Enable/Disable LAN controller.
• Wake on LAN	• Disable • **Enabled**	• If Enabled: LAN_PWR is always on; If Disabled: LAN_PWR is off after entering Suspend mode.

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Advanced Menu > PCIe Configuration

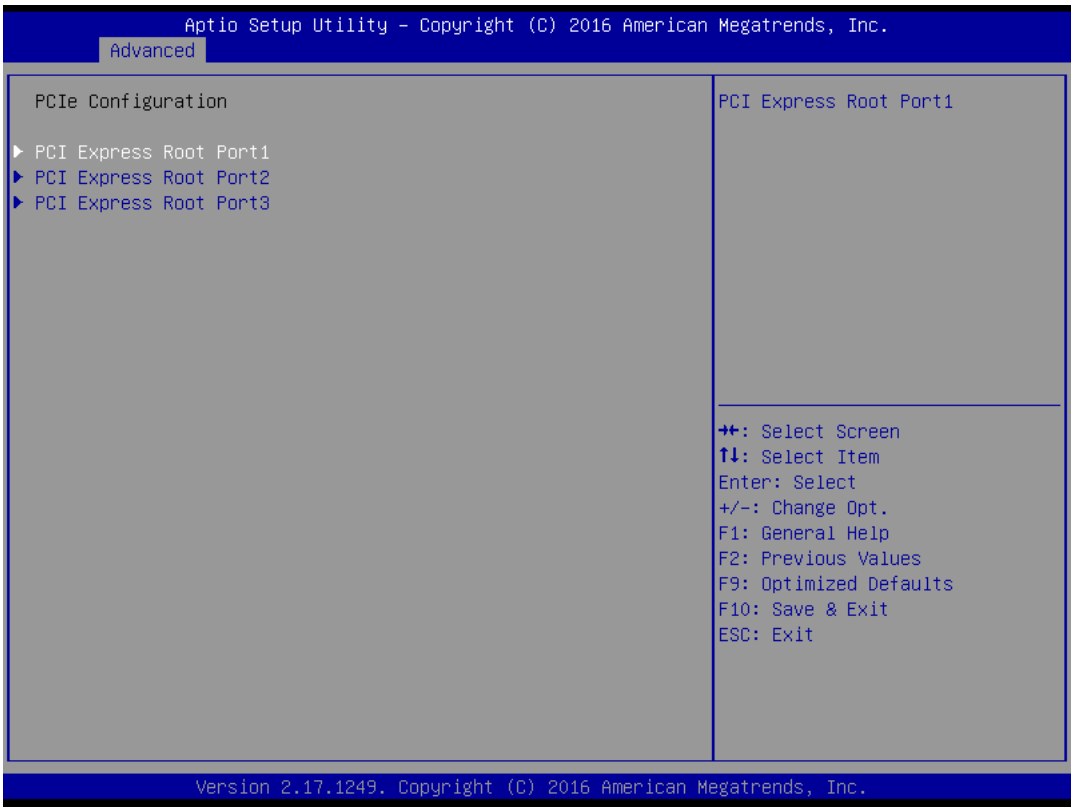


Figure 4-10: BIOS Setup Advanced Menu > PCIe Configuration

Table 4-25: Advanced Menu > PCIe Configuration

Feature	Options	Description
• PCIe Configuration	• Info only	
• PCI Express Root Port x	• Submenu	

Advanced Menu > PCIe Configuration > PCI Express Root Port x

Table 4-26: Advanced Menu > PCIe Configuration > PCI Express Root Port x

Feature	Options	Description
• PCI Express Port x	• **Enabled** • Disabled	• Control the PCI Express Root Port.
• ASPM	• Auto • **Disabled** • L0s • L1 • L0sL1	• PCI Express Active State Power Management settings.
• URR	• **Disabled** • Enabled	• PCI Express Unsupported Request Reporting Enable/Disable.
• FER	• **Disabled** • Enabled	• PCI Express Device Fatal Error Reporting Enable/Disable.
• NFER	• **Disabled** • Enabled	• PCI Express Device Non-Fatal Error Reporting Enable/Disable.

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Table 4-26: Advanced Menu > PCIe Configuration > PCI Express Root Port x (Continued)

• CER	• **Disabled** • Enabled	• PCI Express Device Correctable Error Reporting Enable/Disable.
• SEFE	• **Disabled** • Enabled	• Root PCI Express System Error on Fatal Error Enable/Disable.
• SENFE	• **Disabled** • Enabled	• Enable or disable Root PCI Express System Error on Non-Fatal Error.
• SECE	• **Disabled** • Enabled	• Root PCI Express System Error on Correctable Error Enable/Disable.
• PME SCI	• Disabled • **Enabled**	• PCI Express PME SCI Enable/ Disable.
• Hot Plug	• **Disabled** • Enabled	• Enable or disable PCI Express hotplug.
• PCIe Speed	• **Auto** • Gen 2 • Gen 1	• Configure PCIe port speed.

Advanced Menu > ACPI and Power Management

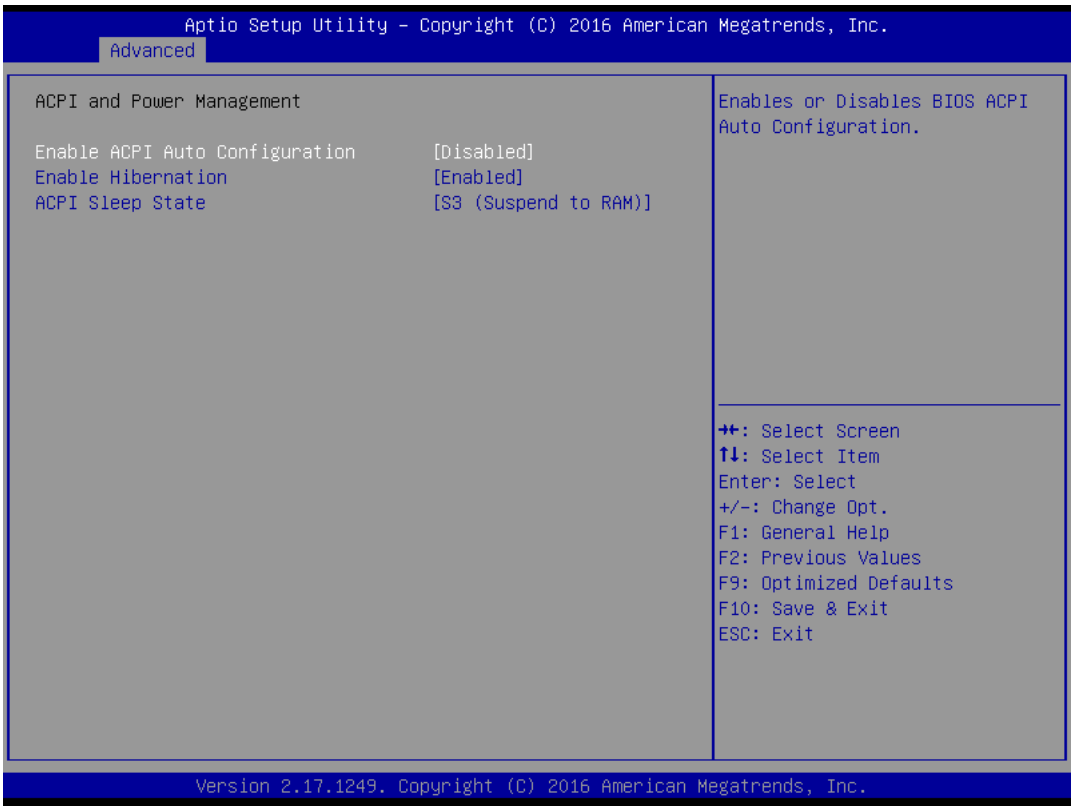


Figure 4-11: BIOS Setup Advanced Menu > ACPI and Power Management

Table 4-27: Advanced Menu > ACPI and Power Management

Feature	Options	Description
• ACPI and Power Management	• Info only	
• Enable ACPI Auto Configuration	• Enabled **Disabled**	• Enables or disables BIOS ACPI Auto Configuration.

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Table 4-27: Advanced Menu > ACPI and Power Management (Continued)

• Enable Hibernation	• **Enabled** Disabled	• Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
• ACPI Sleep State	• Suspend Disabled • **S3 (Suspend to RAM)**	• Select the highest ACPI sleep state the system will enter when the Suspend button is pressed.

Advanced Menu > Sound

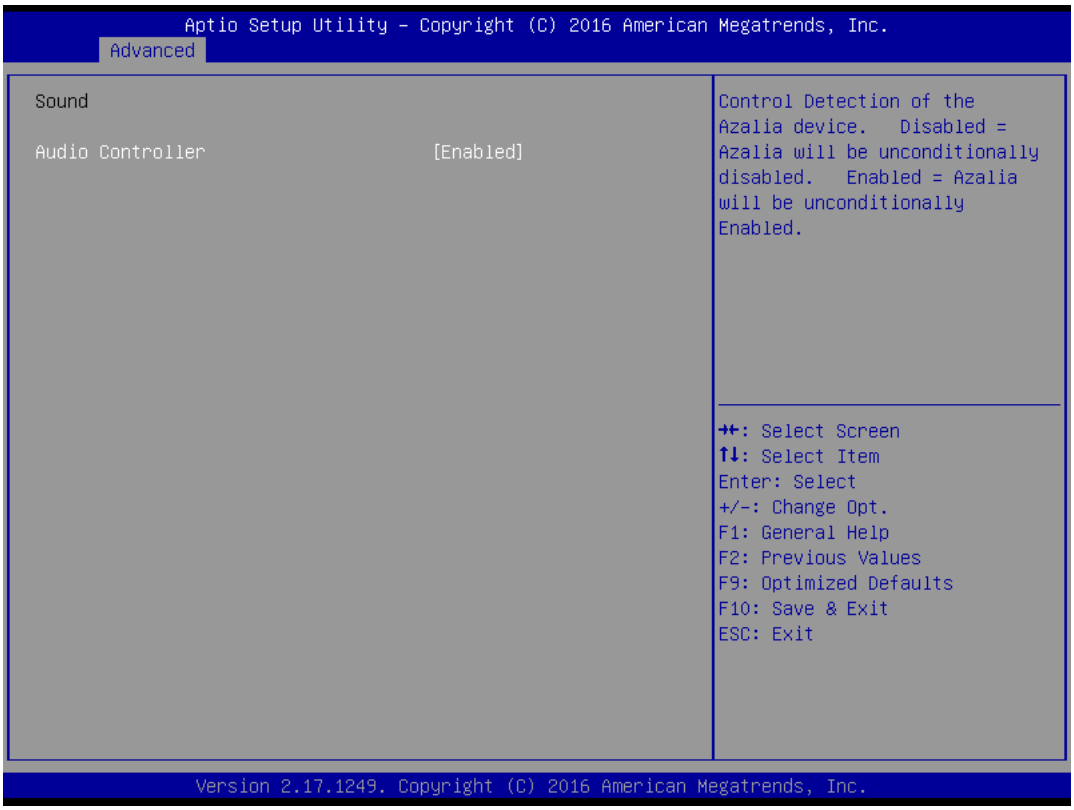


Figure 4-12: BIOS Setup Advanced Menu > Sound

Table 4-28: Advanced Menu > Sound

Feature	Options	Description
• Sound	• Info only	
• Audio Controller	• Disabled • **Enabled**	• Control Detection of the Azalia device. Disabled = Azalia will be unconditionally disabled. Enabled = Azalia will be unconditionally Enabled.

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Advanced Menu > Serial Port Console

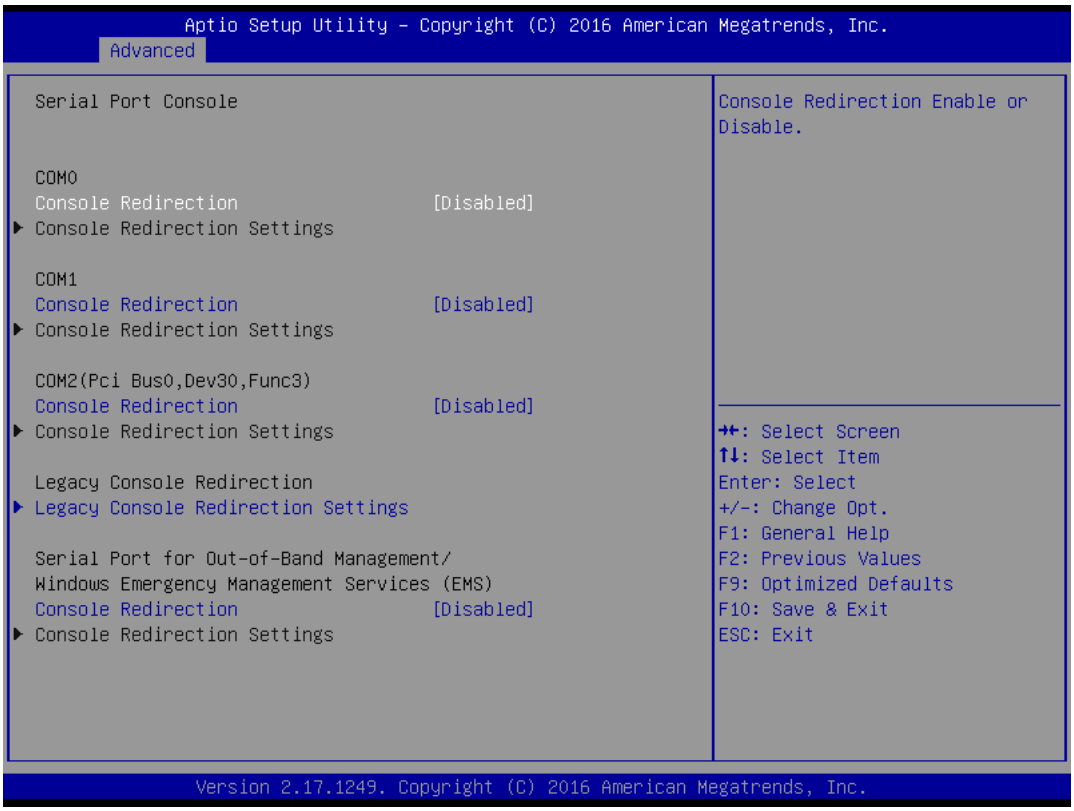


Figure 4-13: BIOS Setup Advanced Menu > Serial Port Console

Table 4-29: Advanced Menu > Serial Port Console

Feature	Options	Description
• Serial Port Console	• Info only	
• COM0	• Info only	
▶ Console Redirection	• **Disabled** • Enabled	• Console Redirection enable or disable.
▶ Console Redirection Settings	• Submenu	• The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
• COM1	• Info only	
▶ Console Redirection	• **Disabled** • Enabled	• Console Redirection enable or disable.
▶ Console Redirection Settings	• Submenu	• The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
• COM2 (Pci Bus0,Dev30,Func3)	• Info only	

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Table 4-29: Advanced Menu > Serial Port Console (Continued)

▶ Console Redirection	• **Disabled** • Enabled	• Console Redirection enable or disable.
▶ Console Redirection Settings	• Submenu	• The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
▶ Legacy Console Redirection	• Info only	
▶ Legacy Console Redirection Settings	• Submenu	
• Serial Port for Out-of-Band • Management/Windows Emergency • Management Services (EMS)	• Info only	
▶ Console Redirection	• **Disabled** • Enabled	• Console Redirection enable or disable.
▶ Console Redirection Settings	• Submenu	• The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

Advanced Menu > Serial Port Console > Console Redirection Settings (COM0/COM1)

Table 4-30: Advanced Menu > Serial Port Console > Console Redirection (COM0/COM1)

Feature	Options	Description
• COM0/COM1 • Console Redirection Settings	• Info only	
• Terminal Type	• VT100 • VT100+ • VT-UTF8 • **ANSI**	• VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes. ANSI: Extended ASCII char set.
• Bits per second	• 9600 • 19200 • 38400 • 57600 • **115200**	• Selects serial port transmission speed. The speed must be matched on the remote computer. Long or noisy lines may require lower speeds.
• Data Bits	• 7 • **8**	• Select data bits.
• Parity	• **None** • Even • Odd • Mark • Space	• Select parity.
• Stop Bits	• **1** • 2	• Select number of stop bits.
• Flow Control	• **None** • Hardware RTS/CTS	• Select flow control.
• VT-UTF8 Combo Key Support	• Disabled • **Enable**	• Enable VT-UTF8 combination key support for ANSI/VT100 terminals.

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Table 4-30: Advanced Menu > Serial Port Console > Console Redirection (COM0/COM1) (Continued)

• Recorder Mode	• **Disabled** • Enable	• With this mode enabled only text will be sent. This is to capture terminal data.
• Resolution 100x31	• **Disabled** • Enable	• Enables or disables extended terminal resolution
• Legacy OS Redirection	• **80x24** • 80x25	• On legacy OSes, the number of rows and columns supported by redirection
• Putty KeyPad	• **VT100** • LINUX • XTERMR6 • SCO • ESCN • VT400	• Select FunctionKey and KeyPad on Putty.
• Redirection After BIOS Post	• **Always Enabled** • BootLoader	• The Settings specify if BootLoader is selected, then legacy console redirection is disabled before booting to legacy OS. Default value is Always Enable which means legacy console redirection is enabled for legacy OS.

Advanced Menu > Serial Port Console > Legacy Console Redirection Settings

Table 4-31: Advanced Menu > Serial Port Console > Serial Port Legacy Console Redirection

Feature	Options	Description
• Legacy Serial Redirection Port	• **COM0** • COM1 • COM2 (Pci Bus0,Dev30,Func3)	• Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages

Advanced Menu > Serial Port Console > Console Redirection Settings (EMS)

Table 4-32: Advanced Menu > Serial Port Console > Serial Port Console Redirection Settings (EMS)

Feature	Options	Description
• Out-of-Band Mgmt Port	• **COM0** • COM1 • COM2 (Pci Bus0,Dev30,Func3)	• Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.
• Terminal Type	• VT100 • VT100+ • **VT-UTF8** • ANSI	• VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.
• Bits per second	• 9600 • 19200 • 57600 • **115200**	• Selects serial port transmission speed. The speed must be matched on the remote computer. Long or noisy lines may require lower speeds.

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Table 4-32: Advanced Menu > Serial Port Console > Serial Port Console Redirection Settings (EMS) (Continued)

• Flow Control	• **None** • Hardware RTS/CTS • Software Xon/Xoff	• Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
• Data Bits	• Info only	
• Parity	• Info only	
• Stop Bits	• Info only	

Advanced Menu > Thermal

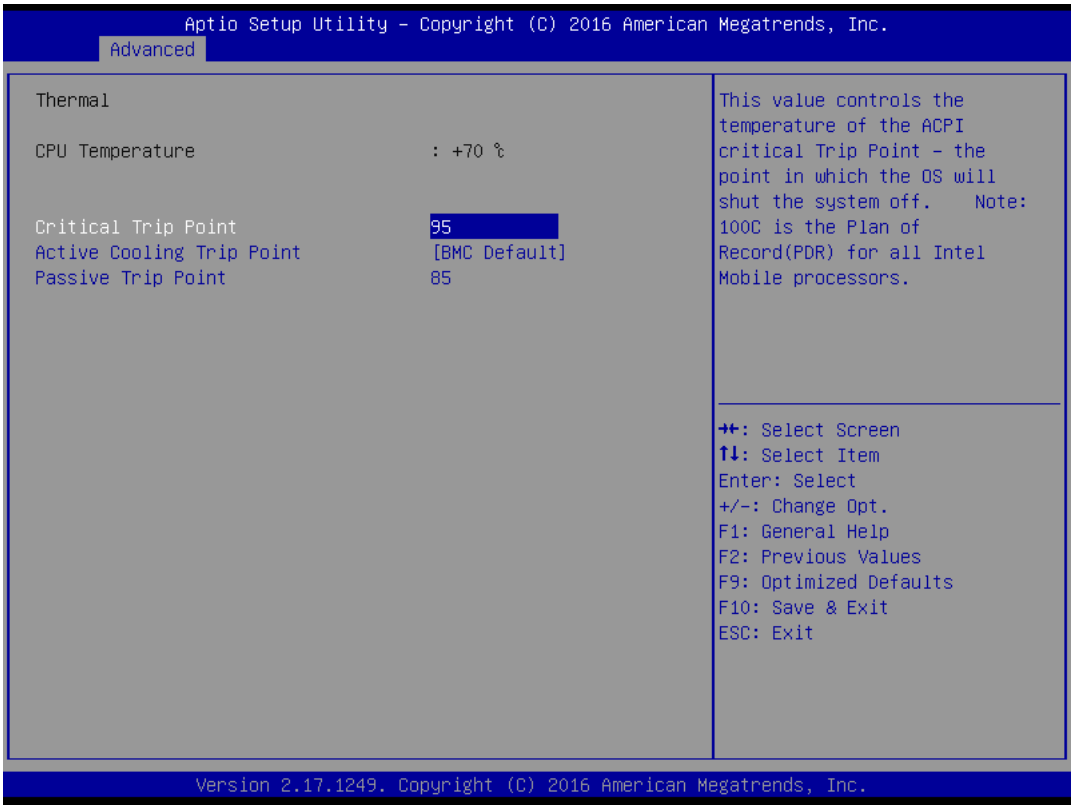


Figure 4-14: BIOS Setup Advanced Menu > Thermal

Table 4-33: Advanced Menu > Thermal

Feature	Options	Description
• Thermal	• Info only	
• CPU Temperature	• Info only	

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Table 4-33: Advanced Menu > Thermal (Continued)

• Critical Trip Point	• 95 C	• This value controls the temperature of the ACPI critical Trip Point - the point in which the OS will shut the system off. Note: 100C is the Plan of Record (PDR) for all Intel Mobile processors.
• Active Cooling Trip Point	• Disabled • 40 C • 50 C • 60 C • 70 C • **BMC Default**	• Active Cooling Trip Point.
• Passive Trip Point	• **Disabled** • 90 C • 80 C	• This value controls the temperature of the ACPI critical Trip Point - the point in which the OS will begin throttling the processor.

Advanced Menu > Miscellaneous

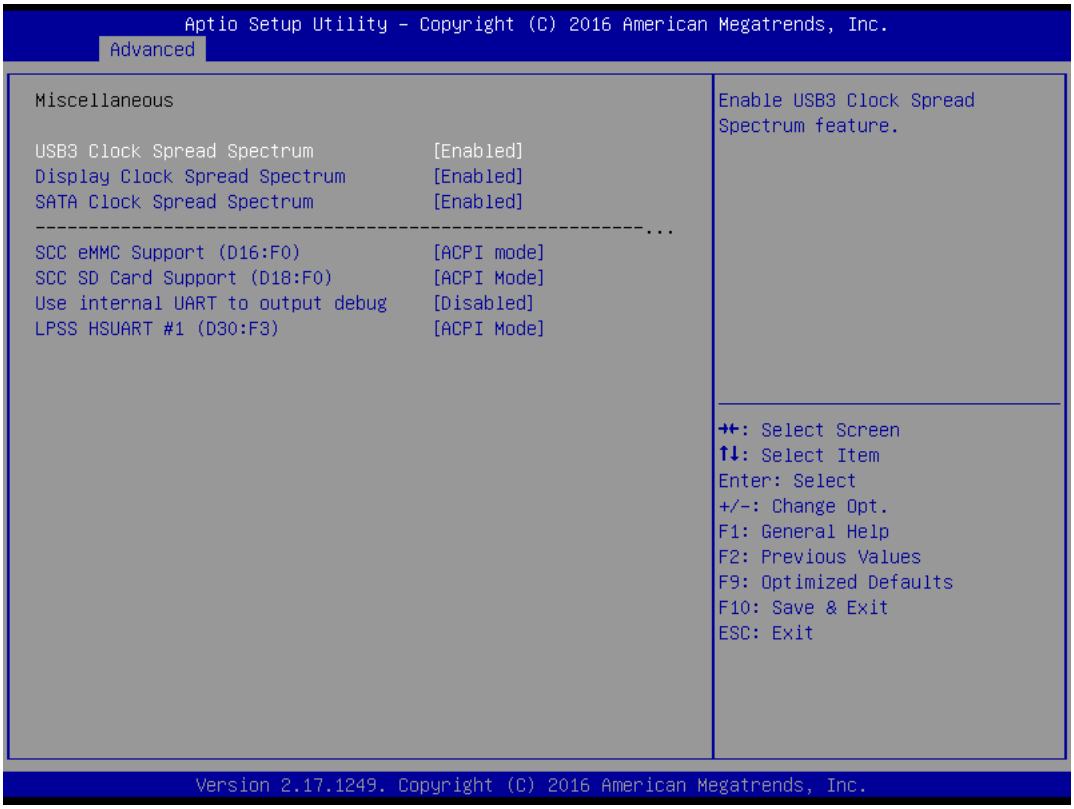


Figure 4-15: BIOS Setup Advanced Menu > Miscellaneous

Table 4-34: Advanced Menu > Miscellaneous

Feature	Options	Description
• Miscellaneous	• Info only	
• USB3 Clock Spread Spectrum	• **Enabled** • Disabled	• Enable USB3 Clock Spread Spectrum feature.

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Table 4-34: Advanced Menu > Miscellaneous (Continued)

• Display Clock Spread Spectrum	• Enabled **Disabled**	• Enable DISPLAY Clock Spread Spectrum feature.
• SATA Clock Spread Spectrum	• Enabled **Disabled**	• Enable SATA Clock Spread Spectrum feature.
• SCC eMMC Support (D16:F0)	• ACPI mode • PCI mode • **Disable**	• SCC eMMC support enable/disable.
• SCC SD Card Support (D18:F0)	• ACPI mode • PCI mode • **Disable**	• SCC SD card support enable/ disable.
• Internal Uart	• Disabled • **Enable**	• Enable/Disable Internal UART
• LPSS HSUART #1 (D30:F3)	• **ACPI mode** • PCI mode • Disable	• Enable/Disable LPSS HSUART #1 Support

Advanced Menu > W83627DHG Super IO Configuration

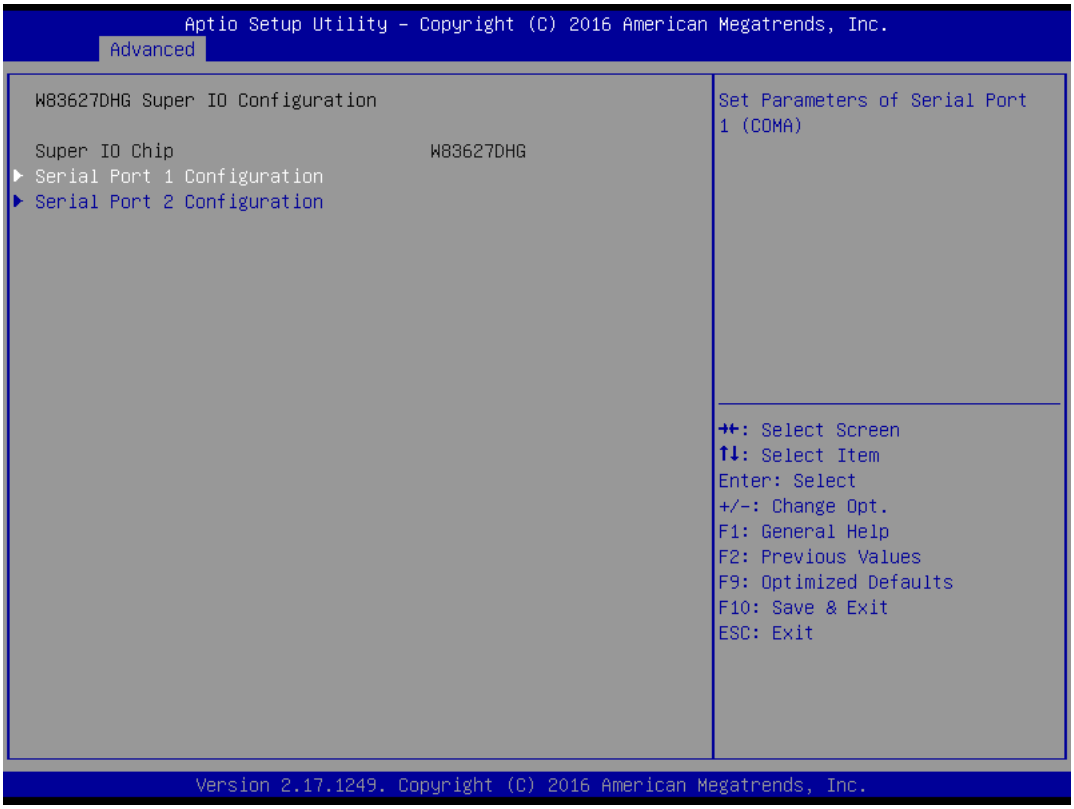


Figure 4-16: BIOS Setup Advanced Menu > W83627DHG Super IO Configuration

Table 4-35: Advanced Menu > W83627DHG Super IO Configuration

Feature	Options	Description
• Super IO Chip	• Info only	
• Serial Port 1 Configuration	• Submenu	
• Serial Port 2 Configuration	• Submenu	

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Table 4-35: Advanced Menu > W83627DHG Super IO Configuration (Continued)

• Serial Port 1 Configuration ▶ Serial Port	• **Enabled** Disabled	• Enable/Disable Serial Port 1 (COM0).
▶ Device Settings	• IO=3F8h; IRQ=4	• Fixed configuration of serial port.
▶ Change Settings	• **Auto** • IO=3F8h; IRQ=4 • IO=3F8h; IRQ=3,4,5,6,7,10,11,12 • IO=2F8h; IRQ=3,4,5,6,7,10,11,12 • IO=3E8h; IRQ=3,4,5,6,7,10,11,12 • IO=2E8h; IRQ=3,4,5,6,7,10,11,12	• Select an optimal setting for Super IO device.
• Serial Port 2 Configuration ▶ Serial Port	• **Enabled** Disabled	• Enable/Disable Serial Port 2 (COM1).
▶ Device Settings	• IO=2F8h; IRQ=3	• Fixed configuration of serial port.
▶ Change Settings	• **Auto** • IO=2F8h; IRQ=3 • IO=3F8h; IRQ=3,4,5,6,7,10,11,12 • IO=2F8h; IRQ=3,4,5,6,7,10,11,12 • IO=3E8h; IRQ=3,4,5,6,7,10,11,12 • IO=2E8h; IRQ=3,4,5,6,7,10,11,12	• Select an optimal setting for Super IO device.

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4.1.4 Security Menu

The Security menu allows you to set User and Administrator system passwords and to retrieve secure boot information.

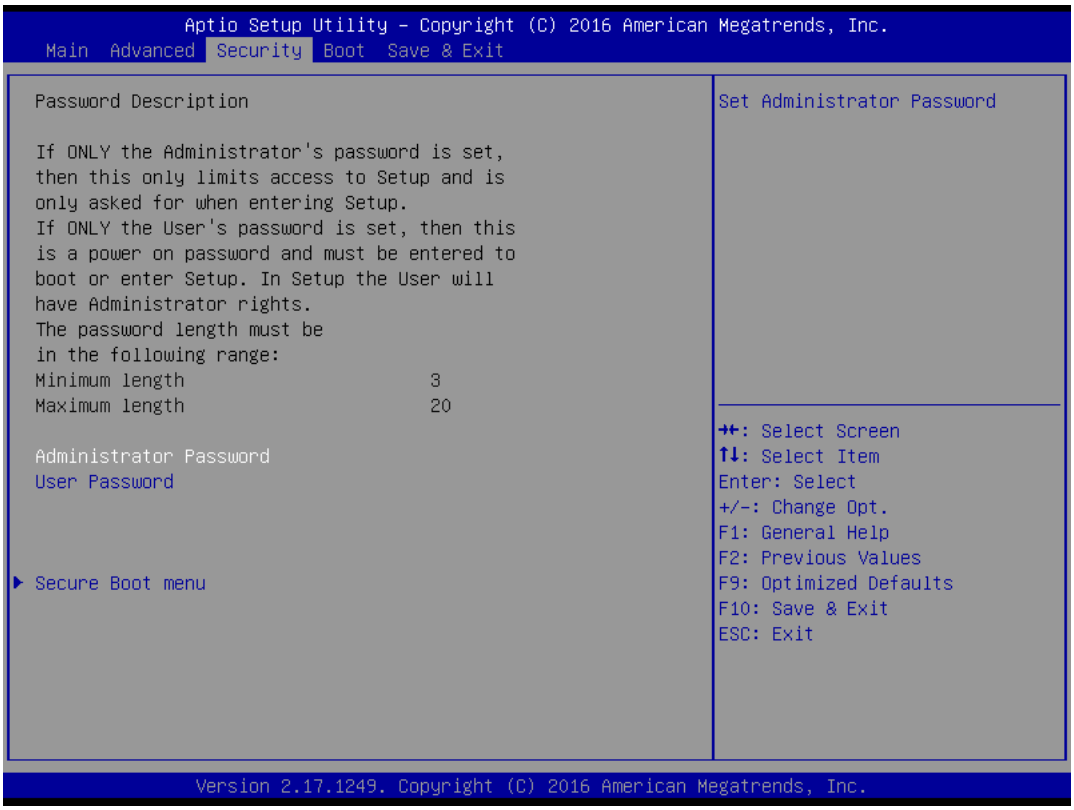


Figure 4-17: BIOS Setup Security Menu

Security Menu > Password Description

Table 4-36: Security Menu > Password

Feature	Options	Description
• Administrator Password	• Enter password	
• User Password	• Enter password	
• Secure Boot menu	• Submenu	• Customizable Secure Boot settings.

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Security Menu > Secure Boot

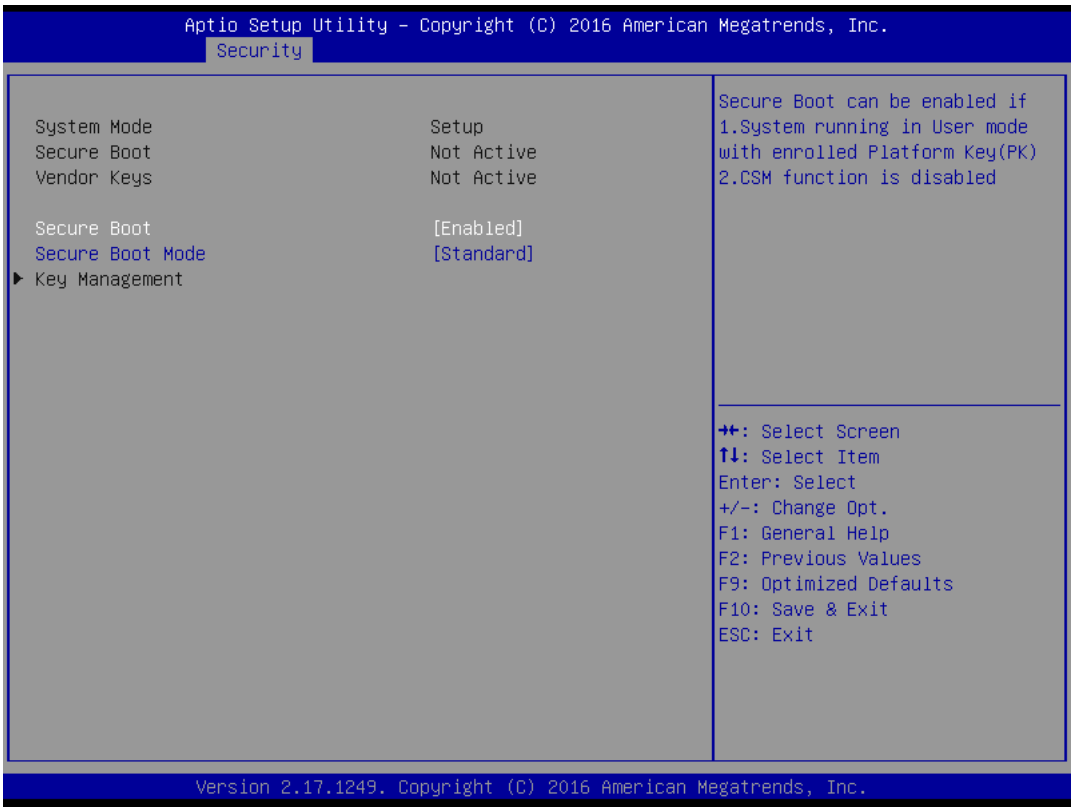


Figure 4-18: BIOS Setup Security Menu > Secure Boot

Table 4-37: Security Menu > Secure Boot

Feature	Options	Description
• System Mode	• Info only	
• Secure Boot	• Info only	
• Vendor Keys	• Info only	
• Secure Boot	• Disabled • **Enabled**	• Secure Boot can be enabled if: 1. System running in User mode with enrolled Platform Key (PK) 2. CSM function is disabled.
• Secure Boot Mode	• **Standard** • Custom	• Secure Boot mode selector. 'Custom' Mode enables users to change Image Execution policy and manage Secure Boot keys.

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4.1.5 Boot Menu

The Boot menu allows you to configure how your system will boot and select the storage location from which the system boot up will occur.

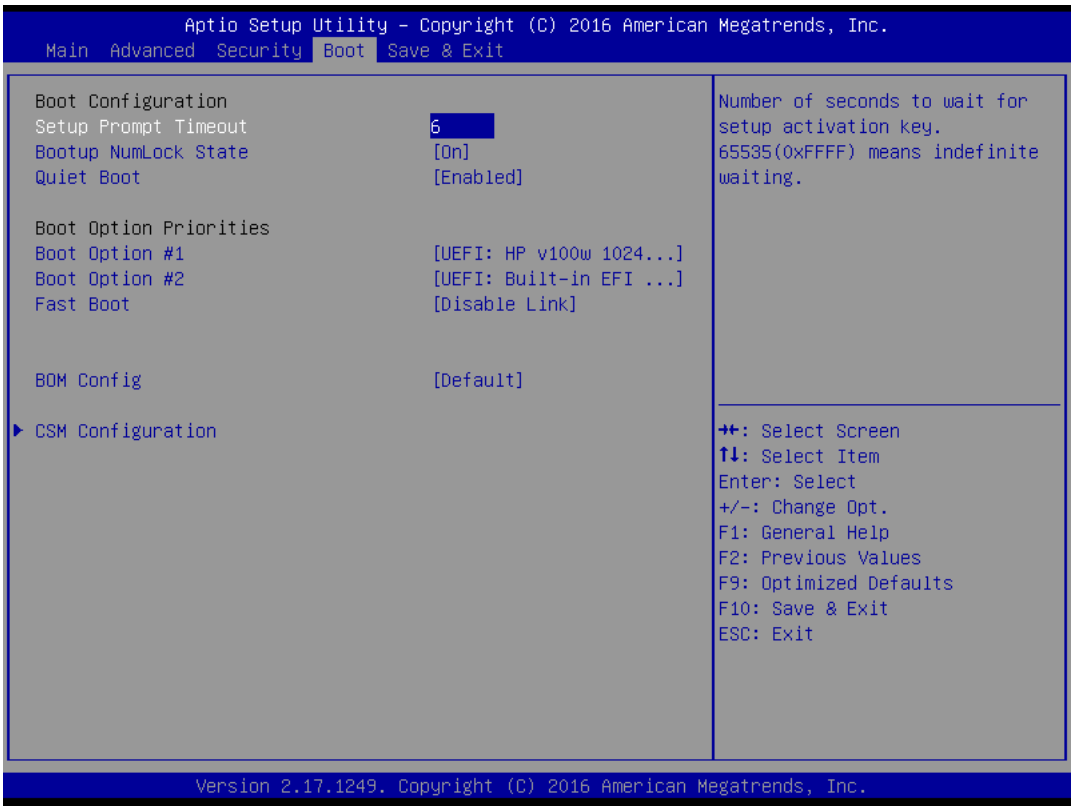


Figure 4-19: BIOS Setup Boot Menu

Table 4-38: BIOS Setup Boot Menu

Feature	Options	Description
• Boot Configuration	• Info only	
• Setup Prompt Timeout	• **6**	• Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
• Bootup NumLock State	• **On** • Off	• Select the keyboard NumLock state.
• Quiet Boot	• Disabled • **Enabled**	• Enable or disables logo Quiet Boot option for OEM Logo function.
• Boot Option Priorities	• Info only	
• Fast Boot	• **Disabled** • Enabled	• Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect on BBS boot options.
• BOM Config	• **Default** • Legacy System • Yocto Linux	• BOM Config
• Hard Drive BBS Priorities	• Info only	
• CSM Parameters	• Submenu	• CSM configuration: Enable/Disable, Option ROM execution settings, etc.

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Boot Menu > CSM Configuration

If more than one drive is attached to the Q7-BW, you can select from the “Compatibility Support Module Configuration” screen the boot order in which the drives are scanned for a bootable OS image.

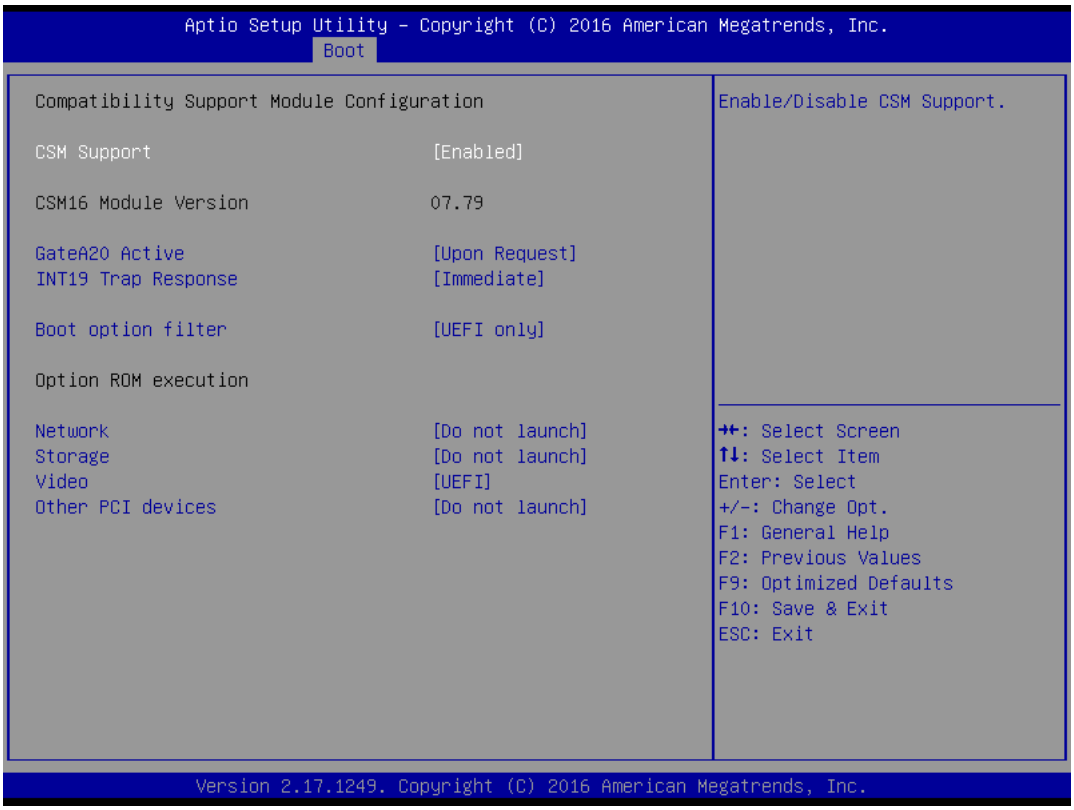


Figure 4-20: BIOS Setup Boot Menu > CSM Configuration

Boot Menu > CSM Configuration

Table 4-39: Boot Menu > CSM Configuration

Feature	Options	Description
• Compatibility Support Module Configuration	• Info	
• CSM Support	• **Enabled** • Disable	• CSM Support
• CSM16 Module Version	• Info only	
• GataA20 Active	• **Upon Request** • Always	• GataA20 Active
• INT19 Trap Response	• **Immediate** • Postponed	• INT19 Trap Response
• Boot option filter	• UEFI and Legacy • Legacy only • **UEFI only**	• Boot option filter
• Option ROM execution order	• Info only	
• Network	• **Do not launch** • UEFI only • Legacy only	• Controls the execution of UEFI and legacy PXE OpROM.

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Table 4-39: Boot Menu > CSM Configuration

• Storage	• Do not launch • UEFI only • **Legacy only**	• Controls the execution of UEFI and legacy storage OpROM.
• Video	• Do not launch • **UEFI only** • Legacy only	• Controls the execution of UEFI and legacy video OpROM.
• Other PCI devices	• **UEFI only** • Legacy only	• Determines OpROM execution policy for devices other than network, storage or video.

4.1.6 Save & Exit Menu

Use the Save and Exit menu to save or discard BIOS setting changes, restore or save setting defaults, and retrieve certain override information.

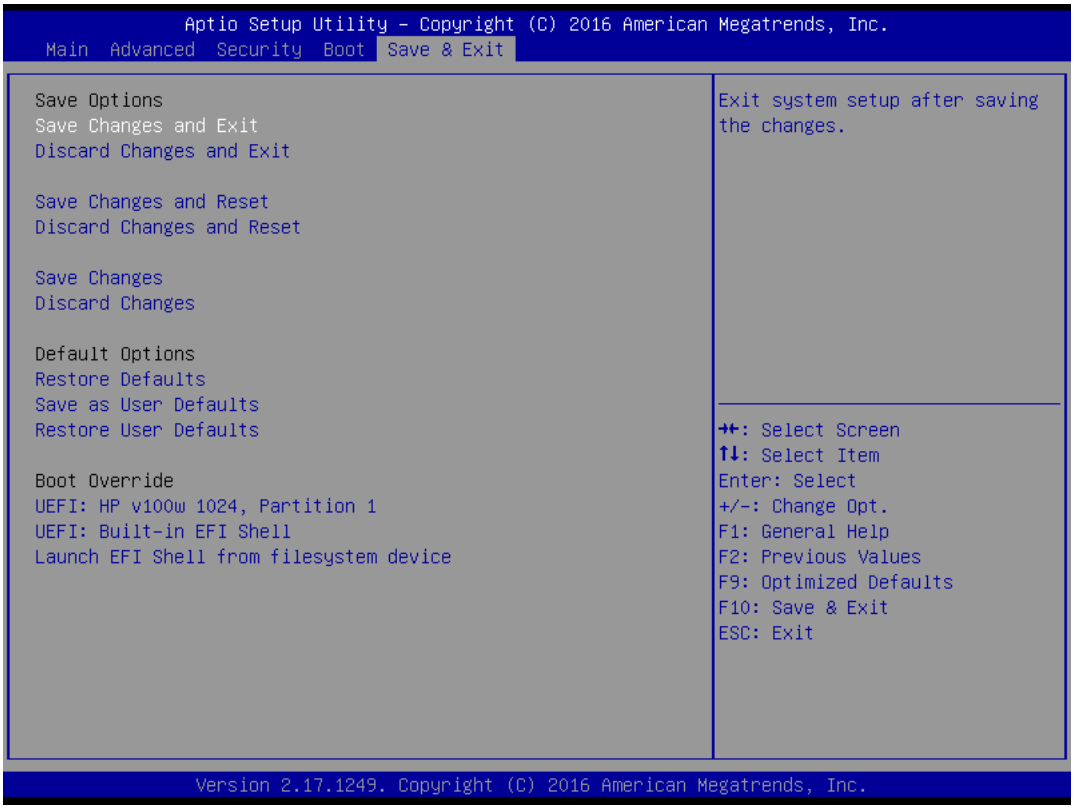


Figure 4-21: BIOS Setup Save and Exit Menu

Table 4-40: Save and Exit Menu

Feature	Options	Description
• Save Options	• Info only	
• Save Changes and Exit	Yes No	• Exit system setup after saving the changes.
• Discard Changes and Exit	Yes No	• Exit system setup without saving any changes.
• Save Changes and Reset	Yes No	• Reset the system after saving the changes.
• Discard Changes and Reset	Yes No	• Reset system setup without saving any changes.
• Save Changes	Yes No	• Save Changes done so far to any of the setup options.

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Table 4-40: Save and Exit Menu

• Discard Changes	Yes No	• Discard Changes done so far to any of the setup options.
• Default Options	• Info only	
• Restore Defaults	Yes No	• Restore/Load Default values for all the setup options.
• Save as User Defaults	Yes No	• Save the changes done so far as User Defaults.
• Restore User Defaults	Yes No	• Restore the User Defaults to all the setup options.
• Boot Override	• Info only	

4.2 SEMA functions

Under the management of the BMC chip (Board Management Controller), the SEMA utility (Smart Embedded Management Agent) provides system control and failure protection—counting, monitoring, and measuring hardware and software events, from which the SoC can trigger corrective commands. The optional SEMA Cloud utility not only controls local events on the module but system client events on the Internet of Things (IoT.) Refer to the following bullets for a list of SEMA functions.

- Total operating hours counter
  Counts the time the module has been run in minutes.
- On-time minutes counter
  Counts the seconds since last system start.
- Temperature monitoring of CPU and Board temperature
  Minimum and maximum temperature values of CPU and board are stored in flash.
- Power monitor
  Reads the current drawn by the board and reports the nominal operating voltage.
- Power cycles counter
- Boot counter
  Boot counter is increased after a HW- or SW-Reset or after a successful power-up.
- Watchdog Timer
  Set / Reset / Disable Watchdog Timer.
- System Restart Cause
  Power loss / Watchdog / External Reset.
- Flash area
  1kB Flash area for customer data
- Protected Flash area
  128 Bytes for Keys, ID's, etc. can be stored in a write- and clear-protectable region.
- Board Identify
  Vendor / Board / Serial number

The SEMA Tools are available for Windows and Linux. SEMA functionality can also be used in applications. Refer to the SEMA software manual and technical manual on the ADLINK web site for more information.

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4.2.1 Board Specific SEMA functions

Voltages

The BMC of the Q7-BW implements a Voltage Monitor and samples several Onboard Voltages. The Voltages can be read by calling the SEMA function, “Get Voltages”. The function returns a 16-bit value divided in Hi-Byte (MSB) and Lo-Byte (LSB).

Table 4-41: BMC Voltage Monitor Values

ADC Channel	Voltage Name	Voltage Formula [V]
0	VCC_CORE	(MSB<<8 + LSB) * 3.3 / 1024
1	VGG_S3	(MSB<<8 + LSB) * 3.3 / 1024
2	V1P05_A	(MSB<<8 + LSB) * 3.3 / 1024
3	VDDQ	(MSB<<8 + LSB) * 3.3 / 1024
4	VRTC	(MSB<<8 + LSB) * 3.3 / 1024
5	V3P3_S	(MSB<<8 + LSB) * 1.1 * 3.3 / 1024
6	V3P3_A	(MSB<<8 + LSB) * 1.1 * 3.3 / 1024
7	VNN_A	(MSB<<8 + LSB) * 3.3 / 1024
8	V1P15_S	(MSB<<8 + LSB) * 3.3 / 1024
9	V1P24_A	(MSB<<8 + LSB) * 3.3 / 1024
10	V1P8_A	(MSB<<8 + LSB) * 3.3 / 1024
11	V5VSB	(MSB<<8 + LSB) * 1.826 * 3.3 / 1024
12	Q7	(MSB<<8 + LSB) * 2.2 * 3.3 / 1024

Main Current

The BMC of the Q7-BW implements a Current Monitor. The current can be read by calling the SEMA function “Get Main Current”. The function returns four 16-bit values divided in Hi-Byte (MSB) and Lo-Byte (LSB). These four values represent the last four currents drawn by the board. The values are sampled every 250ms. The order of the four values is NOT in relationship to time. The access to the BMC may increase the drawn current of the whole system. In this case, you still have three samples without the influence of the read access.

Main Current = (MSB_n<<8 + LSB_n) * 8.06mA

TS#-Events

TS# is activated by a temperature sensor when a device reaches its critical temperature and released when the device is back in its normal temperature range. This counter gives the user information about temperature or cooling issues. This counter is cleared when the system is removed from power. The Q7-BW only monitors the board temperature and does not support TS#-Events.

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Exception Blink Codes

In the case of an error, the BMC shows a blink code on the STATUS-LED (LED1). This error code is also reported by the BMC Flags register. The Exception Code is not stored in the Flash storage and is cleared when the power is removed. Therefore, the “Clear Exception Code”-Command is not supported.

Table 4-42: Blink Codes

Exception Blink Code	Error Message
0	NOERROR
2	NO_SUSCLK
3	NO_SLP_S5
4	NO_SLP_S3
5	NO_PWGIN_5V
6	BIOS_FAIL
7	RESET_FAIL
8	RESETIN_FAIL
9	CRITICAL_TEMP
10	POWER_FAIL
11	VOLTAGE_FAIL
12	NO_V3P3_PRIME_PG
13	NO_V3P3A_PG
14	NO_VDDQ_PG
15	NO_VCC_CORE_PG
16	NO_V3P3S_PG

POWER_FAIL

The BMC Flags register returns the last detected exception code since power up.

4.3 Watchdog Timer

The Q7-BW features three separate Watchdog Timers. One of them is integrated in the SoC and two are provided by the BMC (managed by the SEMA).

The SoC Watchdog can be configured in the BIOS or by programming the Watchdog registers. If this function is used by user application, the application has to provide all logging functionality if desired.

4.4 Temperature Sensors

The Q7-BW supports two temperature sensor functions. One is offered from the SoC and one from a dedicated chip (Texas Instruments LM73) on the board.

The SoC temperature sensors can be configured by programming the appropriate SoC registers. Refer to the Thermal Management chapter in the N-series Intel processor data sheet for more information. The on-board LM73 temperature sensor is managed by the BMC and is configured through the SEMA utility.

4.5 Programming Examples

Programming examples can be provided based on a Linux operating system, upon request.

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Appendix A Technical Support

ADLINK Technology, Inc. provides a number of methods for contacting Technical Support listed in Table A-1 below. Requests for support through Ask an Expert are given the highest priorities, and usually will be addressed within one working day.

- ADLINK Ask an Expert – This is a comprehensive support center designed to meet all your technical needs. This service is free and available 24 hours a day through the ADLINK web site at http://www.adlinktech.com/AAE/. This includes a searchable database of Frequently Asked Questions, which will help you with the common information requested by most customers. This is a good source of information to look at first for your technical solutions. However, you must register online if you wish to use the Ask a Question feature.

ADLINK strongly suggests that you register with the web site. By creating a profile on the ADLINK web site, you will have a portal page called “My ADLINK”, unique to you with access to exclusive services and account information.

- Personal Assistance – You may also request personal assistance by creating an Ask an Expert account and then going to the Ask a Question feature. Requests can be submitted 24 hours a day, 7 days a week. You will receive immediate confirmation that your request has been entered. Once you have submitted your request, you must log in to go to the My Question area where you can check status, update your request, and access other features.
- Download Service – This service is also free and available 24 hours a day at http://www.adlinktech.com. For certain downloads such as technical documents and software, you must register online before you can log in to this service.

Table A-1: Technical Support Contact Information

Method	Contact Information
Ask an Expert	http://www.adlinktech.com/AAE/
Web Site	http://www.adlinktech.com
Standard Mail	**ADLINK Technology, Inc.** Address: 9F, No.166 Jian Yi Road, Zhonghe District New Taipei City 235, Taiwan 新北市中和區建一路 166 號 9 樓 Tel: +886-2-8226-5877 Fax: +886-2-8226-5717 Email: service@adlinktech.com **Ampro ADLINK Technology, Inc.** Address: 5215 Hellyer Avenue, #110 San Jose, CA 95138, USA Tel: +1-408-360-0200 Toll Free: +1-800-966-5200 (USA only) Fax: +1-408-360-0222 Email: info@adlinktech.com **ADLINK Technology (China) Co., Ltd.** Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203) 300 Fang Chun Rd., Zhangjiang Hi-Tech Park Pudong New Area, Shanghai, 201203 China Tel: +86-21-5132-8988 Fax: +86-21-5132-3588 Email: market@adlinktech.com

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Table A-1: Technical Support Contact Information (Continued)

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1 Shang Di East Rd.
Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8626
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园
A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

LiPPERT ADLINK Technology GmbH
Address: Hans-Thoma-Strasse 11
D-68163 Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

PENTA ADLINK Technology GmbH
Ulrichsbergerstrasse 17
94469 Deggendorf, Germany
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Fax: +49 (0) 991 290 94 - 29
Email: emea@adlinktech.com

ADLINK Technology, Inc. (French Liaison Office)
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91940 Les Ulis, France
Tel: +33 (0) 1 60 12 35 66
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Email: france@adlinktech.com

ADLINK Technology Japan Corporation
Address: 〒101-0045 東京都千代田区神田鍛冶町 3-7-4
神田 374 ビル 4F
KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
Chiyoda-ku, Tokyo 101-0045, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5209-6013
Email: japan@adlinktech.com

ADLINK Technology, Inc. (Korean Liaison Office)
Address: 경기도 성남시 분당구 수내로 46 번길 4 경동빌딩 2 층
(수내동 4-4 번지) (우) 463-825
2F, Kyungdong B/D, 4 Sunae-ro 46 beon-gil
Bundang-gu, Seongnam-si, Gyeonggi-do, Korea, 13595
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Email: korea@adlinktech.com

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Table A-1: Technical Support Contact Information (Continued)

	ADLINK Technology Singapore Pte. Ltd. Address: 84 Genting Lane #07-02A, Cityneon Design Centre Singapore 349584 Tel: +65-6844-2261 Fax: +65-6844-2263 Email: singapore@adlinktech.com **ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)** Address: #50-56, First Floor, Spearhead Towers Margosa Main Road (between 16th/17th Cross) Malleswaram, Bangalore - 560 055, India Tel: +91-80-65605817, +91-80-42246107 Fax: +91-80-23464606 Email: india@adlinktech.com **ADLINK Technology, Inc. (Israeli Liaison Office)** Address: 27 Maskit St., Corex Building PO Box 12777 Herzliya 4673300, Israel Tel: +972-54-632-5251 Fax: +972-77-208-0230 Email: israel@adlinktech.com **ADLINK Technology, Inc. (UK Liaison Office)** Tel: +44 774 010 59 65 Email: UK@adlinktech.com

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