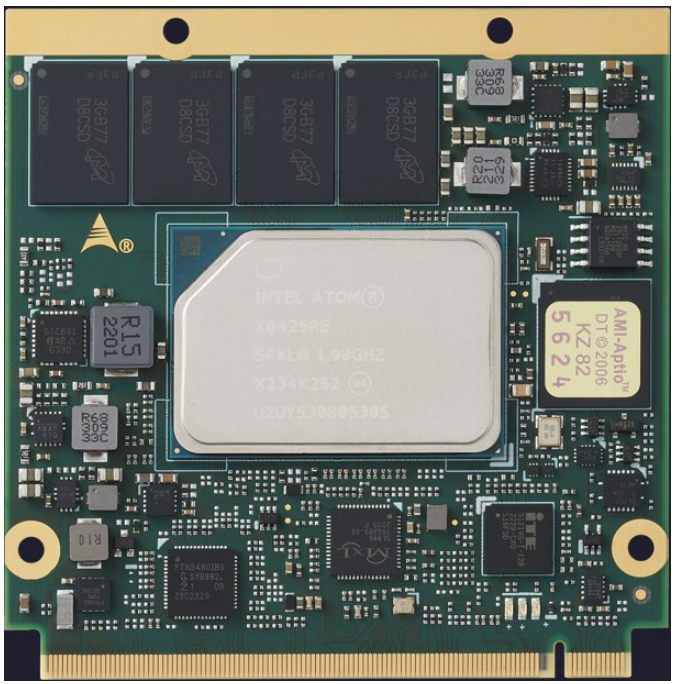
Q7-EL

User's Guide

intel



Revision: Rev. 1.0
Date: 2024-09-02
Part Number: 50M-76005-1000

ADLINK
LEADING EDGE COMPUTING

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Revision History

Revision	Description	Date	Author
1.0	Initial release	2024-09-02	AL

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Preface

Disclaimer

Information in this document is provided in connection with ADLINK products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in ADLINK´s Terms and Conditions of Sale for such products, ADLINK assumes no liability whatsoever, and ADLINK disclaims any express or implied warranty, relating to sale and/or use of ADLINK products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. If you intend to use ADLINK products in or as medical devices, you are solely responsible for all required regulatory compliance, including, without limitation, Title 21 of the CFR (US), Directive 2007/47/EC (EU), and ISO 13485 & 14971, if any. ADLINK may make changes to specifications and product descriptions at any time, without notice.

Environmental Responsibility

ADLINK is committed to fulfil its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

California Proposition 65 Warning: This product can expose you to chemicals including acrylamide, arsenic, benzene, cadmium, Tris(1,3-dichloro-2-propyl)phosphate (TDCPP), 1,4-Dioxane, formaldehyde, lead, DEHP, styrene, DINP, BBP, PVC, and vinyl materials, which are known to the State of California to cause cancer, and acrylamide, benzene, cadmium, lead, mercury, phthalates, toluene, DEHP, DIDP, DnHP, DBP, BBP, PVC, and vinyl materials, which are known to the State of California to cause birth defects or other reproductive harm. For more information go to www.P65Warnings.ca.gov.

Trademarks

Product names mentioned herein are used for identification purposes only and may be trademarks / registered trademarks of respective companies.

Copyright © 2024 ADLINK Technology Incorporated

This document contains proprietary information protected by copyright. All rights are reserved. No part of this manual may be reproduced by any mechanical, electronic, or other means in any form without prior written permission of the manufacturer.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Safety Instructions

For user safety, please read and follow all Instructions, **WARNING**s, **CAUTION**s, and **NOTE**s marked in this manual and on the associated equipment before handling/operating the equipment. Read these safety instructions carefully.

- Keep this manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- Turn off power and unplug any power cords/cables when installing/mounting or un-installing/removing equipment.
- To avoid electrical shock and/or damage to equipment:
- Keep equipment away from water or liquid sources;
- Keep equipment away from high heat or high humidity;
- Keep equipment properly ventilated (do not block or cover ventilation openings);
- Make sure to use recommended voltage and power source settings;
- Always install and operate equipment near an easily accessible electrical socket outlet;
- Secure the power cord (do not place any object on/over the power cord);
- Only install/attach and operate equipment on stable surfaces and/or recommended mountings;
- If the equipment will not be used for long periods of time, turn off the power source and unplug the equipment.

Conventions

The following conventions may be used throughout this manual, denoting special levels of information.

Note: This information adds clarity or specifics to text and illustrations.

Caution: This information indicates the possibility of minor physical injury, component damage, data loss, and/or program corruption.

Warning: This information warns of possible serious physical injury, component damage, data loss, and/or program corruption.

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Getting Service

Ask an Expert: https://www.adlinktech.com/en/Askanexpert

ADLINK Technology, Inc.
No. 66, Huaya 1st Rd., Guishan District, Taoyuan City 333411, Taiwan
Tel: +886-3-216-5088
Fax: +886-3-328-5706
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
6450 Via Del Oro, San Jose, CA 95119-1208, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-600-1189
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
300 Fang Chun Rd., Zhangjiang Hi-Tech Park, Pudong New Area, Shanghai, 201203, China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology GmbH
Hans-Thoma-Strasse 11, D-68163 Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

Please visit the Contact page at www.adlinktech.com for information on how to contact the ADLINK regional office nearest you.

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table of Contents

Revision History 2
Preface 3
List of Figures 8
1. Introduction 9
2. Specifications 10
2.1. Core System 10
2.2. Display Interface Support 11
2.2.1 Display Port 12
2.3. Audio 12
2.4. Expansion Busses 13
2.5. PCI Express Bus 13
2.6. Ethernet 13
GPY 211 13
2.7. Multi I/O and Storage 14
2.8. BIOS 16
2.9. Debug 16
2.10. Power 16
2.11. Mechanical and Environmental 17
3. Block Diagram 18
4. Pinout and Signal descriptions 19
4.1. Signal Terminology Definitions 19
4.2. Signal Description by function 20
4.2.1 GPIO 20
4.2.2 Board to Board Connector 21
4.2.3 Debug Card Connector (DB40) 26
5. Additional Features 29
5.1. LED Status Indicator 29
5.1.1 Power LED（Green LED） 29
5.1.2 Status LED（Blue LED） 29
5.1.3 WDT LED（Red LED） 29
6. Mechanical 30

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

6.1. Module Dimensions (preliminary) 30
7. Thermal Solutions 32
7.1. Heat spreader 32
7.2. Low Profile Heatsink 32

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

List of Figures

Figure 1 – Module function diagram....18
Figure 2 – Module dimensions (top) 30
Figure 3 – Module dimensions (bottom....31

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1. Introduction

The Q7-EL is a QSeven form factor and revision 2.1 compliant computer-on-module that is fully compliant with the SGET (Standardization Group for Embedded Technologies) standards.

Qseven modules are very compact, highly integrated computers. The core of the Q7-EL is the Elkhart Lake SoC, which integrates the next generation Intel® processor core, graphics, LPDDR4 memory controller, and I/O interfaces into a single system-on-chip solution. The Q7-EL also includes contemporary high bandwidth interface such as PCI Express, USB2.0, USB3.0, 2.5 Gigabit Ethernet, SATA etc. It also features Audio, HDMI, LVDS,on board EMMC, SATA SSD, and more.

In addition, an optional fail-safe BIOS implemented to enable the user to start the module even if the original BIOS is corrupted.

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2. Specifications

2.1. Core System

CPU

Elkhart Lake SoC, chip package, size 24 x 35 mm, 10nm Compute Die and 14nm PCH Die on single package, 1493 Pin, Type 3 BGA, 0.593 mm ball pitch.

Intel Elkhart lake SOC is a 64-bit, multi-core processor built on 10-nanometer technology.
The processor supports the following technologies and interfaces:
•LPDDR4
•DDI
•PCI Express
•SATA3.0
•USB2.0/3.0
•eMMC
•SD
•SPI
•I2C
•HDA

Memory

Memory controller supports single and dual channel LPDDR4@3200, 4267 with IBECC •4x 32-bit data bus LPDDR4 DRAM •Total memory capacity of 2GByte, 4 GByte, 8 GByte and 16 Gbyte (memory down)

The design supports following memory configuarations:

2 GByte: 2x 8Gbit (single channel)

4 GByte: 2x 16Gbit (single channel)

4 GByte: 4x 8Gbit (dual channel)

8 GByte: 4x 16Gbit (four channel)

16 GByte: 4x 32Gbit (four channel)

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Embedded BIOS
AMI EUFI with CMOS backup in 8MB SPI BIOS with Intelx2

2.2. Display Interface Support

eDP to LVDS(PTN3460): Via BOM option eDP to LVDS port.

The PTN3460 is the display port to LVDS converter.
- 2-Lane Display Port receiver
- 2-Port LVDS output interface

Max. resolution up to 1920x1200x60(RB), 18-bit color depth
QFN-56 Pin package

LVDS BOM option:

Primary Display

1x single or dual channel LVDS, 18/24 bit resolutions up to 1920x1080 (convert eDP with NXP transceiver PTN3460IBS)

Secondary Display

1x DisplayPort

Tertiary Display

1x DisplayPort or 1x HDMI

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

eDP BOM option:

Primary Display

1x eDP

Secondary Display

1x DisplayPort

Tertiary Display
1x DisplayPort or 1x HDMI

2.2.1 Display Port

DisplayPort support resolutions up to 4096 × 2160@60 Hz, with SSC, max data rate 5.4 GT/s Standard Version 1.2.

DP++ Operation Over HDMI
DP++ or DisplayPort++ (also named as Dual-mode DisplayPort) can directly output HDMI and DVI signals. The level adaptation can be implemented on the Carrier or via plug in cable adapter. In case of carrier board implementation, a level shifter adjusts the I/O voltage to HDMI/DVI compliant signal levels. A dual-mode chipset switches to DVI/HDMI mode (4-lane main DisplayPort link and AUX channel) if a DVI or HDMI passive adapter is detected (by DP0_AUX_SEL).

2.3. Audio

The Q7-EL support Intel High Definition Audio interface that supports audio codecs only. The controller communicates with the internal/external CODECs over the Intel® HD Audio serial link. The link can only operate at 3.3 V. With the support of multi-channel audio stream, 32-bit sample depth, and sample rate of up to 192 kHz, the Intel HD Audio controller provides audio quality that can deliver CE levels of audio experience.

1x High-Definition Audio (HDA)

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.4. Expansion Busses

4x PCIe x1, including all support signals, clock, wake signal.

2.5. PCI Express Bus

There are four lanes and up to four PCI Express root ports, each supporting the PCI Express* Base Specification, Rev. 3.0 at a maximum 8GT/s signaling rate. The root ports can be configured to support a diverse set of lane assignments.

2.6. Ethernet

GPY 211

The Ethernet Network Connection GPY211 is a low power Ethernet PHY transceiver integrated circuit. It offers a cost-optimized solution that is well-suited for routers, switches, and home gateways. It performs the data transmission on an Ethernet twisted pair copper cable of category CAT5e or higher. Four data rates are supported: 2500, 1000, 100, and 10 Mbit/s.

2x Ethernet PHY GPY211/GPY215 support LED signals

Q7-EL has 1 Gigabit Ethernet port which provides:

- IEEE 802.3az Energy Efficient Ethernet
- IEEE 1588/802.1AS precision time synchronization
- IEEE 802.3Qav traffic shaper
- Interrupt moderation, VLAN support, IP checksum offload
- PCIe OBFF (Optimized Buffer Flush/Fill) for improved system power management

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

- Four transmission and four reception queues
- RSS and MSI-X to lower CPU utilization in multi-core systems
- ECC - error correcting memory in packet buffers
- Wake-On-LAN
- NC-SI for increased bandwidth passthrough
- Preboot eXecution Environment (PXE) flash interface
- Jumbo frame support

2.7. Multi I/O and Storage

USB

- 2x USB3.1 gen2 host
- 1x USB2.0 OTG (port0)
- 5x USB2.0 host

USB Mapping: MXM2 connector side connected to Q7-EL SoC side

USB0	<->	USB2.0_Port-0 (host)
USB1	<->	USB2.0_Port-1 (host)
USB2	<->	USB2.0_Port-2 (host)

USB 3.0/2.0

The Q7-EL support six USB2.0 ports and two USB3.0 ports. USB2.0 port can be used to connect to high-speed, full-speed, and low-speed USB devices via xHCI controller. USB3.0 port has an xHCI controller and xDCI controller implemented in it.

SATA

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

The Q7-EL has one integrated SATA host controller that supports DMA ports and supports data transfer rates of Gen 1 (1.5 Gb/s), Gen 2 (3 Gb/s), and SATA Gen 3 (6 Gb/s). The SATA controllers are completely software transparent with an AHCI interface, while providing a lower pin count and higher performance than the legacy parallel ATA interface.

2x SATA3 SATA III 6.0 Gb/s to carrier

GPIO

8x interrupt capable GPIO (shared pins with LPC, non-default BOM option)
8x GPIO from BMC to MXM2 connector
Qseven standard supports 8x GPIO in total

SD Card

1x SDIO 3.0 (4bit)

SPI

The SPI flash controller supports running instructions at 20Mbps, 33Mbps, or 50 Mbps and can be used by BIOS code to provide chipset configuration settings, internal micro-processor code, and configurations. It also supports the Serial Flash Discoverable Parameter (SFDP) JEDEC standard, which provides a consistent way of describing the functional and feature capabilities of serial flash devices through a standard set of internal parameter tables. The SPI flash controller supports up to two SPI Flash devices using two separate chip select pins, with each SPI Flash device can be up to 16 MB.

1x SPI to MXM connector

I2C

1x I2C to MXM

UART

1x UART, two with 2 wire handshake

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.8. BIOS

AMI EUFI with CMOS backup in 8MB SPI BIOS with Intelx2

2.9. Debug

1x LPC connects to DB40 debug connector

2.10. Power

Standard Voltage Input: 4.75V - 5.25V DC

Power Management:

Power States: Supporting C1-C2, S0, S3, S4/S5 (both shutdown by SoC)

- Wake S4/S5 is not supported
- Wake S3 by USB / WOL / WAKE signal

ATX and AT mode and ECO mode are supported.

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.11. Mechanical and Environmental

Form Factor and specification

Qseven® Standard Size Module Rev 2.1, Basic Size 70 mm x 70 mm

Operating Temperature

Standard	0°C to 60°C
Extreme Rugged	-40°C to 85°C

Humidity

5-90% RH operating, non-condensing
5-95% RH storage (operating with conformal coating).

EMI

EN55022 Class B inside an enclosure

Shock and Vibration

HALT testing report confirms the extended operating temperature range during and after vibration. There is a separate shock test report to MIL-STD-202F, Method 213B, Table 213-I, Condition A.

IN ADDITION: When installed on a baseboard, it shall operate under 18 saw-tooth mechanical shocks (3 shocks in each direction) with a peak acceleration of 40g for a duration of 18milliseconds each and 75g for a duration of 6milliseconds each. It is capable of supporting random vibrations: MIL-STD-202F, Method 214A, Table 214-I, Condition D. If HALT testing shows equal or better performance, a separate vibration test report is not necessary.

MTBF

250,000 hrs. commercial 40°C ambient (according MIL calculation) based on actual calculated de-rating

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3. Block Diagram

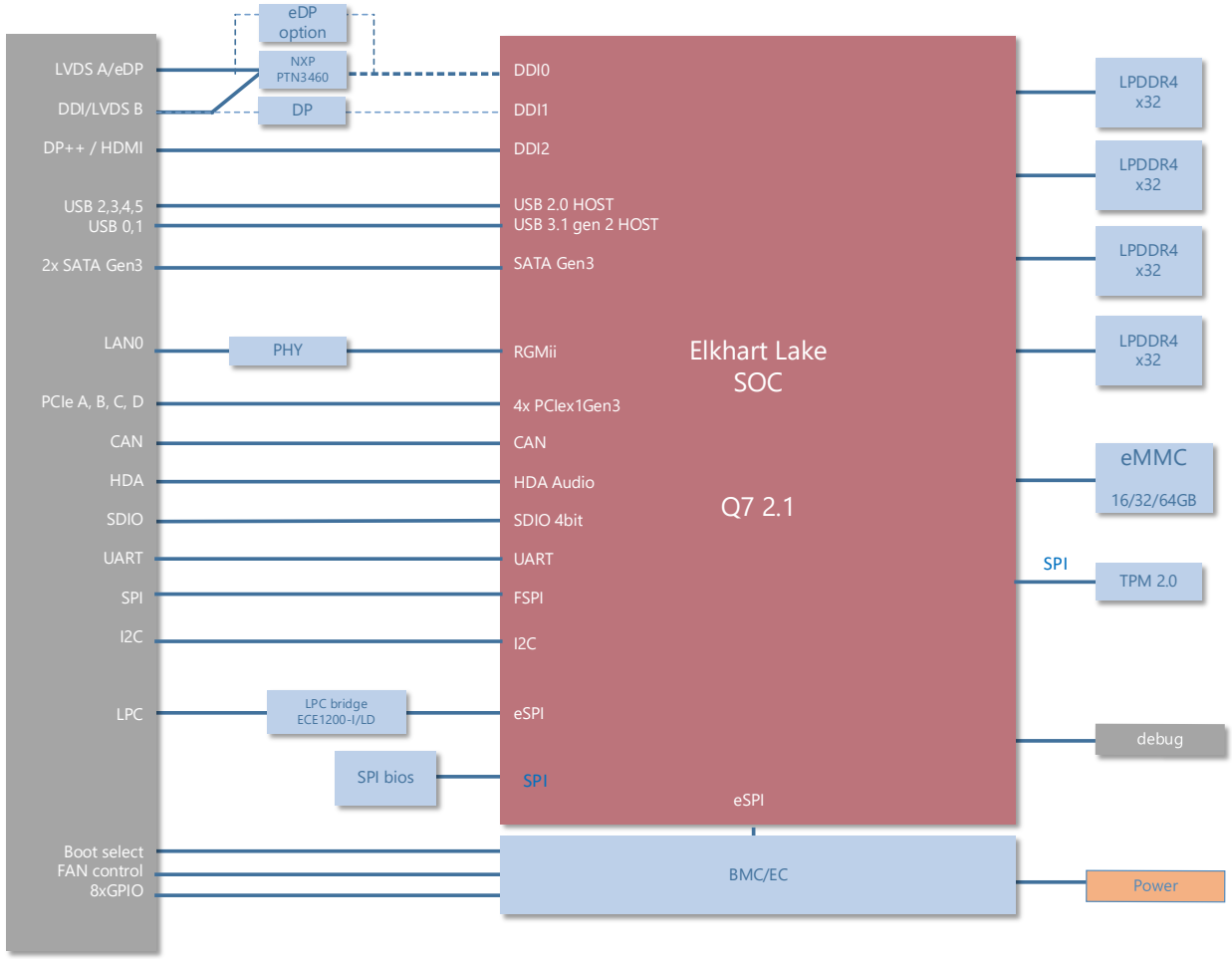


Figure 1 – Module function diagram

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4. Pinout and Signal descriptions

4.1. Signal Terminology Definitions

The following information provides descriptions of the terms used in the signal description table:

Term	Description
I	Input to the Module
O	Output from the Module
I/O	Bi-directional input / output signal
OD	Open drain output
P_+3V3_BMC_A	S5 power P_+3V3_BMC_A tolerant
P_+3V3_A	S5 power P_+3V3_A tolerant
P_+1V5_A	S5 power P_+1V5_A tolerant
P_+1V24_A	S5 power P_+1V24_A tolerant
P_+1V8_A	S5 power P_+1V8_A tolerant
P_+1V05_S0	S0 power P_+1V05_S0 tolerant
P_+3V3_S0	S0 power P_+3V3_S0 tolerant
P_+1V8_S0	S0 power P_+1V8_S0 tolerant
P	Power Input/Output
REF	Reference voltage output
PU	ADLINK implemented pull-up resistor on module
PD	ADLINK implemented pull-down resistor on module
P_+VQ7	Module power input

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.2. Signal Description by function

4.2.1 GPIO

All GPIOs are driven by the BMC according to the Qseven specification.
GPIO0-7 are multiplexed with low pin count. Low pin count is the recommended default setup.

Signal Name	Direction	Direction Preferred	Type / Tolerance	GPIO Use	Sanctioned Alternate Uses
GPIO0 / LPC_AD0	Bi -Dir	Output	CMOS 3.3V	GPIO0	LPC Data 0
GPIO1 / LPC_AD1	Bi -Dir	Output	CMOS 3.3V	GPIO1	LPC Data 1
GPIO2 / LPC_AD2	Bi -Dir	Output	CMOS 3.3V	GPIO2	LPC Data 2
GPIO3 / LPC_AD3	Bi -Dir	Output	CMOS 3.3V	GPIO3	LPC Data 3
GPIO4 / LPC_CLK0	Bi -Dir	Output	CMOS 3.3V	GPIO4	LPC clock
GPIO5 / LPC_FRAME-L	Bi -Dir	Output	CMOS 3.3V	GPIO5	LPC frame indicates the start of a new cycle or the termination of a broken cycle.
GPIO6 / LPC_SERIRQ	Bi -Dir	Output	CMOS 3.3V	GPIO6	Serialized Interrupt.
GPIO7	Bi -Dir	Output	CMOS 3.3V	GPIO7	N/A

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.2.2 Board to Board Connector

Primary side (BOTTOM)			Secondary side (TOP)		
Pin#	**Signal**	**PU/PD**	**Pin#**	**Signal**	**PU/PD**
1	GND		2	GND	
3	GBE_MDI3-		4	GBE_MDI2-	
5	GBE_MDI3+		6	GBE_MDI2+	
7	GBE_LINK100#		8	GBE_LINK1000#	
9	GBE_MDI1-		10	GBE_MDI0-	
11	GBE_MDI1+		12	GBE_MDI0+	
13	GBE_LINK#		14	GBE_ACT#	
15	GBE_CTREF		16	SUS_S5#	
17	WAKE#		18	SUS_S3#	
19	GPO0		20	PWRBTN#	
21	SLP_BTN# / GPII1		22	LID_BTN# / GPII0	
23	GND		24	GND	
Key			Key		
25	GND		26	PWGIN	
27	BATLOW#		28	RSTBTN#	
29	SATA0_TX+		30	SATA1_TX+	
31	SATA0_TX-		32	SATA1_TX+	
33	SATA_ACT#		34	GND	
35	SATA0_RX+		36	SATA1_RX+	
37	SATA0_RX-		38	SATA1_RX-	
39	GND		40	GND	
41	BI-OS_DISABLE#/BOOT_ALT#		42	SDIO_CLK#	
43	SDIO_CD#		44	SDIO_LED	
45	SDIO_CMD		46	SDIO_WP	
47	SDIO_PWR#		48	SDIO_DAT1	

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Primary side (BOTTOM)			Secondary side (TOP)		
Pin#	**Signal**	**PU/PD**	**Pin#**	**Signal**	**PU/PD**
49	SDIO_DAT0		50	SDIO_DAT3	
51	SDIO_DAT2		52	reserved	
53	reserved		54	reserved	
55	reserved		56	USB_OTG_VBUS	
57	GND		58	GND	
59	HDA_SYNC / I2S_WS		60	SMB_CLK/GP1_I2C_CLK	
61	HDA_RST# / I2S_RST# /		62	SMB_DAT/GP1_I2C_DAT	
63	HDA_BCLK / I2S_BCLK /		64	SMB_ALERT#	
65	HDA_SDI / I2S_SDI /		66	GP0_I2C_CLK	
67	HDA_SDO / I2S_SDO /		68	GP0_I2C_DAT	
69	THRM#		70	WDTRIG#	
71	THRMTRIP#		72	WDOUT	
73	GND		74	GND	
75	USB_P7- /USB_SSTX0-		76	USB_P6- /USB_SSRX0-	
77	USB_P7+ /USB_SSTX0+		78	USB_P6+/USB_SSRX0+	
79	USB_6_7_OC#		80	USB_4_5_OC#	
81	USB_P5- / USB_SSTX1-		82	USB_P4- / USB_SSRX1-	
83	USB_P5+ / USB_SSTX1+		84	USB_P4+ / USB_SSRX1+	
85	USB_2_3_OC#		86	USB_0_1_OC#	
87	USB_P3-		88	USB_P2-	
89	USB_P3+		90	USB_P2+	
91	USB_CC		92	USB_ID	

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Primary side (BOTTOM)			Secondary side (TOP)		
Pin#	**Signal**	**PU/PD**	**Pin#**	**Signal**	**PU/PD**
93	USB_P1-		94	USB_P0-	
95	USB_P1+		96	USB_P0+	
97	GND		98	GND	
99	eDP0_TX0+ / LVDS_A0+		100	eDP1_TX0+ / LVDS_B0+	
101	eDP0_TX0- / LVDS_A0-		102	eDP1_TX0- / LVDS_B0-	
103	eDP0_TX1+ / LVDS_A1+	PU, 470k, V1P8S	104	eDP1_TX1+ / LVDS_B1+	
105	eDP0_TX1- / LVDS_A1-	PU, 470k, V1P8S	106	eDP1_TX1- / LVDS_B1-	
107	eDP0_TX2+ / LVDS_A2+	PU, 470k, V1P8S	108	eDP1_TX2+ / LVDS_B2+	
109	eDP0_TX2- / LVDS_A2-	PU, 470k, V1P8S	110	eDP1_TX2- / LVDS_B2-	
111	LVDS_PPEN	PU, 470k, V1P8S	112	LVDS_BLEN	
113	eDP0_TX3+ / LVDS_A3+	PU, 470k, V1P8S	114	eDP1_TX3+ / LVDS_B3+	
115	eDP0_TX3- / LVDS_A3-	PU, 470k, V1P8S	116	eDP1_TX3- / LVDS_B3-	
117	GND		118	GND	
119	eDP0_AUX+ / LVDS_A_CLK+		120	eDP1_AUX+ / LVDS_B_CLK+	
121	eDP0_AUX- / LVDS_A_CLK-		122	eDP1_AUX- / LVDS_B_CLK-	
123	LVDS_BLT_CTRL/GP _PWM_OUT0		124	GP_1-Wire_Bus/ HDMI_CEC	
125	GP2_I2C_DAT / LVDS_DID_DAT		126	eDP0_HPD# / LVDS_BLC_DAT	
127	GP2_I2C_CLK / LVDS_DID_CLK		128	eDP1_HPD# / LVDS_BLC_CLK	

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Primary side (BOTTOM)			Secondary side (TOP)		
Pin#	**Signal**	**PU/PD**	**Pin#**	**Signal**	**PU/PD**
129	CAN0_TX		130	CAN0_RX	
131	DP_LANE3+ / TMDS_CLK+		132	USB_SSTX1-	
133	DP_LANE3- / TMDS_CLK-		134	USB_SSTX1+	
135	GND		136	GND	
137	DP_LANE1+ / TMDS_LANE1+		138	DP_AUX+	
139	DP_LANE1- / TMDS_LANE1-		140	DP_AUX-	
141	GND		142	GND	
143	DP_LANE2+ / TMDS_LANE0+		144	USB_SSRX1-	
145	DP_LANE2- / TMDS_LANE0-		146	USB_SSRX1+	
147	GND		148	GND	
149	DP_LANE0+ / TMDS_LANE2+		150	HDMI_CTRL_DAT	
151	DP_LANE0- / TMDS_LANE2-		152	HDMI_CTRL_CLK	
153	DP_HDMI_HPD#		154	DP_HDP#	
155	PCIE_CLK_REF+		156	PCIE_WAKE#	
157	PCIE_CLK_REF-		158	PCIE_RST#	
159	GND		160	GND	
161	PCIE3_TX+		162	PCIE3_RX+	
163	PCIE3_TX-		164	PCIE3_RX-	
165	GND		166	GND	
167	PCIE2_TX+		168	PCIE2_RX+	
169	PCIE2_TX-		170	PCIE2_RX-	
171	UART0_TX		172	UART0_RTS#	

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Primary side (BOTTOM)			Secondary side (TOP)		
Pin#	**Signal**	**PU/PD**	**Pin#**	**Signal**	**PU/PD**
173	PCIE1_TX+		174	PCIE1_RX+	
175	PCIE1_TX-		176	PCIE1_RX-	
177	UART0_RX		178	UART0_CTS#	
179	PCIE0_TX+		180	PCIE0_RX+	
181	PCIE0_TX-		182	PCIE0_RX-	
183	GND		184	GND	
185	LPC_AD0 / GPIO0		186	LPC_AD1 / GPIO1	
187	LPC_AD2 / GPIO2		188	LPC_AD3 / GPIO3	
189	LPC_AD4 / GPIO4		190	LPC_FRAME# / GPIO5	
191	SERIRQ / GPIO6		192	LPC_LDRQ# / GPIO7	
193	VCC_RTC		194	SPKR / GP_PWM_OUT2	
195	FAN_TACHOIN / GP_TIMER_IN		196	FAN_PWMOUT / GP_PWM_OUT1	
197	GND		198	GND	
199	SPI_MOSI		200	SPI_CS0#	
201	SPI_MISO		202	SPI_CS1#	
203	SPI_SCK		204	MFG_NC4	
205	VCC_5V_SB		206	VCC_5V_SB	
207	MFG_NC0		208	MFG_NC2	
209	MFG_NC1		210	MFG_NC3	
211	NC*		212	NC*	
213	NC*		214	NC*	
215	NC*		216	NC*	
217	NC*		218	NC*	
219	VCC		220	VCC	
221	VCC		222	VCC	

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Primary side (BOTTOM)			Secondary side (TOP)		
Pin#	Signal	PU/PD	Pin#	Signal	PU/PD
223	VCC		224	VCC	
225	VCC		226	VCC	
227	VCC		228	VCC	
229	VCC		230	VCC	

4.2.3 Debug Card Connector (DB40)

For information on LVDS support for a single-channel with 4 lanes, please refer to the details below:

Pin Number	Interface	Signals	Comments
1	SPI Program Interface	VCC_SPI_IN	SPI Power Input from flash tool to module P.S. HW need add MOS FET to switch SPI power for SPI ROM.
2		GND	
3		SPI_BIOS_CS0#	
4		SPI_BIOS_CS1#	
5		SPI_BIOS_MISO	
6		SPI_BIOS_MOSI	
7		SPI_BIOS_CLK	
8	LPC Debug card Interface	3V3_LPC	System power 3.3V provide from COM module
9		GND	
10		BIOS_DIS0	
11		RST#	
12		CLK33_LPC	
13		LPC_FRAME#	

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

14		LPC_AD3	
15		LPC_AD2	
16		LPC_AD1	always power 3.3V provide from COM module
17		LPC_AD0	
18	SMC Program interface	3.3V_SMC	always power 3.3V provide from COM module
19		3.3V_A	always power 3.3V provide from COM module
20		GND	
21		TXD6	
22		RXD6	
23		FUMD0	
24		RESET_IN#	
25		DATA	
26		CLK	
27		OCD0A	include a jumper to connect OCD0A via 1K0 pull-up to 3.3V_SMC
28		OCD0B	include a jumper to connect OCD0B via 1K0 pull-down to GND
29	Test point	PWRBTN#	
30		SYS_RESET#	
31		CB_RESET#	
32		CB_PWROK	
33		SUS_S3#	
34		SUS_S4#	
35		SUS_S5#	

Copyright © 2024 ADLINK Technology, Inc.
ADLINK LEADING EDGE COMPUTING
LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

36	For SMC Debug	POSTWDT_DIS#	Connect to Jumper for Debug
37		SEL_BIOS	Connect to Jumper for Debug
38		BIOS_MODE	Connect to Jumper for Debug
39		SMC_STATUS	Connect to LED
40	NC	RESVD	

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5. Additional Features

5.1. LED Status Indicator

5.1.1 Power LED（Green LED）

The Power LED that is controlled by SLP_S3# and should be light only in S0 state.

5.1.2 Status LED（Blue LED）

The Status LED is controlled by SEMA. The Status LED will signal system state changes and power up failures. The system state changes can be HW-Reset, SW-Reset, Power-Up, Power-Down, Reset-Button and Power-Button activity. The Status LED will light for short time. Power-Up failures can be a corrupted BIOS or failures at the onboard power supply. A blink code will be displayed in case of a failure. In S3 state, the Status LED will be displayed on by short periodic flashes for every 4sec.

5.1.3 WDT LED（Red LED）

The WDT LED is driven by SEMA and will light when a watchdog timeout occurs. It stays on as long till it is cleared by software or by reset button.

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

6. Mechanical

6.1. Module Dimensions

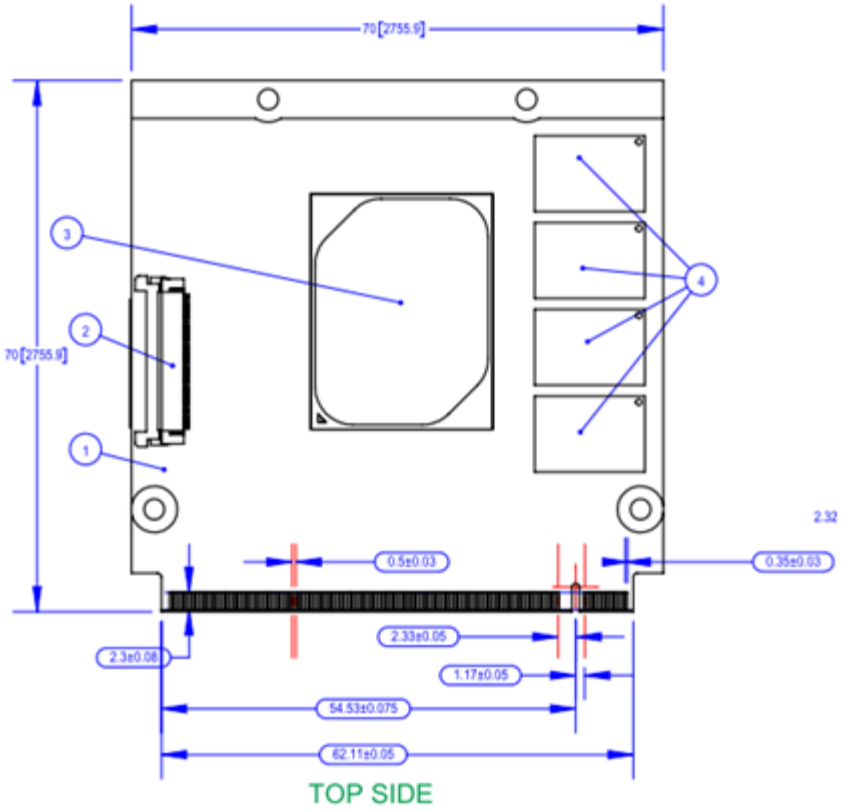


Figure 2 – Module dimensions (top)

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

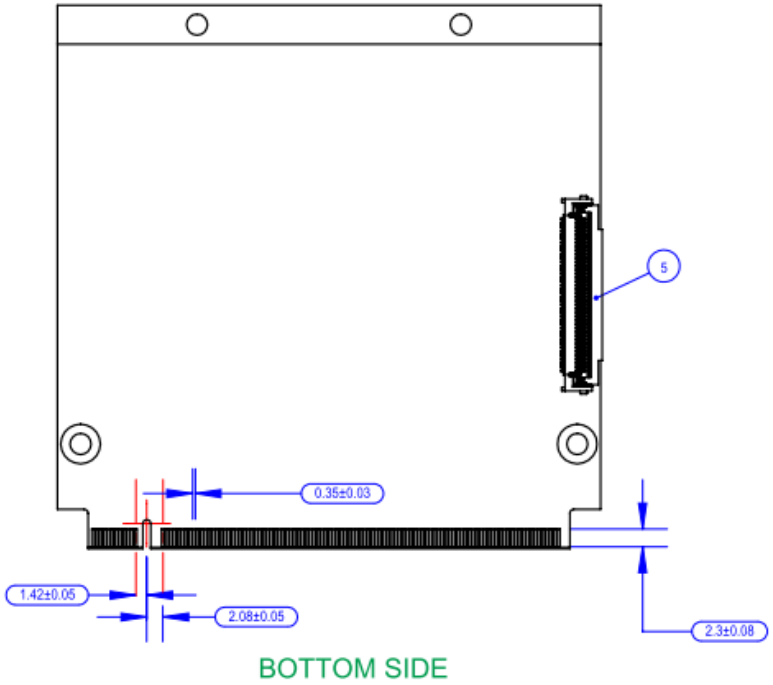


Figure 3 – Module dimensions (bottom

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7. Thermal Solutions

7.1. Heat spreader

One design / Dual Core / Low Power Quad Core

7.2. Low Profile Heatsink

Dual Core / Quad Core u pro 12W power dissipation（Top mounting with springs）

Copyright © 2024 ADLINK Technology, Inc.
Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000