

CG-OpenRack-19 Half-Width OpenSled Server Design Specification

Version 0.63

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1 Revision History

Date	Name	Description
11-28-2016	ADLINK Technology Inc.	Version 0.1 Content layout
12-16-2016	ADLINK Technology Inc.	Version 0.5 Draft for internal review
12-18-2016	ADLINK Technology Inc.	Version 0.6 Updates based on Mondo, Jeff discussions
12-19-2016	ADLINK Technology Inc.	Version 0.61 Updated B2B connectors and compute zone section.
1-6-2017	ADLINK Technology Inc.	Version 0.62 Added B2B connector positions.
1-16-2017	ADLINK Technology Inc.	Version 0.63 updated project name and provided additional input from sponsors

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3 License

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4 Scope

CG-OpenRack-19 OpenSled server is scalable carrier-grade rack level system that integrates high performance compute, storage and networking in a standard rack. As such, there are many possible system configurations. However, certain rules and requirements ensure that different modules will operate properly in compliant systems.

This document provides the detailed interoperability requirements of a CG-OpenRack-19 OpenSled server. This document describes the physical makeup of the OpenSled server with a focus on the board to board interfaces between the compute board and the mezzanine card. This includes mechanical requirements as well as requirements related to electrical power feeds, optical and electrical interfaces, airflow and cooling, and environmental robustness.

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5 Overview

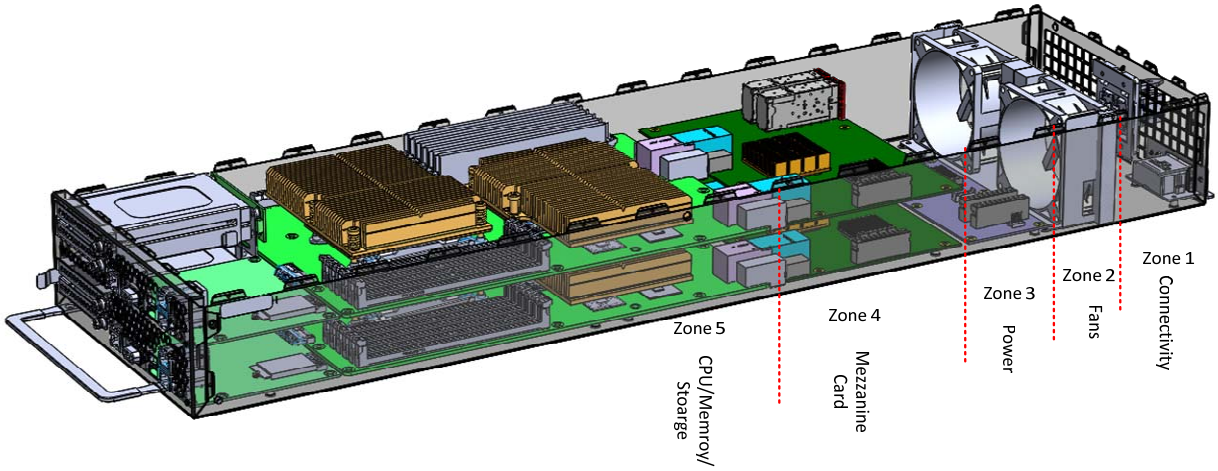
5.1 Overview

The OpenSled server is a half-width sled in the CG-OpenRack-19 form factor. The OpenSled server is constructed based on zones, which are partitioned chassis spaces that are reserved to implement different functionalities for the server.

- Zone 1: Defines the rear compartment (should be fairly open for air flow requirements), optical and power connectors.
- Zone 2: Defines the types of fans to be used in order to provide the required airflow for half-width sled.
- Zone 3: Defines the power specification for the half-width OpenSled server to support CPU/memory/storage, mezzanine, and fans.
- Zone 4: Defines the mezzanine card area for networking options.
- Zone 5: Defines the compute board size, shape and interconnectivity to mezzanine card.

The zone partition of OpenSled server makes it easier to upgrade the networking and computing capability independent of each other. In case that a higher bandwidth is required, the OpenSled server supports upgrading the mezzanine board alone. The reverse is also true. When upgrading the computing sled in accord with Intel update cycle, the other zones can be kept without any changes.

Figure 1. OpenSled Server with Different Functional Zones



5.2 CG-OpenRack-19 Introduction

CG-OpenRack-19 is scalable carrier-grade rack level system that integrates high performance compute, storage and networking in a standard rack. In general, the system is made up of compute and storage-centric sleds, Ethernet switches, a power source, and supporting rack infrastructure as shown in Figure 2.

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There are five major system component types: the system rack, power conversion/distribution, Top-of-Rack (ToR) switches, and two types of pluggable modules (sleds) which are differentiated by form factor (width).

- System Rack: The rack provides physical structure for the system, airflow control, security, and network interconnects.
- Power Source: Rack-mount power conversion and distribution infrastructure that provides a nominal 12VDC to two bus bar pairs mounted at the rear of the system.
- Half-Width Sled: A 2U enclosure that takes up half of the shelf width. A common use of this sled size is to provide high density compute resources.
- Full-Width Sled: A 2U enclosure that takes up the full shelf width. A common use of this sled size is to provide high capacity/throughput storage resources.
- Top-of-Rack (ToR) Switch: Each rack can be equipped with a variable number of management plane and data plane switches, also referred to as Top of Rack switches. Each of these aggregates management and/or data traffic to internal network switching planes.

Figure 2. Rack with Half-Width and Full-Width Sleds



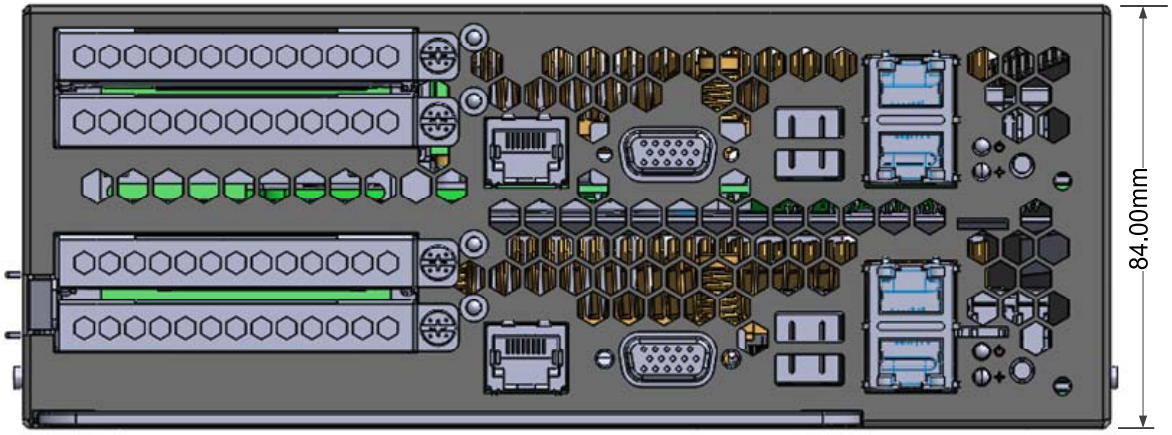
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6 OpenSled Server Physical Specification

6.1 OpenSled Server Mechanical Dimensions

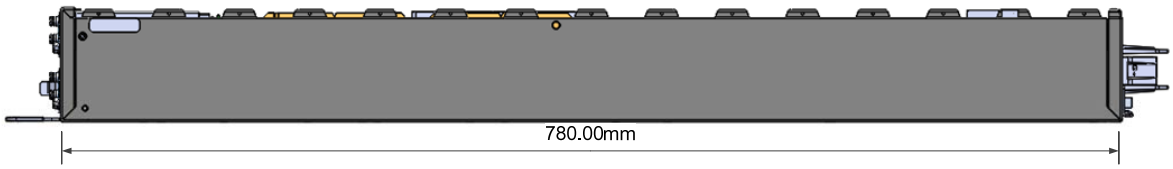
The OpenSled server occupies a vertical spacing of 2 Rack Units (RU). The vertical height from the bottom face to the top face is 84.00mm.

Figure 3. OpenSled Vertical Height (front view)



The OpenSled server has a horizontal depth of 780.00mm as measured from the front face to the rear face.

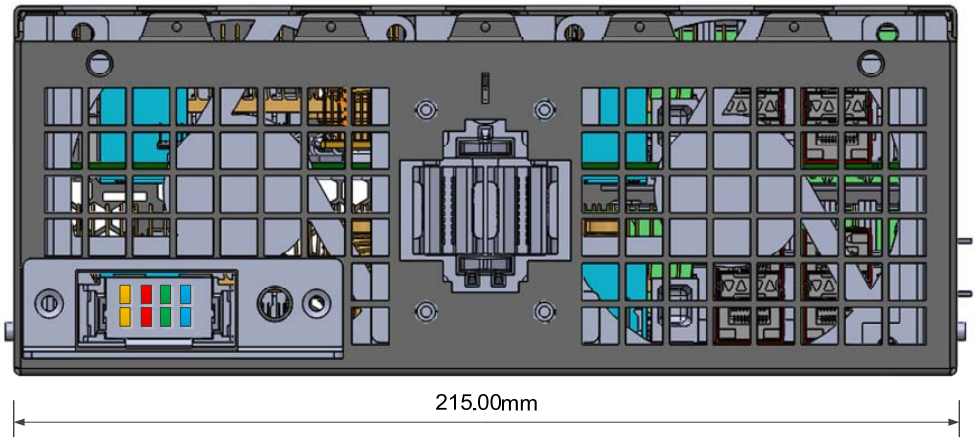
Figure 4. OpenSled Horizontal Depth (side view)



The OpenSled server has a horizontal width of 215.00mm as measured from the left face to the right face.

Figure 5. OpenSled Horizontal Width (rear view)

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6.2 OpenSled Server Zone Layout

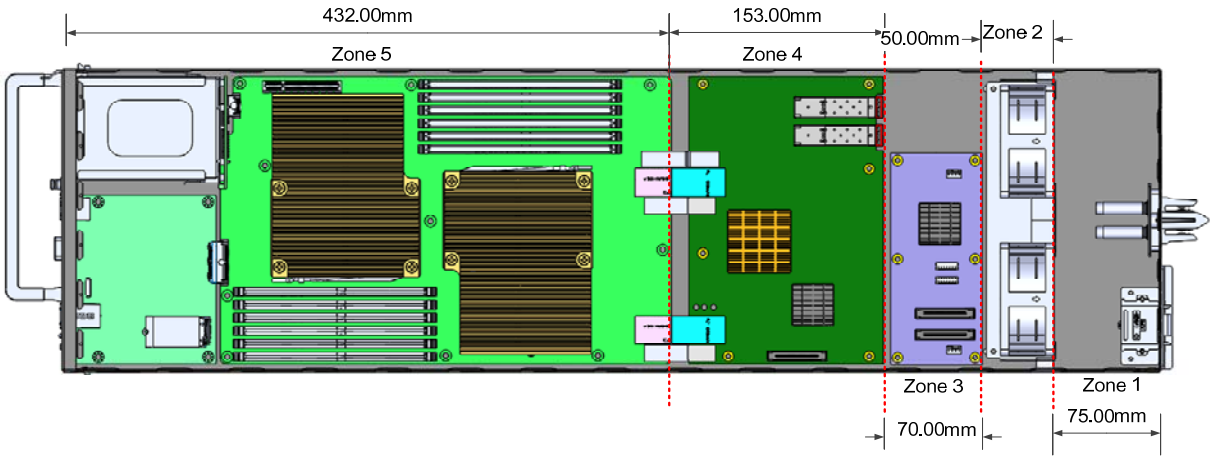


Figure 6. OpenSled Zone Layout (Top view)

The OpenSled server includes five functional zones. The Zone 1 is for connectivity, and has a depth of 75.00mm. The Zone 2 is for fan, and has a depth of 50.00mm. The Zone 3 is for power board, and has a depth of 70.00mm. The zone 4 is for mezzanine card, and has a depth of 145.00mm. The zone 5 is for compute sled, and has a depth of 440.00mm.

The zone 1, zone 2 and zone 3 are using single-layer structure, and they provide the common power, cooling, and blind-mate optical connector infrastructure for the OpenSled server. The zone 4 and zone 5 are using two-layer structure, and each layer includes a compute board and a mezzanine card to

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implement the required networking to blind-mate optical connector. Totally the OpenSled server provides two independent server nodes with shared power input and cooling facility.

6.3 OpenSled Server Mechanical Retention and Handle Features

The mechanical retention and handle features of the OpenSled server are following the mechanical retention and handle requirements described in Section 6.6 of CG-OpenRack-19 Sled and Rack Specification.

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7 Connectivity Zone Specifications

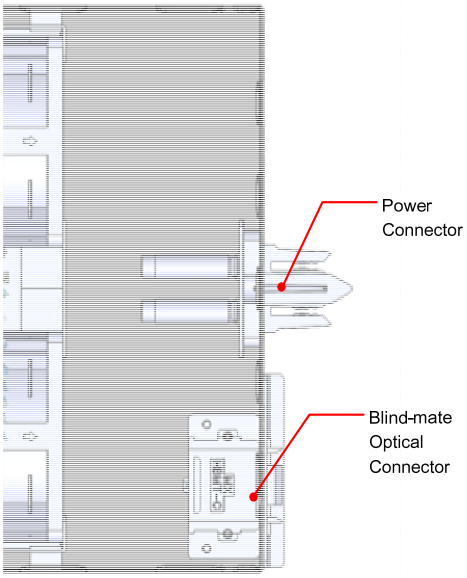
Zone 1 defines for the connectivity zone for power and optical connectors.

7.1 Power Connector Placement

The power is retrieved from the two vertical bus bars in the rear of the CG-OpenRack-19 shelf. When the half-width OpenSled server is installed in the left side of the shelf, it takes 12VDC power input from the left bus bar. When the half-width OpenSled server is installed in the right side of the shelf, it takes 12VDC power input from the right bus bar.

The power connector of the OpenSled server is following the power connector and bus bar pair requirements described in Section 6.3 and Section 7.1 of CG-OpenRack-19 Sled and Rack Specification.

Figure 7. OpenSled Power Connector Placement (Top view)



7.2 Optical Connector Placement

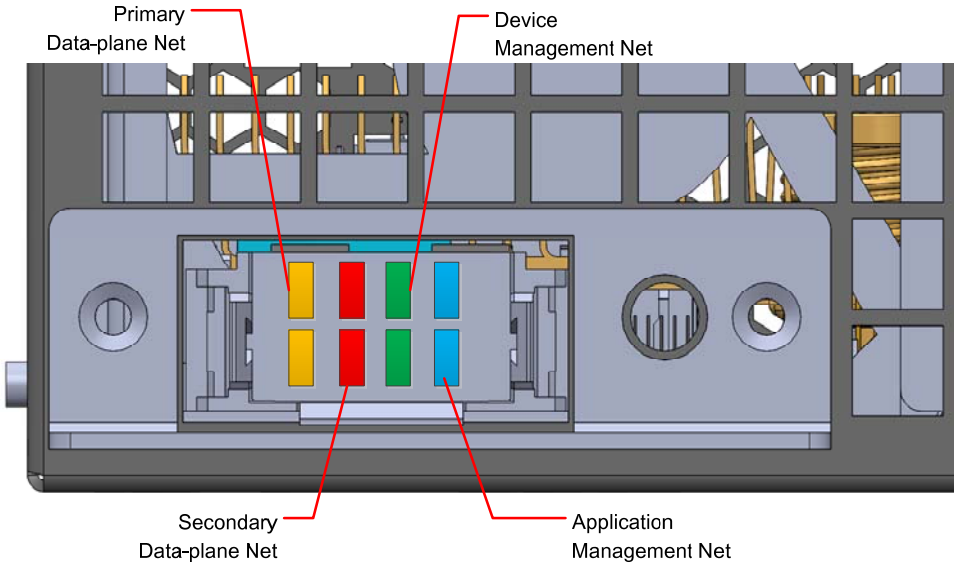
The main network connections of the OpenSled server is implemented by following the sled optical data port requirements described in Section 8 of CG-OpenRack-19 Sled and Rack Specification.

There are totally eight pairs of rear-mounted blind-mate “daughtercard” optical housing that mate with a compatible “backplane” hosing on the rear of a CG-OpenRack-19 shelf. The eight interfaces are organized into two groups, and each group provides four links between a server node and the TOR switches.

- Yellow optic connector: 10/40GbE primary data-plane link
- Red optic connector: 10/40GbE secondary data-plane link
- Green optic connector: 1GbE IPMI-based device management link
- Blue optic connector: 1GbE application management link

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Figure 8. OpenSled Server Blind-mate Optical Connector Assignment (rear view)

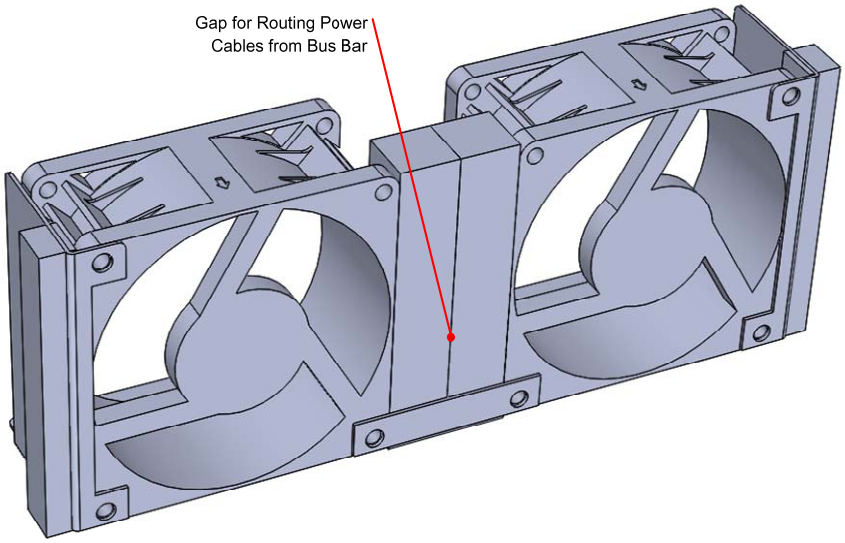


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8 Cooling Zone Specifications

Zone 2 defines for the cooling zone to place two PWM fans. In the middle of the two fans, there is a small gap that is reserved to the cabling of the power line from the bus bar.

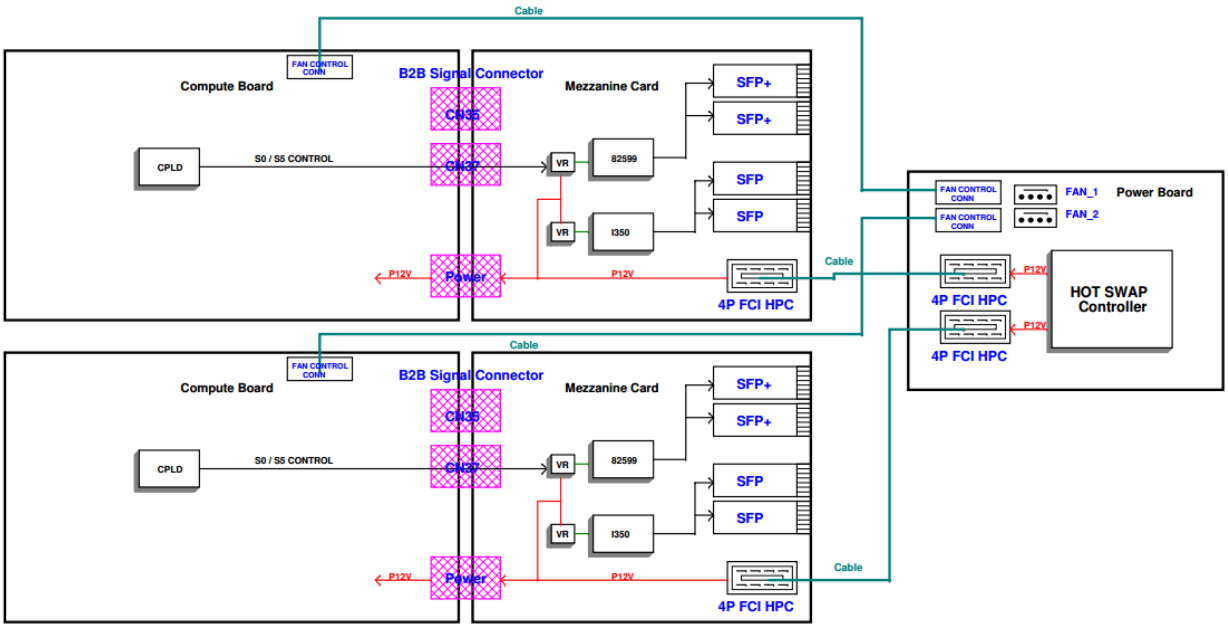
Figure 9. **OpenSled Server FAN Zone**



There is a BMC on each server node, which is responsible for monitoring the temperature sensors on the compute board and its supporting mezzanine card, and then a proper fan speed is selected and a corresponding PWM value is outputted by each BMC. A PWM comparator on the power board will select the larger PWM to driver the fans.

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Figure 10. The Power and Fan Scheme of OpenSled Server



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9 Power Zone Specifications

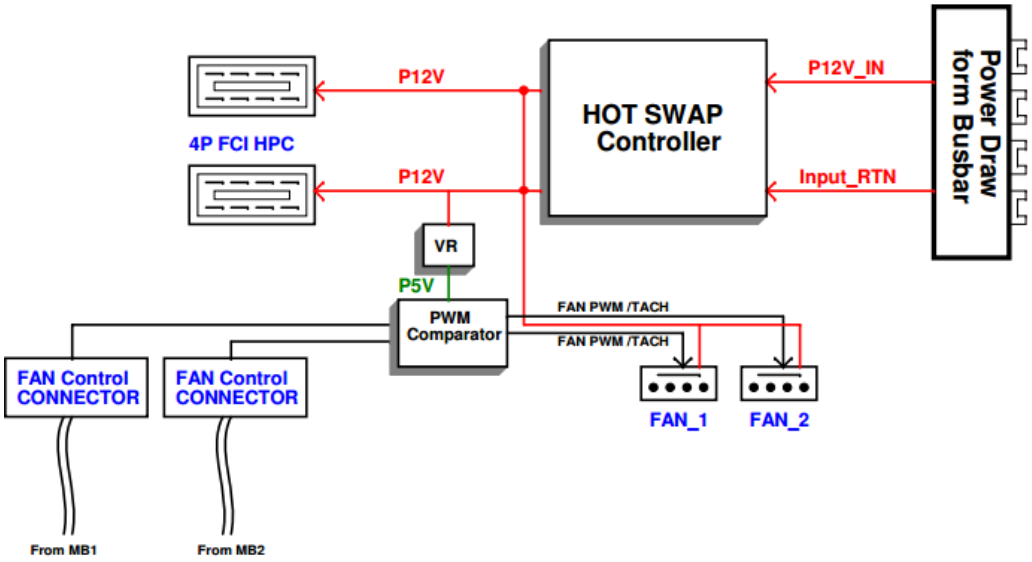
Zone 3 defines for power zone to place the power board, which takes power form the rear bus-bar and supplies it to the mezzanine cards, compute boards, and also the cooling fans.

9.1 Power and Fan Schema

The power supply board includes a hot-swap controller which is used to support the hot-swapping of the whole OpenSled server. When the power board detects the insertion of the OpenSled server is put in place, it will enable the +12V power supply from bus-bar to the mezzanine card directly.

The electronic components on the mezzanine cards draw power via a voltage regulator behind the +12V power supply. There is board to bard connector between compute board and mezzanine card, which is used to route the +12V power supply from the mezzanine card to the front server board. There are several voltage regulators on the compute board that transform the +12V power supply into the required voltage levels on the compute board. The cooling fans draw its power directly from a voltage regulator on the power board.

Figure 11. Block Diagram of Power Board



9.2 Power Cable Connector

The power board and mezzanine card use one pair of HPC connectors from FCI Electronics for power delivery from power board to mezzanine card via a cable. The pin definitions are described in the following table.

Table 1. The Pin Definitions of Power Cable Connectors

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Net name	Pin	Description	Group
P12V	A1	P12V power delivery from power board to mezzanine card	Power
P12V	B1		
GND	A2	Ground return	Ground
GND	B2		

9.3 Fan Cable Connector

The power board is also responsible for the PWN splitting and driver the cooling FAN. Because there are two server nodes in the OpenSled server, so there are two PWM signals from two independent compute board, and they are all routed to a PWM comparator on the power board via fan cables, and the PWM comparator selects the higher PWM signal and uses it to determine the speed of the cooling fans.

The fan cable connector is from HIROSE (P/N: DF11-14DP-2DSA), and the pin definitions of the fan cable connector is shown in the table 2.

Table 2. The Pin Definitions of the Fan Cable Connector

Net name	Pin	I/O	Description
GND	1		Ground return
GND	2		Ground return
BBC_FAN_PWM3	3	O	FAN PWM output from motherboard to FAN board
BBC_FAN_TACH3	4	I	FAN TACH input from FAN board to motherboard
BBC_FAN_PWM2	5	O	FAN PWM output from motherboard to FAN board
BBC_FAN_TACH2	6	I	FAN TACH input from FAN board to motherboard
BBC_FAN_PWM1	7	O	FAN PWM output from motherboard to FAN board
BBC_FAN_TACH1	8	I	FAN TACH input from FAN board to motherboard
BBC_FAN_PWM3_EN	9	O	FAN board power control signal from motherboard to FAN board
FAN_PWM3_PRESENT_N	10	I	FAN present signal from FAN board to motherboard, Low active.
BBC_FAN_PWM2_EN	11	O	FAN board power control signal from motherboard to FAN board
FAN_PWM2_PRESENT_N	12	I	FAN present signal from FAN board to motherboard, Low active.

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BBC_FAN_PWM1_EN	13	O	FAN board power control signal from motherboard to FAN board
FAN_PWM1_PRESENT_N	14	I	FAN present signal from FAN board to motherboard, Low active.

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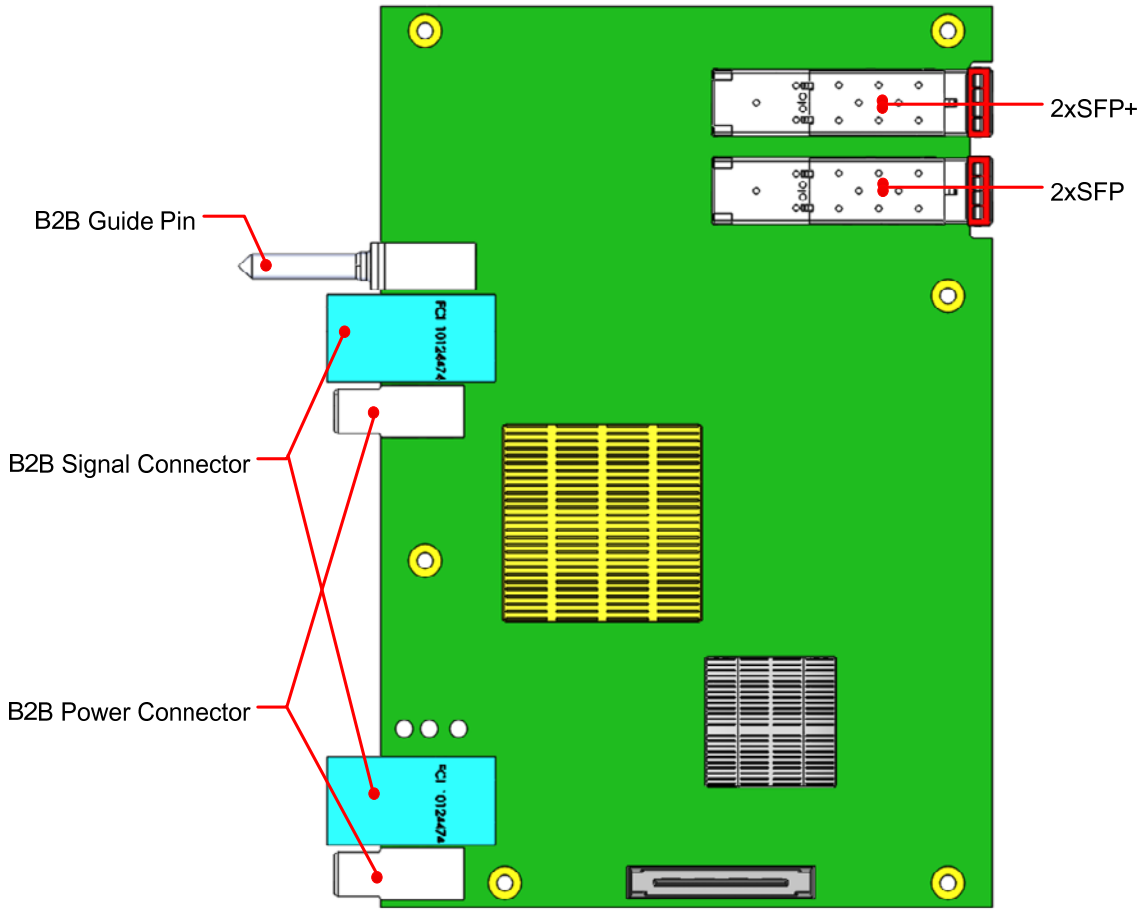
10 Mezzanine Card Zone Specifications

Zone 4 defines for a replaceable mezzanine card in order to support different network configurations. By now, both 2x10G and 2x40G data plane net can be supported.

On the front side, the mezzanine card has 5 board to board (B2B) connectors. Two of them are used for signal connection, two of them are used for power connection, and the remained one is guide pin.

On the rear side, the mezzanine card has 2xSFP and 2xSFP+ interfaces that provide the required optical connection to the rear blind-mate connector.

Figure 12. OpenSled Server Mezzanine Card (top view)



10.1 B2B Signal Connector

The mezzanine card uses two FCI AirMax VSe R.A. connectors (P/N:10124474) for the signal connection.

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There are two B2B signal connectors (CN35 and CN37). The signal connector (CN35) includes one group of PCIex8 Gen3 lanes. The pin definition of CN35 is shown in Table 3.

Table 3. The Pin Definitions of B2B Signal Connector CN35

Net name	Pin	Drive	IO/Signal Type	AC Cap on board	Description	PCIE root port or Group
BBC_PCIE-P0	A1	PCH	O/CLK	N/A	100 MHz PCIe 3.0 specification compliant differential clock	
BBC_PCIE-N0	B1	PCH	O/CLK	N/A	100 MHz PCIe 3.0 specification compliant differential clock	
GND	C1					
CPU0_BBC_C_TXP24	D1	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1A**
CPU0_BBC_C_TXN24	E1	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1A**
GND	F1					
CPU0_BBC_C_TXP28	G1	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1B**
CPU0_BBC_C_TXN28	H1	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1B**
GND	I1					
CPU0_BBC_RXP27	J1	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1A**
CPU0_BBC_RXN27	K1	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1A**
GND	L1					
CPU0_BBC_RXP31	M1	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1B**
CPU0_BBC_RXN31	N1	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1B**
GND	O1					
GND	A2					
SATA_C_TX-P2	B2	PCH	O/SATA	Yes	PCH Serial ATA 2 Differential Transmit Pair	
SATA_C_TX-N2	C2	PCH	O/SATA	Yes	PCH Serial ATA 2 Differential Transmit Pair	

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GND	D2					
CPU0_BBC_C_TXP25	E2	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1A**
CPU0_BBC_C_TXN25	F2	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1A**
GND	G2					
CPU0_BBC_C_TXP29	H2	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1B**
CPU0_BBC_C_TXN29	I2	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1B**
GND	J2					
CPU0_BBC_RXN26	K2	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1A**
CPU0_BBC_RXP26	L2	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1A**
GND	M2					
CPU0_BBC_RXP30	N2	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1B**
CPU0_BBC_RXN30	O2	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1B**
GND	P2					
SATA_C_RX-P2	A3	DEVICE	I/SATA	No	PCH Serial ATA 2 Differential Receive Pair	
SATA_C_RX-N2	B3	DEVICE	I/SATA	No	PCH Serial ATA 2 Differential Receive Pair	
GND	C3					
CPU0_BBC_C_TXP26	D3	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1A**
CPU0_BBC_C_TXN26	E3	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1A**
GND	F3					
CPU0_BBC_C_TXP30	G3	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1B**
CPU0_BBC_C_TXN30	H3	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1B**
GND	I3					
CPU0_BBC_RXP25	J3	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1A**
CPU0_BBC_RXN25	K3	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1A**

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GND	L3					
CPU0_BBC_RXP29	M3	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1B**
CPU0_BBC_RXN29	N3	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1B**
GND	O3					
GND	A4					
SATA_C_TX-P3	B4	PCH	O/SATA	Yes	PCH Serial ATA 3 Differential Transmit Pair	
SATA_C_TX-N3	C4	PCH	O/SATA	Yes	PCH Serial ATA 3 Differential Transmit Pair	
GND	D4					
CPU0_BBC_C_TXP27	E4	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1A**
CPU0_BBC_C_TXN27	F4	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1A**
GND	G4					
CPU0_BBC_C_TXP31	H4	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1B**
CPU0_BBC_C_TXN31	I4	CPU0	O/PCIe	Yes	PCIe Transmit Data Output	**PE1B**
GND	J4					
CPU0_BBC_RXN24	K4	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1A**
CPU0_BBC_RXP24	L4	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1A**
GND	M4					
CPU0_BBC_RXP28	N4	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1B**
CPU0_BBC_RXN28	O4	DEVICE	I/PCIe	No	PCIe Receive Data Input	**PE1B**
GND	P4					
CPU0_P0_ATT_PWR_LED	A5	PCA9555 PW	O/CMOS	N/A	This indicator is connected to the Attention LED or Power LED on the baseboard (PCI Express Hot-Plug Interface)	**PCI-E hot plug**
CPU0_P0_RRC_RDY_N	B5	RRC	I/CMOS	N/A	Low when switch Ready AND Present AND Power Good	**PCI-E hot plug**

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GND	C5					
BBC_PCIE-P1	D5	PCH	O/CLK	N/A	100 MHz PCIe 3.0 specification compliant differential clock	
BBC_PCIE-N1	E5	PCH	O/CLK	N/A	100 MHz PCIe 3.0 specification compliant differential clock	
GND	F5					
LS_RRC_PRESENT_N	G5	PCIe device	I/CMOS	N/A	Input signal that indicates PCIE device is plugged into the slot	**PCI-E hot plug**
Reserved	H5					
GND	I5					
Reserved	J5					
Reserved	K5					
GND	L5					
Reserved	M5					
Reserved	N5					
GND	O5					
GND	A6					
CPU0_P0_PCIE_RESET_N	B6	CPLD	O/CMOS	N/A	Reset singal for PCIE hot plug device	**PCI-E hot plug**
CPU0_P0_MRL_SW_N	C6	PCIe device	I/CMOS	N/A	Manual retention latch status or Electromechanical latch status input indicates that the retention latch is closed or open	**PCI-E hot plug**
GND	D6					
Reserved	E6					
Reserved	F6					
GND	G6					
Reserved	H6					
Reserved	I6					

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GND	J6					
FC_RX0_L0_P	K6	DEVICE	I/KR	Yes	Serial Data Input for Ethernet interface	**Group B, Port 0**
FC_RX0_L0_N	L6	DEVICE	I/KR	Yes	Serial Data Input for Ethernet interface	**Group B, Port 0**
GND	M6					
Reserved	N6					
Reserved	O6					
GND	P6					
CPU0_P0_ATT_BUTTON_N	A7	RRC board	I/CMOS	N/A	Input signal per slot which indicates that the user wishes to hot remove or hot add a PCI Express card/module	**PCI-E hot plug**
CPU0_P0_PWREN	B7	PCA9555 PW	O/CMOS	N/A	Output signal that indicates power enable for PCIe device	**PCI-E hot plug**
GND	C7					
Reserved	D7					
Reserved	E7					
GND	F7					
Reserved	G7					
Reserved	H7					
GND	I7					
Reserved	J7					
Reserved	K7					
GND	L7					
Reserved	M7					
Reserved	N7					
GND	O7					

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GND	A8					
LS_I2C_ALERT_N	B8	DEVICE	I/CMOS	N/A	SMBus Alert to PCH	
Reserved	C8					
GND	D8					
Reserved	E8					
Reserved	F8					
GND	G8					
Reserved	H8					
Reserved	I8					
GND	J8					
Reserved	K8					
Reserved	L8					
GND	M8					
Reserved	N8					
Reserved	O8					
GND	P8					
BBC_SMB_L_CLK	A9	PCH	IO/I2C	N/A	PCH I2C bus	
BBC_SMB_L_DAT	B9	PCH	IO/I2C	N/A	PCH I2C bus	
GND	C9					
Reserved	D9					
Reserved	E9					
GND	F9					
Reserved	G9					
Reserved	H9					
GND	I9					

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Reserved	J9					
Reserved	K9					
GND	L9					
Reserved	M9					
Reserved	N9					
GND	O9					
GND	A10					
IPMB_CLK_B	B10	BMC	IO/I2C	N/A	IPMB I2C Bus	
IPMB_DAT_B	C10	BMC	IO/I2C	N/A	IPMB I2C Bus	
GND	D10					
Reserved	E10					
Reserved	F10					
GND	G10					
Reserved	H10					
Reserved for hybrid	I10					
GND	J10					
PCIE_SCL_CN_L	K10	BMC	IO/I2C	N/A	BMC I2C bus	
PCIE_SDA_CN_L	L10	BMC	IO/I2C	N/A	BMC I2C bus	
GND	M10					
BUF_SLPS5_N	N10	CPLD	O	N/A	SLP_S5# is for power plane control	
BBC_RST_N	O10	PCH	O/P3V3	N/A	Platform Reset	
GND	P10					

The signal connector (CN35) includes serval groups of PCIex1 Gen3 lanes and NC-SI for implementing IPMI-based device management net. The pin definitions of CN37 is shown in table 4.

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Table 4. The Pin Definitions of B2B Signal Connector CN37

Net name	Pin	Drive	IO/Signal Type	AC Cap on board	Description	Group
Reserved	**A1**					
Reserved	**B1**					
GND	**C1**					
Reserved	**D1**					
Reserved	**E1**					
GND	**F1**					
Reserved	**G1**					
Reserved	**H1**					
GND	**I1**					
PLTRST_DEV2-L	**J1**	PCH	O/P3V3	N/A	Platform Reset	MISC
Reserved	**K1**					
GND	**L1**					
Reserved	**M1**					
Reserved	**N1**					
GND	**O1**					
GND	**A2**					
Reserved	**B2**					
Reserved	**C2**					
GND	**D2**					
Reserved	**E2**					
Reserved	**F2**					
GND	**G2**					
Reserved	**H2**					

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Reserved	**I2**					
GND	**J2**					
Reserved	**K2**					
Reserved	**L2**					
GND	**M2**					
Reserved	**N2**					
Reserved	**O2**					
GND	**P2**					
Reserved	**A3**					
Reserved	**B3**					
GND	**C3**					
Reserved	**D3**					
Reserved	**E3**					
GND	**F3**					
Reserved	**G3**					
Reserved	**H3**					
GND	**I3**					
Reserved	**J3**					
Reserved	**K3**					
GND	**L3**					
Reserved	**M3**					
Reserved	**N3**					
GND	**O3**					
GND	**A4**					

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Reserved	**B4**					
Reserved	**C4**					
GND	**D4**					
Reserved	**E4**					
Reserved	**F4**					
GND	**G4**					
Reserved	**H4**					
Reserved	**I4**					
GND	**J4**					
CSA_LAN1_CLK-P	**K4**	PCH	O/CLK	N/A	100 MHz PCIe 3.0 specification compliant differential clock	CLOCK
CSA_LAN1_CLK-N	**L4**	PCH	O/CLK	N/A	100 MHz PCIe 3.0 specification compliant differential clock	CLOCK
GND	**M4**					
Reserved	**N4**					
Reserved	**O4**					
GND	**P4**					
Reserved	**A5**					
Reserved	**B5**					
GND	**C5**					
Reserved	**D5**					
Reserved	**E5**					
GND	**F5**					
Reserved	**G5**					
Reserved	**H5**					
GND	**I5**					

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CSA_LAN2_CLK-N	**J5**	PCH	O/CLK	N/A	100 MHz PCIe 3.0 specification compliant differential clock	CLOCK
CSA_LAN2_CLK-P	**K5**	PCH	O/CLK	N/A	100 MHz PCIe 3.0 specification compliant differential clock	CLOCK
GND	**L5**					
Reserved	**M5**					
Reserved	**N5**					
GND	**O5**					
GND	**A6**					
C_RMII_RXD0	**B6**	Ethernet controller	O	N/A	Receive Data	NC-SI
Reserved	**C6**					
GND	**D6**					
C_NCSI_ARB_IN	**E6**	Ethernet controller	I	N/A	Hardware Arbitration Input	NC-SI
Reserved	**F6**					
GND	**G6**					
C_NCSI_ARB_OUT	**H6**	Ethernet controller	O	N/A	Hardware Arbitration Output	NC-SI
C_LAN4_50M_CLK	**I6**	Clock buffer	O/CLK	N/A	Reference Clock	NC-SI
GND	**J6**					
Reserved	**K6**					
Reserved	**L6**					
GND	**M6**					
Reserved	**N6**					
Reserved	**O6**					
GND	**P6**					

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C_RMII_IPMC_NIC_TXD1	**A7**	BMC	I	N/A	Transmit Data	NC-SI
Reserved	**B7**					
GND	**C7**					
C_RMII_NIC_IPMC_CRS_DV	**D7**	Ethernet controller	O/P3V3_SB	N/A	Carrier Sense/Receive Data Valid	NC-SI
C_RMII_IPMC_NIC_TXD0	**E7**	BMC	I	N/A	Transmit Data	NC-SI
GND	**F7**					
Reserved	**G7**					
Reserved	**H7**					
GND	**I7**					
CSA_LAN2_C_RXP	**J7**	DEVICE	I/PCIE	No	PCI Express Differential Receive Pair	PORT 8
CSA_LAN2_C_RXN	**K7**	DEVICE	I/PCIE	No	PCI Express Differential Receive Pair	PORT 8
GND	**L7**					
Reserved	**M7**					
Reserved	**N7**					
GND	**O7**					
GND	**A8**					
C_RMII_RXD1	**B8**	Ethernet controller	O	N/A	Receive Data	NC-SI
C_RMII_IPMC_NIC_TX_EN	**C8**	BMC	I	N/A	Transmit Enable	NC-SI
GND	**D8**					
Reserved	**E8**					
Reserved	**F8**					

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GND	**G8**					
CSA_VGA_C_TXN	**H8**	PCH	O/PCIE	Yes	PCI Express Differential Transmit Pair	PORT 3
CSA_VGA_C_TXP	**I8**	PCH	O/PCIE	Yes	PCI Express Differential Transmit Pair	PORT 3
GND	**J8**					
CSA_LAN1_C_RXP	**K8**	DEVICE	O/PCIE	No	PCI Express Differential Receive Pair	PORT 7
CSA_LAN1_C_RXN	**L8**	DEVICE	O/PCIE	No	PCI Express Differential Receive Pair	PORT 7
GND	**M8**					
Reserved	**N8**					
Reserved	**O8**					
GND	**P8**					
CSA_I2CCLK	**A9**	BMC	O/P3V3_SB	N/A	I2C bus	I2C
CSA_I2CDAT	**B9**	BMC	IO/P3V3_SB	N/A	I2C bus	I2C
GND	**C9**					
Reserved	**D9**					
Reserved	**E9**					
GND	**F9**					
Reserved	**G9**					
Reserved	**H9**					
GND	**I9**					
CSA_LAN1_C_TXN	**J9**	PCH	O/PCIE	Yes	PCI Express Differential Transmit Pair	PORT 7
CSA_LAN1_C_TXP	**K9**	PCH	O/PCIE	Yes	To MICA-5200	PORT 7
GND	**L9**					
Reserved	**M9**					

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Reserved	**N9**					
GND	**O9**					
GND	**A10**					
Reserved	**B10**					
Reserved	**C10**					
GND	**D10**					
Reserved	**E10**					
Reserved	**F10**					
GND	**G10**					
CSA_LAN2_C_TXP	**H10**	PCH	O/PCIE	Yes	PCI Express Differential Transmit Pair	PORT 8
CSA_LAN2_C_TXN	**I10**	PCH	O/PCIE	Yes	PCI Express Differential Transmit Pair	PORT 8
GND	**J10**					
Reserved	**K10**					
Reserved	**L10**					
GND	**M10**					
Reserved	**N10**					
Reserved	**O10**					
GND	**P10**					

10.2 B2B Power Connector

The mezzanine card uses two pair of FCI Airmax 2x2 R/A power connectors (P/N: 10052620) for power delivery from Mezzanine card to compute sled. The pin definitions are described in the table 5.

Table 5. The pin definitions of power connectors

Net name	Pin	Description	Group
P12V	**A1**	P12V power rail from backplane	Power

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P12V	**B1**	to motherboard	
P12V	**C1**		
P12V	**A2**		
P12V	**B2**		
P12V	**C2**		
GND	**A3**	Ground return	Ground
GND	**B3**		
GND	**C3**		
GND	**A4**		
GND	**B4**		
GND	**C4**		

10.3 B2B Guide Pin

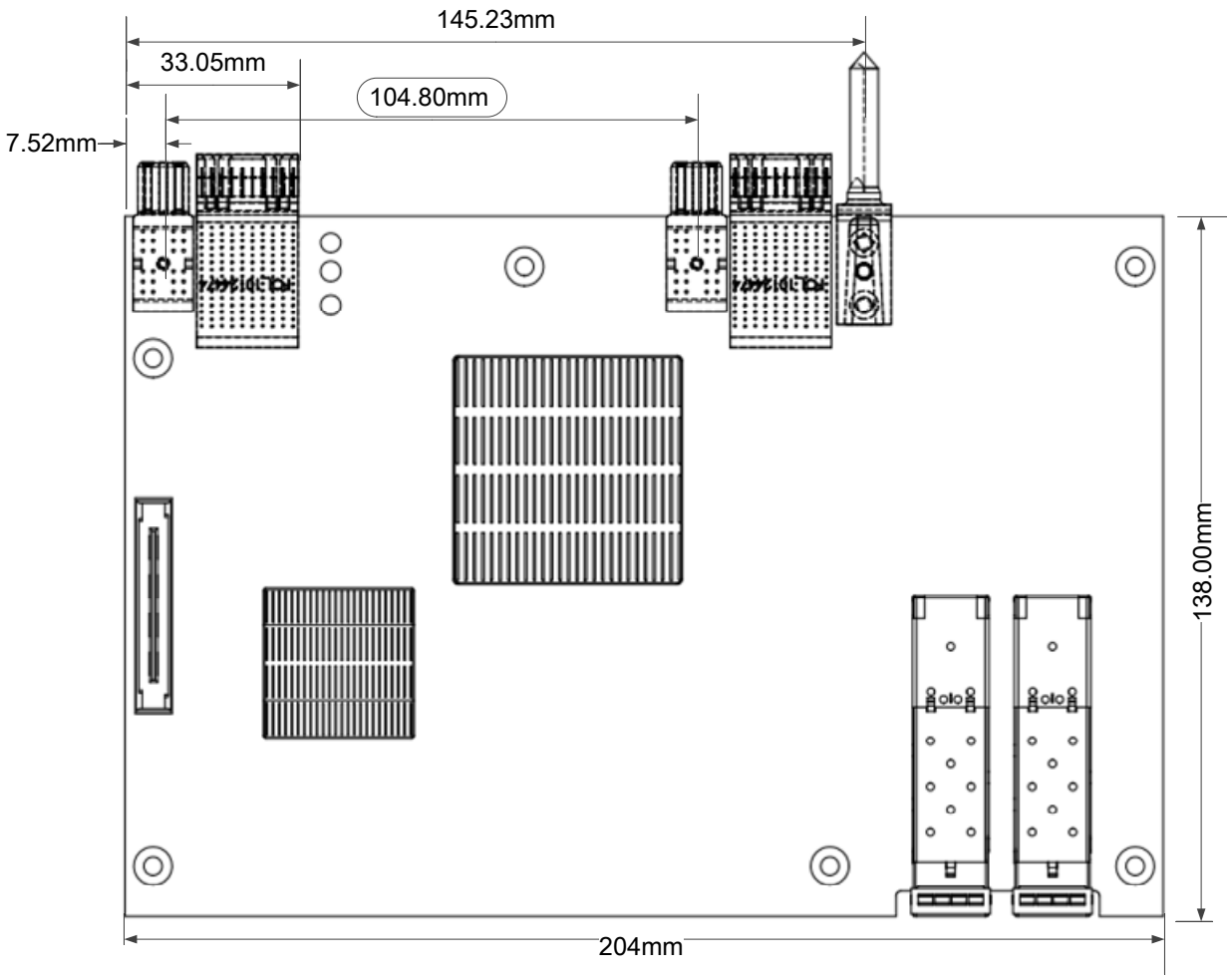
The compute server and mezzanine card uses one pair of FCI Airmax 10.8mm R/A guide pin (P/N: 10044366) to achieve blind mating.

10.4 B2B Connector Positions

The following figure illustrates the B2B connector positions respective to the mezzanine card edge.

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Figure 13. B2B Connector Locations



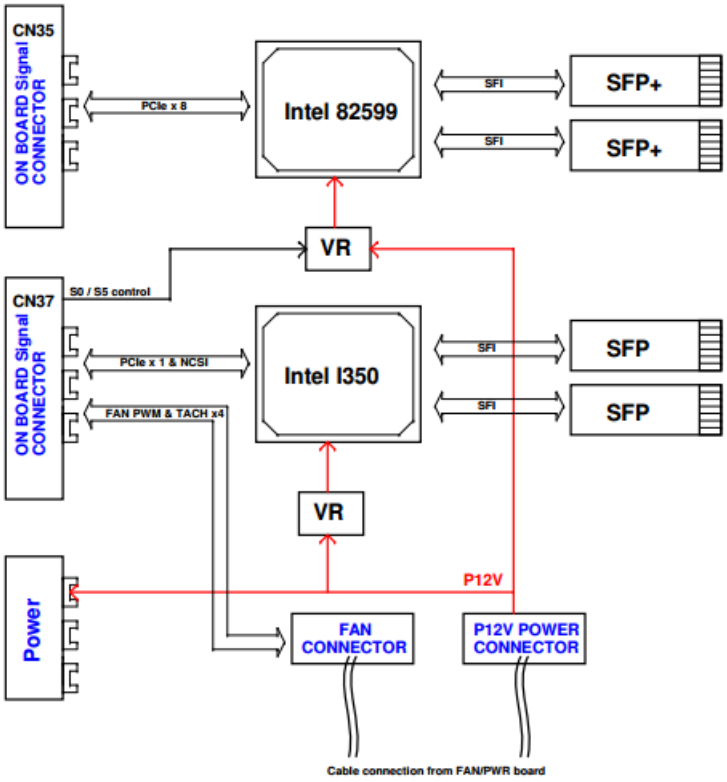
10.5 10G Mezzanine Card Example

The block diagram in Figure 12 illustrates the design of a 10G mezzanine card. One Intel 82599 is used to implement the primary and secondary 10G data links. One Intel I350 with NC-SI interface is used to implement the 1GbE IPMI-based device management link and 1GbE application management link. The optical links are routed to the optical connector placement on the rear of the shelf.

The power supply to Intel 82599 is disabled when the computing board enters ACPI S0/S5 state. In order to provide out-of-band management, the power supply to Intel I350 is always enabled.

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Figure 14. Block Diagram of 10G Mezzanine Card



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11 Compute Zone Specifications

Zone 5 defines for the Open POD for the Compute, Memory, Storage and optional NIC front panel interface. Zone 5 is located in the front half of the Open POD and allocates 440mm(L) x 215mm(W) and 84mm (2U) (H) space.

The Compute zone is dedicated to specific CPU, BMC Management; front and rear connections enabling a wide range of applications that is specific to the required use case. Appendix.14.3 provides an example of the Zone 5 configuration which is based on the ADLINK Modular Industrial Cloud Architecture MCN-2600 CPU Sled.

Zone 5 Compute area includes (but not limited to):

- Stackable Compute boards based on X86 architecture
- ARM, ASIC, FPGA, etc Silicon architectures
- Memory
- Storage (HDD or SDD)
- Network Interface Controller (NIC)
- Interfaces to Mezzanine Zone, Storage and NIC
- System level management functions via BMC chipsets
- Power and storage management
- Front panel options if required

Zone 5 Compute area can be comprised of two stackable CPU boards providing a dense compute module in a 2U ½ width Pod. Each CPU board has the ability to connect to multiple storage devices initially, and expand to all storage sleds that can be used as storage pods.

This specification provides the internal connections between the CPU, Storage, Optional Network Interface, and Mezzanine card. Included in this section is the On-Board Management functions required to manage the CPU, Power, and Fans via IPMI 2.0 and a Board Management Controller (BMC).

Appendix 14.3 provides the specification of ADLINK's 2600-based CPU motherboard as a reference for Zone 5 CPU design.

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11.1 B2B Connectors

The compute board shall use the following components to implement the board to board connection with mezzanine card.

- B2B signal connector: The compute board shall implement two signal connectors as described in Section 10.1, and connector type shall use FCI Airmax VSe connector (P/N: 10115913).
- B2B power connector: The compute board shall implement two power connectors as described in Section 10.2 and the connector type shall use FCI Airmax 2x2 R/A power connector (P/N: 10028917).
- B2B guide pin: The compute board shall implement one guide pin, and the connector type shall use FCI Airmax 10.8mm R/A guide receptacle module (P/N: 10037912).

11.2 Power System

The compute board takes its +12V power from the B2B power as mentioned above. The +12V power are transferred into the required voltages on the motherboard. The power supply on the motherboard is also divided into two different power domains.

The main power domain includes the main components to the host, like CPU, memory, Hard disk, PCIe interface, and so on. The main power is enabled when the user switch on the power on through a front plane button or send a “Chassis Control (Power on)” command to BMC via its IPMB or LAN interface.

The standby power domain includes BMC, NC-SI network cards, and PCH to enable out of band IPMI based management, and power button startup. The standby power domain is always enabled if the power supply is alive.

11.3 Front Panel

There can be two server boards in an OpenSled server, and each server shall have a front plane interface with the following required functionalities.

- Power button: The user can trigger a graceful shutdown of the operation system if pushing the button less than 4 seconds. The user can trigger a forceful shutdown of the operation system if pushing the button longer than 4 seconds.
- Reset button: The user can trigger a cold reset of the motherboard by pushing the invaginate reset button.
- Power LED: The power LED is green and controlled by hardware directly. The LED is on when main power is enabled, and the LED is off when main power is disabled.
- Status LED: The status LED is red/green dual-color LED and controlled by BMC. The red color is used to indicate BIOS post status. The green color is used to indicate system status after BIOS post, can be connected with the BMC watchdog status. The BMC also implements an OEM command to let the user control the green LED via IPMI command.

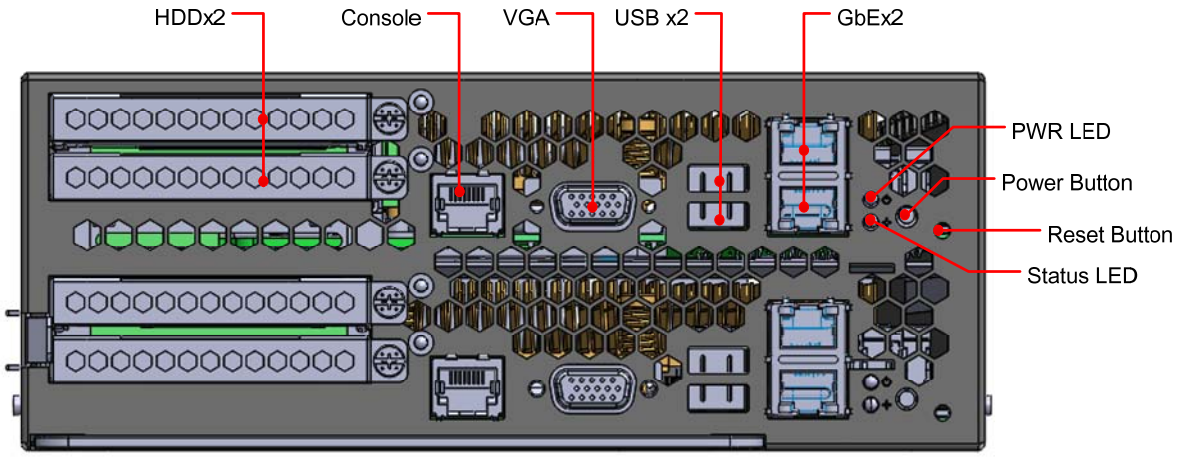
Optionally they can provide the following interfaces.

- GeE interface: The GeE interface can be used for local debugging in the development phase.

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- USB interface: The USB interface is provided to install the mouse and keyboard.
- VGA interface: It benefits when local GUI is required.
- Console interface: It benefits when the user wants to access the system via a serial port.
- HDD bay: Hot-swappable HDD bay can be implemented to provide local storage.

Figure 15. Front Panel Interface of Compute sled



11.4 Basic Input Output System (BIOS)

The motherboard BIOS shall be customized to improve the power efficiency. The measures include:

- CPU Power Technology is set to "Energy Efficient"
- CPU EIST is enabled

11.4.1 Setup Menu

The BIOS setup utility shall provide the following setup screen.

- Main BIOS setup screen: BIOS Vendor, Core Version, Motherboard Name, BIOS Build Time, System Language, System Date, and System Time.
- Advanced BIOS setup screen: Board Automatic Power-up Configuration, ACPI Configuration, Super IO Configuration, Serial Port Console Redirection, iSCSI Configuration, PCIe SR-IOV Support, PXE boot Configuration, BMC Watchdog Configuration, LAN Bypass Configuration.
- Intel RefCode Setup screen: Processor Configuration, Advanced Power Management Configuration, Common RefCode Configuration, Memory Configuration, IIO Configuration, PCH Configuration.
- Server Management setup screen: BMC Firmware Revision, and BMC Watchdog Configuration.
- Security setup screen: Administered Password, User Password, and HDD Security Configuration.
- Boot setup screen: Setup Prompt Timeout, Bootup NumLock State, Quiet Boot Configuration, and Boot Option Priorities.

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11.4.2 Post Error Code

Table 6. BIOS POST Error Codes and Interpretation

Error Code	Description
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	Reset PPI is not available
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM

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0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error

11.5 Baseboard Management Controller (BMC)

The BMC shall work as a standalone system, providing out-of-band IPMI management service that is not dependent on the health status of the host. The BMC is responsible to monitor the thermal situation of the board and control the fan speed adaptively, and as well as provide remote control for the x86 system.

11.5.1 LAN Interface

The BMC shall provide LAN accessing via the NC-SI interface built on the host network cards. And the host network cards are be powered from the standby power, and it can work even if the host is powered down (main power is cut off).

If the motherboard has more than one NC-SI packages. By default the IPMI LAN interface shall be directed to the 1G port on the rear optical connector. Optionally, the user can direct the IPMI LAN interface to the 1G GbE interface on the front panel via sending IPMI command to BMC.

11.5.2 Serial Over LAN (SOL)

Because a GUI interface does not scale, the BMC does not require supporting the graphic-based iKVM feature, instead the BMC shall provide the text-based Serial Over LAN (SOL) feature. With SOL

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redirection system administrators can remotely view the text-based host console from anywhere and perform any task that doesn't require a GUI.

11.5.3 Power Monitoring and Controlling

The BMC shall support power monitoring through the hot-swap controller, and a current sensor shall be implemented to provide real-time power consumption of the motherboard. A series of voltage sensors shall also be implemented to monitor the key power rails on the motherboard.

The BMC shall support power on/off/cycle and cold/warm reset the host system through out-of-band IPMI commands. Use can execute a host recovery action by triggering the power control regardless of the host operation status.

The BMC can optionally enable the Intel Node Manager power limiting function. The user can enforce a power limit policy by bridging Intel Node Manager Commands to the Intel Management Engine (ME) via BMC.

11.5.4 Fan Speeding and Connector

The BMC shall implement a series of temperature sensors to monitor the thermal situation of the key components in the motherboard, including inlet air temperature, CPU, DIMM and PCH. When BMC works in a single board system, based on the aggregated thermal situation, the BMC will run the FAN based on an adaptive speeding algorithm.

When there are no thermal alarms, the BMC will run the FAN at a miniLevel speed, and the miniLevel speed is decided monotonously based on the inlet air temperature. A higher inlet air temperature will generate a higher miniLevel speed. When there are thermal alarms, the BMC will increase the FAN speed to eliminate the thermal alarms. The higher the thermal alarm level is, the faster the BMC increases the FAN speed, until the FANs reach their largest speed. After all thermal alarms are eliminated, the BMC will return the FAN speed gradually to a miniLevel, which is calculated based on the current inlet air temperature.

The BMC shall also implement tachometers to monitor the fan speed and OEM command to fix the fan speed.

11.5.5 IPMI Sensors

The BMC can optional implement a serial of logical sensors to respect the operation status of the whole system. User can check the sensor reading or Sensor Event Log (SEL) to determine whether the system is running properly.

11.5.6 System Event Log (SEL)

The BMC supports shall support Sensor Event Log (SEL) with a size larger than 10 KB. The BMC uses circular SEL type, and the SEL repository acts like a ring buffer. When the repository becomes full, oldest logs are overwritten by new logs.

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12 Environmental Specifications

The OpenSled server shall meet the following environmental requirements:

- Operating temperature: 0 °C ~ +40 °C
- Short term operating: -5°C to +45°C, 5%-90% relative humidity
- Storage temperature: -40 °C~+70 °C
- Operating humidity: 20% ~ 90%RH@40℃, non-condensing
- Non-operating: 5%-90% relative humidity
- EMI: NEBS Level-3 compliance, FCC class A, CE emission, CCC, UL, CB and RoHS compliant

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13 Shock & Vibration

The OpenSled server shall meet shock and vibration requirements according to the following table.

Table 7. Vibration and Shock Capability

	Operating	Non-operating
Vibration	N/A	2.2Grms, 10 minutes per axis on all three axes
Shock	Half-sine 2G, 11ms pulse, 100 pulses in each direction, on each of the three axes	Trapezoidal, 25G, 170 inches/sec delta V, three drops in each direction, on each of the three axes.

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14 Appendix

14.1 Appendix: Commonly Used Acronyms

ACPI – advanced configuration and power interface

BIOS – basic input/output system

BMC – baseboard management controller

DDR4 – double data rate type 4

DIMM – dual inline memory module

EMI – electromagnetic interference

IPMI – intelligent platform management interface

LAN – local area network

PCB – printed circuit board

PCIe – peripheral component interconnect express

PCH – platform control hub

POST – power-on self-test

PWM – pulse-width modulation

RU – rack unit (1.75”)

SATA – serial AT attachment

SEL – system event log

SFP - small form-factor pluggable

SOL – serial over LAN

TOR – top of rack

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14.2 Appendix: ADLINK Modular Industrial Cloud Architecture CPU board

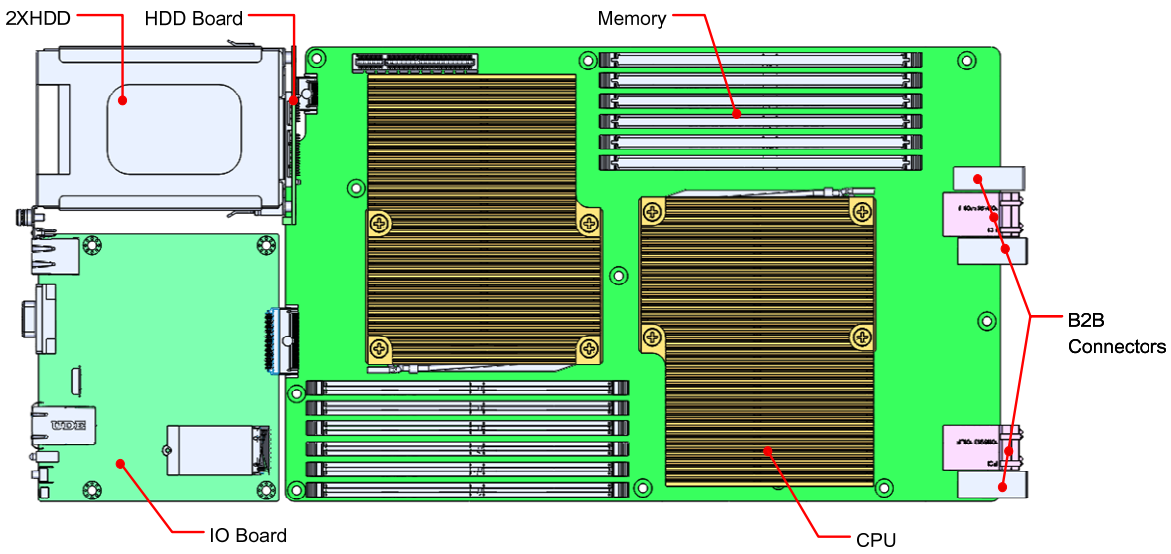
Below are the design specifications for the ADLINK MCN-2600 CPU which can be used for the CG OpenSled system:

The compute board is built based on Modular Industrial Cloud Architecture (MICA) proposed by ADLINK technologies. It benefits from the reuse of existing compute modules from ADLINK MICA products, and inherits the benefits from MICA including modular design, industrial features, and cloud computing support.

14.2.1 Motherboard Features

The motherboard uses Haswell/Broadwell processors, which are 64-bit, multi-core processors built on (Haswell) 22 / (Broadwell) 14-nanometer technology. The processors are designed to be paired with the C612 chipset on the Grantley platform. There are 12x DDR4-1600/1866/2133 DIMM sockets with ECC, with maximum 192GB memory.

Figure 16. Compute Board Layout



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The other features of the motherboard are listed in the following table.

Table 8. The main features of the MICA motherboard

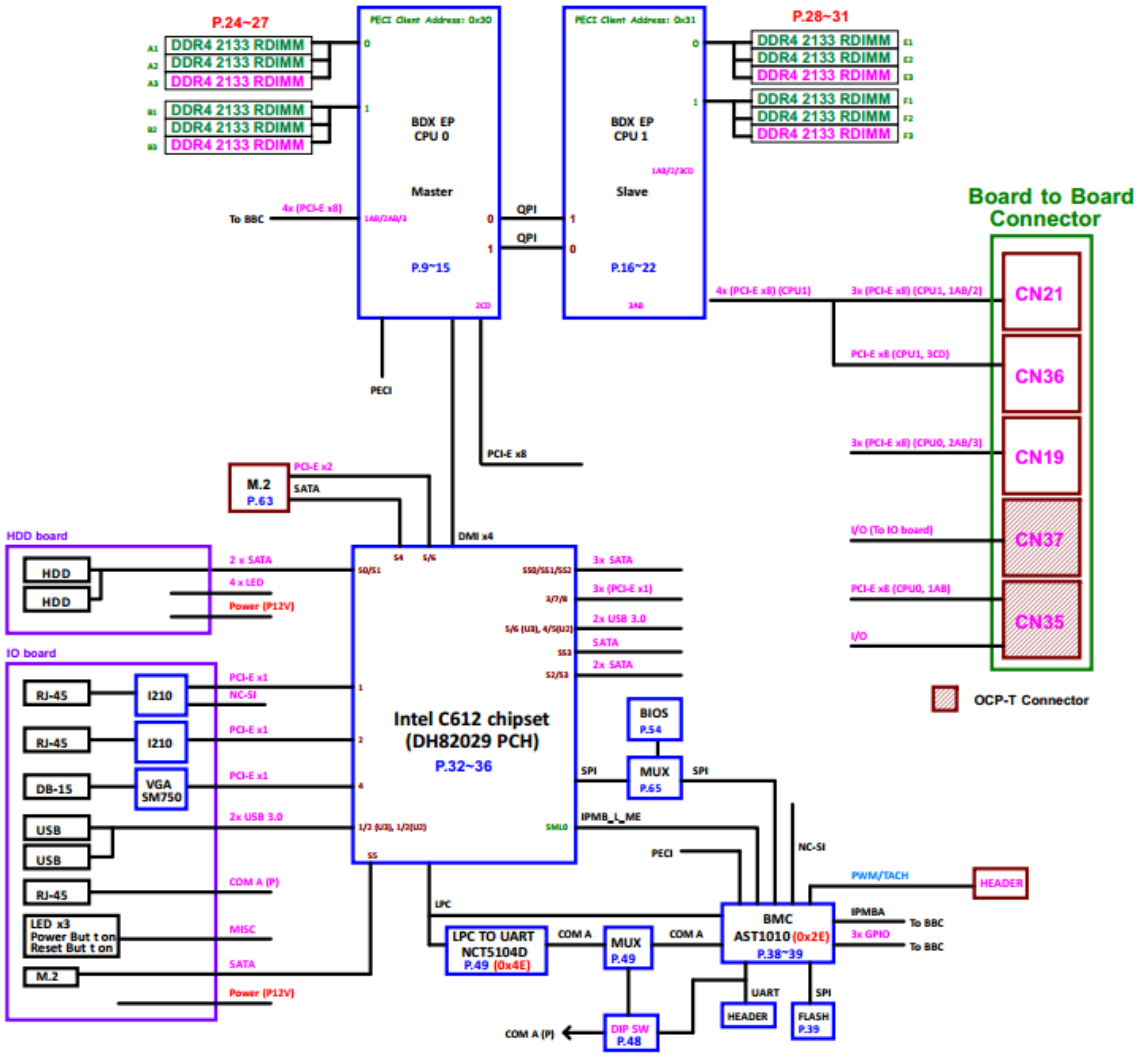
I/O Interface	**Ethernet**	2x RJ-45 10/100/1000BASE-T Ethernet ports
	Console	1x RJ-45 serial port
	USB	2x USB 3.0
	Graphics	1x VGA
	HDD/SSD	2x 2.5'' Hot-swappable SATA drive bays & 2x M.2 SSD
	LEDs	Power, Status (Dual-color), HDD
Control Buttons	**Power**	1x Power button(front)
	Reset	1x Reset Button(front)
Others	**Backplane**	2x PCIe G3 x 8 to Mezzanine card
	Operating System	Window 7/10 64bit, Linux Kernel 2.6 or above
Mechanical	**Form Factor**	213.9mmx 40.44mm x 432.1mm (W x H x D)

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14.2.2 Block Diagram

The following figure illustrates the functional block diagram of the MICA motherboard. For OpenSled server, only the back board connector CN35 and CN37 are soldered.

Figure 17. Block Diagram of Compute Motherboard

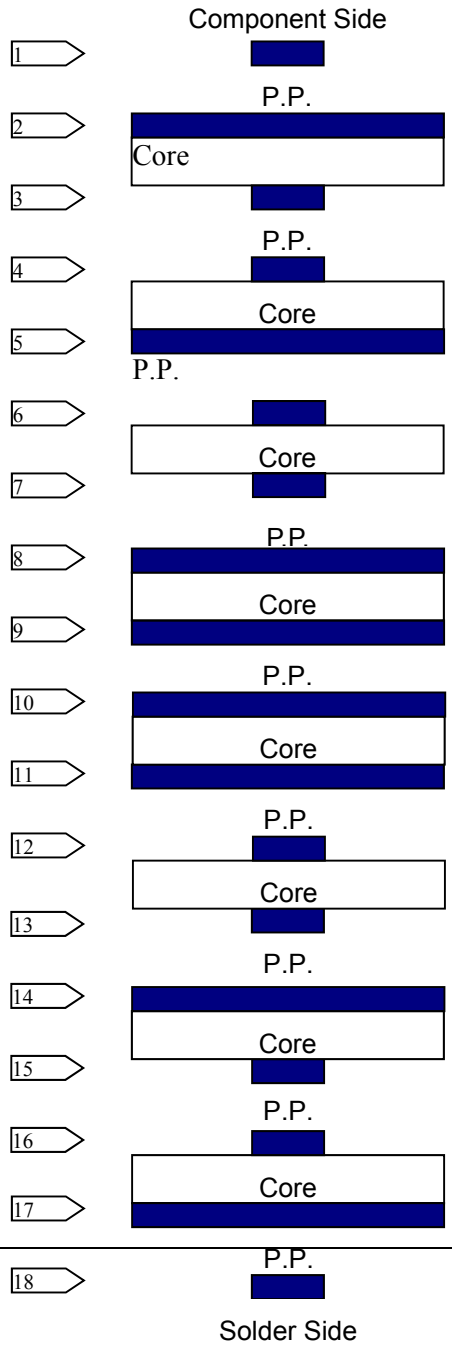


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14.2.3 Printed Circuit Board Stack-up

The motherboard's PCB stack-up and characteristic impedance estimation are defined in Table 1 and Table 2, respectively.

Table 9. **Stack-up of the Compute Motherboard**

Project Name： MICA-2600	Layer	Description	P.P / Core / Copper	Thickness mil	Dk	Df
						
		Solder Mask		0.7	4.2	0.026
		2nd Copper		1.6		
	1	Component	0.5 oz Cu *			
	A	P.P.	1078-62%	2.7	3.44	0.0042
	2	GND	0.5 oz Cu	0.6		
	B	Core	1086*1	3.0	3.45	0.0040
	3	S1	0.5 oz Cu	0.6		
	C	P.P.	1078-62%*2	5.4	3.46	0.0040
	4	GND	0.5 oz Cu	0.6		
	D	Core	1086*1	3.0	3.45	0.0040
	5	S2	0.5 oz Cu	0.6		
	E	P.P.	1078-62%*2	5.4	3.46	0.0040
	6	GND	0.5 oz Cu	0.6		
	F	Core	1086*1	3.0	3.45	0.0040
	7	S3	0.5 oz Cu	0.6		
	G	P.P.	1078-62%*2	5.4	3.46	0.0040
	8	GND	1.0 oz Cu	1.2		
	H	Core	3313*1	4	3.49	0.0039

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	9	Power	1.0 oz Cu	1.2		
	I	P.P.	2116HR*2+2116	14.1	3.57	0.0037
	10	Power	1.0 oz Cu	1.2		
	J	Core	3313*1	4	3.49	0.0039
	11	GND	1.0 oz Cu	1.2		
	K	P.P.	1078-62%*2	5.4	3.46	0.0040
	12	S4	0.5 oz Cu	0.6		
	L	Core	1086*1	3.0	3.45	0.0040
	13	GND	0.5 oz Cu	0.6		
	M	P.P.	1078-62%*2	5.4	3.46	0.0040
	14	S5	0.5 oz Cu	0.6		
	N	Core	1086*1	3.0	3.45	0.0040
	15	GND	0.5 oz Cu	0.6		
	O	P.P.	1078-62%*2	5.4	3.46	0.0040
	16	S6	0.5 oz Cu	0.6		
	P	Core	1086*1	3.0	3.45	0.0040
	17	GND	0.5 oz Cu	0.6		
	Q	P.P.	1078-62%	2.7	3.44	0.0042
	18	Component	0.5 oz Cu *	1.6		
		2nd Copper				
		Solder Mask		0.7	4.2	0.026
				93.7		
Material：Fiberglass made of IT-150DA	**Target Thickness：**		**2.4 mm ±0.2mm = [86.614 ~ 102.362 mils]**			

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Table 10. Characteristic impedance estimation of the motherboard PCB

Layer / Style #	W1	T	H1	H	S	Er	Zo (Ω)	Target	Tolerance
L1, L18 / 1	4.5	1.6	0.7	2.7	NA	3.44	49.40	**50**	**± 10%**
L1, L18 / 1	6.7	1.6	0.7	2.7	NA	3.44	40.55	**40**	**± 10%**
L1, L18 / 1	7.5	1.6	0.7	2.7	NA	3.44	38.10	**37.5**	**± 10%**
L3, L5, L7, L12, L14, L16 / 2	3.8	0.6	3.0	9.01	NA	3.45/3.46	49.72	**50**	**± 10%**
L3, L5, L7, L12, L14, L16 / 2	5.7	0.6	3.0	9.01	NA	3.45/3.46	39.92	**40**	**± 10%**
L3, L5, L7, L12, L14, L16 / 2	6.3	0.6	3.0	9.01	NA	3.45/3.46	37.60	**37.5**	**± 10%**
L9, L10 / 2	5.5	1.2	4	24.48	N/A	3.49/3.57	50.64	**50**	**± 10%**
Differential Signal Trace									
L1, L18 / 3	4.5	1.6	0.7	2.7	4.5	3.44	83.53	**83**	**± 10%**
L1, L18 / 3	4.5	1.6	0.7	2.7	5	3.44	85.31	**85**	**± 10%**
L1, L18 / 3	4	1.6	0.7	2.7	10	3.44	98.78	**100**	**± 10%**
L3, L5, L7, L12, L14, L16 / 4	4.5	0.6	3.0	9.01	4	3.45/3.46	83.17	**83**	**± 10%**
L3, L5, L7, L12, L14, L16 / 4	4.5	0.6	3.0	9.01	4.5	3.45/3.46	84.55	**85**	**± 10%**
L3, L5, L7, L12, L14, L16 / 4	3.5	0.6	3.0	9.01	7	3.45/3.46	100.22	**100**	**± 10%**

14.3 Appendix: OEM IPMI Command

Below are the OEM IPMI commands that shall be supported by the motherboard BMC.

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14.3.1 OEM Adlink Set LED Status (NetFn = 2Eh, Cmd=10h)

Byte	Data Field
1~3	ADLINK Manufacturer ID –005F13h, LS byte first.
4	*LED ID:* 00h=OOS (Red) LED 01h = Health (Green) LED 02h = APP LED Other values: reserved
5	*LED Function:* 00h = LED OFF override. 01h - 1Eh = LED BLINKING override. The off duration is specified by the value of this byte, and the on duration is specified by the value of byte 5. Both values specify the time in hundreds of milliseconds (100 ms-3 s). 1Fh = LED state is restored to Local Control state 20h-FEh Reserved FF = LED ON override
6	*On-duration:* The LED on-time in hundreds of milliseconds if (01h <=Byte 5<=1Eh) and ignored otherwise. Otherwise, this field is ignored and is set to 0h.
	Response Field
1	Completion Code
2~4	ADLINK Manufacturer ID –005F13h, LS byte first.

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14.3.2 OEM Adlink Get LED Status (NetFn = 2Eh, Cmd=11h)

Byte	Data Field
1~3	ADLINK Manufacturer ID –005F13h, LS byte first.
4	LED ID: 00h=OOS (Red) LED 01h = Health (Green) LED 02h = APP LED Other values: reserved
	Response Field
1	Completion Code
2~4	ADLINK Manufacturer ID –005F13h, LS byte first.
5	*LED ID:* 00h=OOS (Red) LED 01h = Health (Green) LED 02h = APP LED Other values: reserved
6	*LED Function:* 00h = LED OFF override. 01h - 1Eh = LED BLINKING override. The off duration is specified by the value of this byte, and the on duration is specified by the value of byte 7. Both values specify the time in hundreds of milliseconds (100 ms-3 s). 1Fh = LED is in Local Control state 20h-FEh Reserved FF = LED ON override
7	*On-duration :* The LED on-time in hundreds of milliseconds if (01h <=Byte 6<=1Eh) and ignored otherwise set to 0h.

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14.3.3 OEM Adlink Set NC-SI Channel (NetFn = 2Eh, Cmd=20h)

Byte	Data Field
1~3	ADLINK Manufacturer ID –005F13h, LS byte first.
4	NC-SI package selection Bits 7:3 = Reserved Bit 2:1 = 00b (select channel #0) 01b (select channel #1) 10b (select channel #2) 11b (select channel #3) Bit 0= 0b (select package #0) 1b (select package #1) Note: package is used to select ncsi network card, and channel is used to select one port of the network card.
	Response Field
1	Completion Code
2~4	ADLINK Manufacturer ID –005F13h, LS byte first.

14.3.4 OEM Adlink Get NC-SI Channel (NetFn = 2Eh, Cmd=21h)

Byte	Data Field
1~3	ADLINK Manufacturer ID –005F13h, LS byte first.
	Response Field
1	Completion Code
2~4	ADLINK Manufacturer ID –005F13h, LS byte first.
5	Active NC-SI package selection Bits 7:3 = Reserved Bit 2:1 = 00b (select channel #0) 01b (select channel #1) 10b (select channel #2) 11b (select channel #3) Bit 0= 0b (select package #0) 1b (select package #1) Note: package is used to select ncsi network card, and channel is used to select one port of the network card.

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14.3.5 OEM Adlink Set Fan Level (NetFn = 2Eh, Cmd=80h)

Byte	Data Field
1~3	ADLINK Manufacturer ID –005F13h, LS byte first.
4	Fan Tray Site Number start from 0. If all fans are controlled together, this filed takes a single number.
5	Change the FAN Control mode: 00h = restore FAN speed to local control 01h = override the current FAN level 02h = override the mini FAN level Other values are invalid.
6	FAN level to set, value range (1~10), Ignored when byte 5 is set to 00h. Fix the current FAN level when byte 5 is set to 01h Fix the mini FAN level when byte 5 is set to 02h
	Response Field
1	Completion Code
2~4	ADLINK Manufacturer ID –005F13h, LS byte first.

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14.3.6 OEM Adlink Get Fan Level (NetFn = 2Eh, Cmd=81h)

Byte	Data Field
1~3	ADLINK Manufacturer ID –005F13h, LS byte first.
4	Fan Tray Site Number start from 0. If all fans are controlled together, this filed takes a single number.
	Response Field
1	Completion Code
2~4	ADLINK Manufacturer ID –005F13h, LS byte first.
5	FAN Control mode 00h = FAN in local control 01h = Current FAN level in override control, FAN speed is fixed 02h = Mini FAN level in override control Other values are invalid.
6	Mini FAN level, value range (1~10)
7	Current FAN level value range (1~10)

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