Next Generation Software Defined Radio Operating Environment Whitepaper



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1. Introduction

Traditional Operating Environments (OE's) are struggling today to meet the high data rate performance and stringent Size, Weight and Power (SWaP) requirements of resource-constrained Software Defined Radios (SDRs). To address these challenges, a next-generation commercial-off-the-self (COTS), standards-compliant SDR OE is needed—one that is vertically-integrated and performance-optimized.

2. Overview

First generation standards-based SDR OEs—originally defined by Department of Defense (DoD) contractors on the Joint Tactical Radio System (JTRS) program (see JTRS OE box below) — have reached their performance ceiling. A new breed of OE is necessary to ensure that the exciting benefits of SDR and the JTRS program are fully realized.

JTRS OE
A standards-based SDR OE was defined by DoD contractors on the JTRS program to address radio waveform interoperability requirements. This OE, specified by the JTRS Software Communications Architecture (SCA), is comprised of a Core Framework (CF), CORBA middleware, and an Operating System (OS) with associated board support packages, as illustrated in Figure 1. The OE imposes design constraints on waveforms and other applications to provide increased portability of those applications from one radio platform to another. These design constraints include specified interfaces between the CF and application software, and restrictions on waveform usage of the OS. The SCA thus provides a development rule set focused on the detailed radio set, waveform and software development standards, and specifications that describe how to make the system designed to it interoperable. The CF is an architectural concept defining the essential, "core" set of open software interfaces and profiles that provide for the deployment, management, interconnection, and intercommunication of software application components in embedded, distributed-computing communication systems.

When the JTRS program kicked off several years ago, OEs were developed by building custom implementations of SCA-compliant CFs on top of existing COTS middleware products. Given the multi-vendor nature of these initial JTRS OE implementations, the potential for end-to-end performance optimizations was limited. Further, specialized processors, such as digital signal processors (DSPs) and field-programmable gate arrays (FPGAs) commonly used in resource-constrained platforms, interfaced with these OEs through a high-overhead custom hardware abstraction layer (HAL). The result—first generation SDR OE's are handcuffed performance-wise and struggling today to meet the increasingly high data rates and stringent SWaP requirements of resource-constrained, small form factor SDRs.

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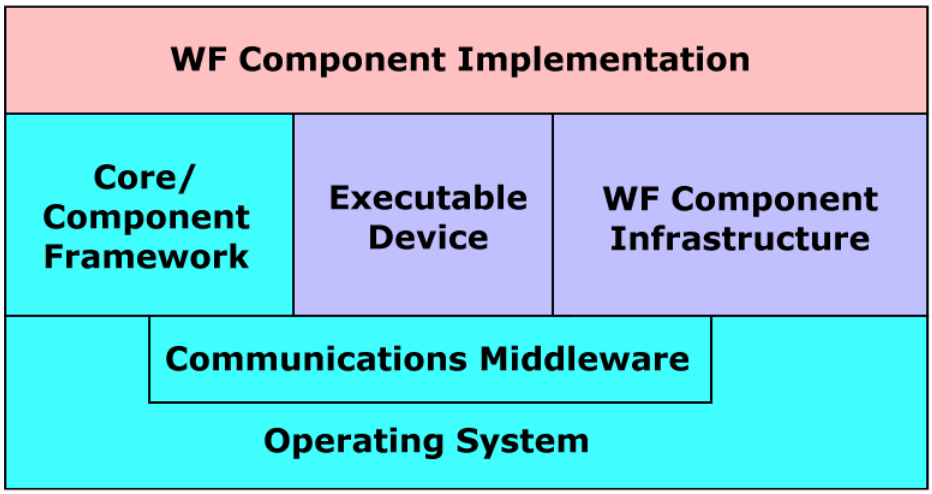


Figure 1 – Logical Architecture of a Standards-Compliant SDR

3. A Next-Generation OE

To pick up where original OEs have maxed out, next-generation COTS, standards-compliant SDR OEs need to be developed as vertically-integrated, performance-optimized products. These new OEs must feature small memory footprints and have the ability to run on any mix of general purpose processor (GPP), DSP and FPGA processor technologies. They also need to be optimized for performance across the complete run-time SDR architecture. It is this mix of qualities that will ensure that SDR is viable across a wide range of resource- constrained platforms.

In fact, there has been much promising work within the Independent Software Vendor (ISV) community on developing next-generation OEs. ISVs are developing OE solutions that can maintain the full functionality of first generation OEs, but yet are not dependent on underlying OSs or compilers to achieve small memory footprints. And maybe most appealing to system integrators and SDR developers, these next-generation platform-independent OEs provide a direct plug-and-play OE replacement for existing SDRs needing to reduce SWaP and provides SDR developers with a flexible, cost effective COTS alternative to internally developed solutions.

4. Middleware is a Critical Component

Middleware's role in next-generation OEs cannot be overstated. At its very essence, middleware provides location-transparent communications between waveform components and enables these components to be located on different processors in an SDR. Middleware is 'where the rubber meets the road' for SDR. To achieve this task, it is crucial that it operates efficiently with both the underlying OS and the CF.

However, when building their first generation SDR OE's, radio manufacturers undertook the significant effort of building custom core frameworks and integrating them with existing COTS CORBA middleware—as specified by the SCA2,3 —and OSs. Therefore, optimization potential of this multi-vendor, integrated solution is inherently limited, and has resulted in large memory footprints and suboptimal performance.

Compounding this middleware challenge is the fact that CORBA historically has been associated with large enterprise applications, not real-time embedded systems. It is only now that next-generation OEs can benefit from the significant effort that has been devoted in recent years within the middleware community to streamline CORBA for use in embedded, real-time applications.

For example, new OMG CORBA standards such as CORBA/e4 have been introduced to address the most demanding requirements of performance-based embedded applications without forfeiting the interoperability, portability and platform independence. Designed to dramatically reduce the footprint and overhead of typical enterprise middleware, this new standard eliminates much of the dynamic and resource consuming aspects of CORBA, thereby facilitating implementations that can meet the stringent requirements of real-time embedded systems such as SDRs.

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5. The Processor Challenge

To meet the stringent SWaP requirements of resource-constrained platforms, specialized processors, such as DSPs and FGPAs, are often used in the design of an SDR. Therefore, the logical SDR architecture described above should map to a physical architecture consisting of these specialized processors as well as GPPs, with waveform components executing on and communicating across all three processor types.

First generation OE designers implemented adapters, or HALs, to enable waveform components implemented on these specialized processors to communicate with components implemented on GPPs, as shown in Figure 2. These adapters required the implementation of custom message protocols which resulted in decreased portability of waveform components due to the specialized interfaces, and decreased performance (latency and throughput) due to the processing overhead of these adapters. These HALs were proprietary in nature and not based upon open standards. Waveform developers were also forced to implement custom message protocol handlers in addition to the waveform logic required to deliver radios to their customers. This handcrafting of message protocol handlers ultimately led to increases in development and maintenance costs.

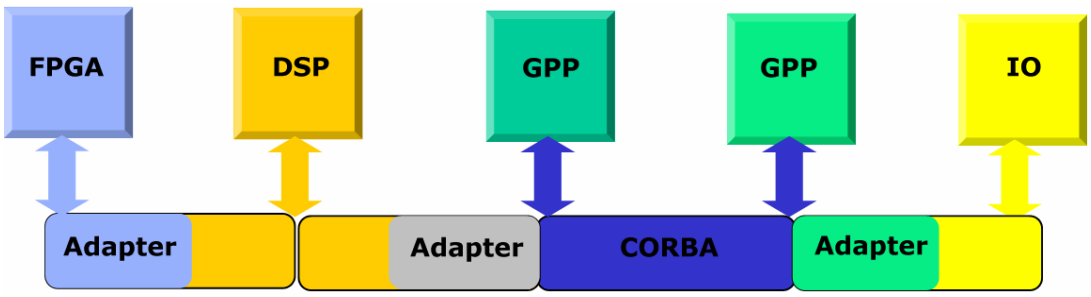


Figure 2 – Physical Architecture of First Generation Operating Environment

Today, next-generation OEs employ an alternative approach, in which the use of standards-based, COTS communications middleware is extended across all processor types, as shown in Figure 3, bringing architectural consistency throughout the SDR. For SCA-compliant SDRs, this architectural consistency had been achieved by utilizing the high performance, small footprint CORBA ORBs available on the three processor types above. Now, waveform components implemented on each of these processors may communicate with others without knowledge of their location and without the handcrafting of special protocols or adapters. This ubiquitous standard communication layer allows radio developers to re-target their software to lower cost, higher performance, lower power platforms as processor technologies continue to mature.

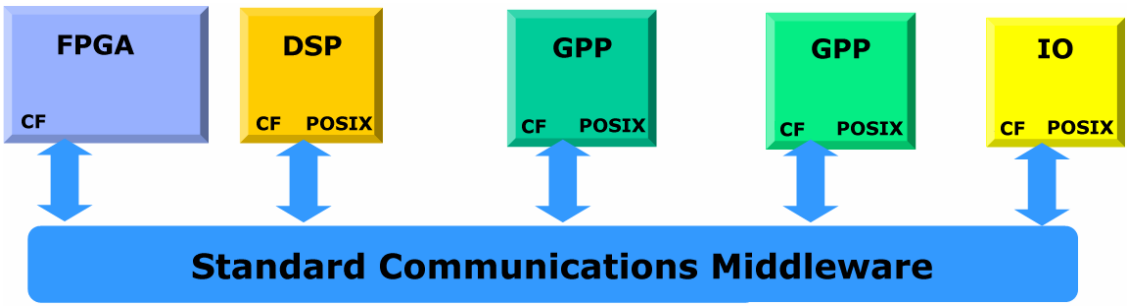


Figure 3 – Physical Architecture of Next Generation Operating Environment

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To address the resource constraints of DSPs, next-generation OE's leverage the availability of high-performance, COTS middleware specifically designed and optimized for DSPs. For example, ADLINK delivers a C language CORBA ORB utilizing 75 percent less memory than comparable C++ implementations. This dramatic saving in memory footprint, achieved without any sacrifices in performance or functionality, enables the deployment of SDR architectures on DSPs and allows a common SDR architecture to be used seamlessly across the increasingly typical processor types used in SDRs.

For FPGA-based components, hardware ORBs are used in second generation OEs to enable CORBA-based communication between FPGAs, DSPs and GPPs. Implemented as portable VHDL cores, these types of hardware ORB can be used by radio developers with FPGAs or as part of an ASIC.

This is in contrast to first generation SDR implementations that attempted to extend CORBA to FPGA's by executing a CORBA ORB on embedded processor cores within an FPGA. This approach not only failed to achieve the desired portability, consistent SDR architecture and SWaP goals of SDRs, but since adapters were still required within the FPGA, this solution also decreased throughput and increased latency.

Due to the architectural consistency of next-generation OEs, new radio platform configurations are now available to address the stringent SWaP demands of resource-constrained systems. It is now feasible to implement an SDR-compliant, handheld radio using only DSPs, or just DSPs and FPGAs, and recent proposals from the DoD are requesting SDR platforms with precisely these processor configurations.

6. The Role of CORBA ETF

Another key technology utilized in next-generation OEs is the CORBA Extensible Transport Framework (ETF). This framework allows the development of standard and efficient protocols to support optimized communication between ORBs. The ETF provides the flexibility to implement protocols other than TCP/IP (the CORBA default) for real-time systems, including highly optimized shared memory performance transports with zero copy behavior over RapidIO and compactPCI.

7. The New OMG Software Radio Specification

Additional SWaP savings can be realized by SDR OEs based upon the new OMG Software Radio Specification1 and the flexibility inherent in this standard. The standard, which represents the commercial evolution of the SCA, allows SDR developers to tailor their solutions by eliminating architectural features, as needed, to deliver only the SDR features required by their end users.

8. Conclusion

In summary, next-generation SDR OEs address SWaP concerns without constraining processor hardware choices while providing the benefits of a consistent SDR architecture. Software vendors such as ADLINK have developed small footprint, high performance OEs with a static memory footprint of well under 1MB. This 3-10X reduction in size makes standards- based SDRs viable for even the smallest of form factor applications. ADLINK also offers the Integrated Circuit ORB (ICO) for FPGA and ASIC SDR platforms to provide end-to-end architectural consistency across all processor types in use today for SDR platforms.

The availability of these next-generation OEs relieves radio manufacturers of the development and maintenance burden associated with custom OEs and significantly accelerates time to market for their SDR products. As a result, application developers using these architectures can now focus on delivering radio functionality rather than struggling to build proprietary middleware to allow communication between the disparate processors used within SDRs. The technological advances in next-generation OEs along with the commercial availability of optimized implementations for the military and commercial markets has made SDR an available reality today.

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