

Open Standard Module™ Design Guide

OSM Design Guide V1.1

November 7, 2024



Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

REVISION HISTORY

Revision	Comments	Originator	Date
1.0	Initial Release of OSM Design Guide	M. Stelter / iesy GmbH	Oct. 28, 2021
1.1	Changed IO voltage of digital PCIe signals to 1.8 V (5.3) Changed PCIe_A_PRSNT# to PCIe_CLKREQ# Removed PCIe_[A:D]_PRSNT# contacts Changed IO Voltage of PCIe_WAKE# (Table 8) Finished sentence in chapter 2.5 Changed recommendation for pull-ups on SD-Card signals (6.1 and Figure 39) Fixed typos Clarification of voltage monitoring (9.5)	M. Stelter / iesy GmbH	Nov. 04, 2024

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

CONTENTS

Revision History **2**
Contents **3**
Figures 6
Tables 8

1 Introduction **9**
1.1 Legal 9
1.1.1 Copyright 9
1.1.2 Intellectual Property 9
1.2 Disclaimers 10
1.3 General Introduction 10
1.4 Purpose of This Document 10
1.5 Design Help 10
1.6 Abbreviations and Acronyms Used 11
1.7 Document References 13
1.7.1 SGeT Documents 13
1.7.2 Industry Standards Documents 13
1.8 Schematic Example Correctness 15
1.9 Software Support 15
1.10 Schematic Example Conventions 16

2 Infrastructure: Sizes, LGA-Package, Power Delivery, System Management **17**
2.1 Module Sizes 17
2.2 LGA-Package 17
2.3 Module Power 19
2.3.1 Input Voltage Range 19
2.3.2 Input Voltage Rise Time 19
2.3.3 Module Maximum Input Power 19
2.3.4 Power Path 21
2.4 Module I/O Voltage 22
2.5 CARRIER_PWR_EN 22
2.6 RESET_IN# 22
2.7 RESET_OUT# 23
2.8 PWR_BTN# 24
2.9 Power Up Sequence 24
2.10 Sleep Mode 26
2.11 Boot Selection 27
2.11.1 Boot Definitions 27
2.11.2 BOOT_SELx# 27
2.11.3 FORCE_RECOVERY# 28
2.12 RTC_PWR 29
2.13 Reserved 29
2.14 Vendor Defined Contacts 30
2.15 Voltage Test Contacts 30

3 Display Interfaces **31**
3.1 LVDS Interface 31
3.2 Parallel RGB 31
3.3 Embedded DisplayPort (eDP) 31
3.4 MIPI DSI 32

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.5 eDP/DP++ Interface 33
3.5.1 DP over DP++ 33
3.5.2 HDMI over DP++ 34
4 Low / Medium Speed Serial I/O Interfaces 35
4.1 Asynchronous Serial Ports (UART) 35
4.1.1 RS232 Ports 35
4.1.2 RS485 Half Duplex 36
4.2 I2C Interfaces 38
4.2.1 I2C Level Translation, Isolation and Buffering 38
4.2.2 General I2C Bus EEPROMs 38
4.2.3 I2C Based I/O Expanders 39
4.2.4 Other I2C Devices 40
4.3 Touch Screen Controller Interfaces 42
4.4 I2S Interfaces 43
4.4.1 Cirrus Logic I2S Audio Example 43
4.4.2 Texas Instruments TLV320AIC3105 I2S Audio Example 43
4.5 SPI Interfaces 45
4.5.1 OSM Implementation 45
4.5.2 SPI Device Examples – 1.8 V I/O 46
4.6 CAN Bus 47
4.6.1 OSM Implementation 47
4.6.2 Isolation 48
5 High Speed Serial I/O Interfaces 49
5.1 USB 49
5.1.1 USB A Client / Host direct from Module (USB 2.0) 49
5.1.2 USB B Host direct from Module (USB 2.0) 51
5.1.3 USB C and USB D Host direct from Module (USB 3.0) 51
5.1.4 USB Hub 53
5.1.5 USB Type-C – Parade PS8750B 54
5.1.6 USB Control Signals 55
5.2 Ethernet 56
5.2.1 MAC-Interfaces 56
5.2.2 SMI-Interface 56
5.2.3 OSM Implementation 57
5.2.4 Ethernet MAC I/O Voltage Output 58
5.2.5 GBE Carrier Connector Implementation Example 58
5.2.6 GBE Mag-Jack Connector Recommendations 58
5.2.7 GBE LEDs 59
5.2.8 GBE software-defined contacts 59
5.3 PCIe 60
5.3.1 PCIe x1 Device Down on Carrier 61
5.3.2 Mini-PCIe 62
5.3.3 PCIe Reference Clock buffer 63
5.4 M.2 64
5.4.1 B keying 64
5.4.2 M keying 66
5.4.3 E keying 67
6 SDIO interface 68

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

6.1 SD Card Implementation 68
6.2 SDIO / Wireless Modules 69
6.3 SDIO I/O-Voltage 69
6.3.1 SD-Card 69
6.3.2 Other interface types 70
7 Camera Interfaces 71
8 GPIO 72
8.1 OSM Module Native GPIO 72
8.2 GPIO Expansion 72
9 Carrier Power Circuits 73
9.1 Power Budgeting 73
9.2 Carrier Input Power Sources 74
9.2.1 5 V Input 75
9.2.2 12 V Input 77
9.2.3 Wide Range Power Input 78
9.3 Power Hot Swap Controller 80
9.4 High Voltage LED Supply 81
9.5 Voltage Monitoring 82
9.6 Power Over Ethernet 83
9.7 Li-ION Battery Charger 83
10 Thermal Management 84
11 Carrier PCB Design Rule Summary 85
11.1 Decoupling for power contacts 85

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Figures

Figure 1 OSM Sizes (view from top, through the module) 17
Figure 2 Basic Module and Carrier Power Path 21
Figure 3 Reset Switch 23
Figure 4 Power Button Switch 24
Figure 5 OSM Carrier Power Up Sequence – No Power Button Case 25
Figure 6 OSM Carrier Power Up Sequence – With Power Button Case 26
Figure 7 Boot Selection Jumpers 27
Figure 8 RTC Backup: Coin Battery / Supercap 29
Figure 9 MIPI DSI 32
Figure 10 DisplayPort++ 33
Figure 11 Asynchronous Serial Port Transceiver – RS232 – TRS3253E 35
Figure 12 Asynchronous Serial Port Transceiver – RS232 – MAX13235E 36
Figure 13 Asynchronous Serial Port Transceiver – RS485 – Half-Duplex 37
Figure 14 I2C Power Domain Isolation using FETs 38
Figure 15 I2C Power Domain Isolation and Buffer 38
Figure 16 I2C EEPROM for general purpose 39
Figure 17 I2C Device: I/O Expander 39
Figure 18 I2C Device: Accelerometer 40
Figure 19 I2C Device: Accelerometer und Magnetometer 40
Figure 20 I2C Device: Gyroscope 40
Figure 21 I2S Audio Codec Cirrus Logic WM8904 43
Figure 22 I2S Audio CODEC TI TLV320AI 44
Figure 23 Audio Amplifier TI TPA2016D2 44
Figure 24 SPI Flash Socket 45
Figure 25 CAN Bus Implementation 48
Figure 26 USB A Client / Host direct from module 50
Figure 27 USB OTG – Discrete VBUS Enable through ID-Pin 50
Figure 28 USB B Host direct from Module 51
Figure 29 USB C / USB D as USB 3.0 Host Port 52
Figure 30 USB 3.0 Hub 53
Figure 31 USB Type-C – Parade PS8750B 54
Figure 32 RGMII PHY Implementation 57
Figure 33 Interfacing a PCIe x1 Carrier Board Device 61
Figure 34 Mini-PCIe Slot 62
Figure 35 PCIe Clock Buffer 64
Figure 36 M.2 Key B 65
Figure 37 M.2 Key M 66

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Figure 38 M.2 Key E 67
Figure 39 SD Card Interface 69
Figure 40 Voltage translation for SDIO voltage 70
Figure 41 Input Connector 75
Figure 42 Carrier Power Switch for 5 V / 6 A 75
Figure 43 Buck Converter 3.3 V / 2 A 76
Figure 44 Buck Converter 1.8 V / 0.6 A 76
Figure 45 Buck Converter 1.5 V / 3 A 77
Figure 46 Boost Converter for Backlight-Power 12 V / 3.2 A 77
Figure 47 Step Down Switcher 12 V to 5 V / 8 A 78
Figure 48 Wide Range 10 V - 30 V to 5 V / 12 A 78
Figure 49 Hot Swap Controller 80
Figure 50 LP8545 LED Backlight Power 81
Figure 51 Voltage monitor with Supervisor and Delay 82
Figure 52 Power decoupling 85

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Tables

Table 2 Limiting Input Power 19
Table 3 Example of Boot-Select Configuration 27
Table 4 I2C Device Examples 41
Table 5 SPI Device Examples 46
Table 6 USB Power Distribution Switch Examples 55
Table 7 SMI Interfaces 56
Table 8 PCIe Data Transfer Rates 60
Table 8 PCIe Management Contacts 60
Table 10 PCIe Interfaces Contacts (PCIE A & B) 61
Table 11 PCIe Interfaces Contacts (PCIE C & D) 61
Table 12 Hypothetical Power Budget Example 73
Table 13 Carrier Input Power Source Possibilities 74

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1 INTRODUCTION

This document is based upon the “OSM Specification V1.0” document from 2020-12-09.

1.1 Legal

1.1.1 Copyright

© Copyright 2020, SGET Standardization Group for Embedded Technology e.V.

All Open Standard Modules™ shall be published and licensed under **Creative Commons Plus (CC+)** Dual License. This allows an open license model, like Creative Commons Attribution-ShareAlike License (**CC BY-SA 4.0**) for a defined set of materials, components and software as well as for a commercial license for everything that is not included in this set. For example, block diagrams, Altium libraries and BOM might be included in the set, but not Altium design files. Thus, it is possible to license services or custom developments under a commercial license without violating the open-source idea.

1.1.2 Intellectual Property

This SGET document conforms to the current SGET® Intellectual Property Rights Policy as incorporated in the “*Agreement on Intellectual Property Rights (IPR) on work results from the working groups of the registered association SGET (SGET)*” which supplements the SGET Statutes and the SGET Standards Development Team (SDT) procedures.

Accordingly, it has to be noted that patent rights and other intellectual property rights not held by SGET may legally protect some content of this SGET document. SGET is not obligated to identify the parts of this specification that require licensing or other legitimization. The contents of this SGET document are advisory only. Users of SGET documents are responsible for protecting themselves against liability for infringement of patents. This SGET document does not contain any intellectual property known to the Standards Development Team (SDT) of this document which might be relevant for the specification defined herein, other than the intellectual property identified below. Please contact the respective patentee for further information. SGET makes no judgment as to the validity of these claims or the licensing terms offered by the claimants.

a) Intellectual property available for licensing under reasonable and non-discriminatory terms.
    a. DE patent application 10 2019 115 189.9 (iesy GmbH & Co. KG) This patent application covers certain aspects of the Open Standard Module™ specification. iesy GmbH & Co. KG has assured SGET that it is willing to provide a non-exclusive, free license of DE patent application 10 2019 115 189.9 and all intellectual property rights evolving from this patent application to those licensees (Members and non-Members alike) desiring to implement this specification.
b) Intellectual property with undetermined licensing availability:
    a. US patent US 9,510,461 (Samsung Electro-Mechanics Co., Ltd.), including patent family members
    b. KR 101548799 and
    c. CN patent CN 104241256

These patents relate to insulation of soldered joints between base boards and module boards/spacers by means of hot-melt tape, thermal bonding tape or thermosetting bonding tape The SDT believes that these patents do not directly impact the Open Standard Module™ specification which does not define such insulation. They might, however, be relevant for implementations, which seek to use additional insulation.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1.2 Disclaimers

SGET provides no warranty with regard to this SGET document or any other information contained herein and hereby expressly disclaims any implied warranties of merchantability or fitness for any particular purpose with regard to any of the foregoing. SGET assumes no liability for any damages incurred directly or indirectly from any technical or typographical errors or omissions contained herein or for discrepancies between the product and this SGET document. In no event shall SGET be liable for any incidental, consequential, special, or exemplary damages, whether based on tort, contract or otherwise, arising out of or in connection with this SGET document or any other information contained herein or the use thereof.

Compliance with this specification does not absolve manufacturers of Open Standard Module™ equipment from the requirements of safety and regulatory agencies (EN, UL, CSA, FCC, IEC, etc.).

All content and information within this document are subject to change without prior notice.

1.3 General Introduction

The idea of all Open Standard Modules™ is to create a new, future proof and versatile standard for small-size, low-cost embedded computer modules, combining the following key characteristics:

- Completely machine processible during soldering, assembly and testing
- Pre-tinned LGA package for direct PCB soldering without connector
- Pre-defined soft- and hardware interfaces
- Open-Source in soft- and hardware

The Open Standard Module™ specification allows developing, producing and distributing embedded modules for the most popular MCU32, ARM and x86 architectures. For a growing number of IoT applications this standard helps to combine the advantages of modular embedded computing with increasing requirements regarding costs, space and interfaces.

The OSM Modules are specified in the SGeT ***Open Standard Modules™ Hardware Specification 1.0***. The specification document is available free of charge from the SGeT web site (www.sget.org), subject to their terms of use.

Similarly, this ***OSM Design Guide*** is available free of charge from the SGeT web site, subject to the SGeT terms of use.

1.4 Purpose of This Document

The primary purpose of this document is to serve as a Design Guide for developers of OSM Carrier Boards and for OSM Module customers who wish to have a OSM based system developed.

A secondary purpose of this document is to serve as a reference to OSM Module developers, to help them understand the application of the Modules they are developing.

Finally, this document should be valuable to FAEs and Product managers to help them understand the OSM Module infrastructure.

1.5 Design Help

There are number of ways to have a OSM Carrier board developed:

- Design internally, but have your OSM Module vendor review your design. Make sure to also have the appropriate semiconductor companies review the portions of the design that utilize their components.
- Use a 3rd party firm that specializes in OSM Carrier development. Such resources may be listed on the SGeT web page (www.sget.org).
- Contact your OSM Module vendor. The Module vendor will have an FAE available for advice. Many vendors will also undertake custom Carrier design projects, for significant opportunities.

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1.6 Abbreviations and Acronyms Used

- **ADC** Analog to Digital Converter
- **ARM** Advanced RISC Machines _____ www.arm.com
- **BCT** Boot Configuration Table
- **BSP** (software) Board Support Package
- **CAD** Computer Aided Design
- **CAN** Controller Area Network
- **CSI** (MIPI) Camera Serial Interface _____ www.mipi.org
- **DAC** Digital to Analog Converter
- **DNI** Do Not Install (component is not loaded)
- **DP** DisplayPort
- **DP++** Dual-mode DisplayPort
- **DSP** Digital Signal Processor
- **DSI** (MIPI) Display Serial Interface _____ www.mipi.org
- **EDID** Extended Display Identification Data _____ www.vesa.org
- **EEPROM** Electrically Erasable Programmable Read Only Memory
- **e-MMC** Embedded Multi Media Card _____ www.jedec.org
- **ESD** Electro Static Discharge
- **GBE** Gigabit Ethernet _____ www.ieee.org
- **Gbps** Gigabit per second
- **GPIO** General Purpose Input / Output
- **HDMI** High Definition Multimedia Interface _____ www.hdmi.org
- **IC** Integrated Circuit
- **I2C** Inter-Integrated Circuit _____ www.nxp.com
- **IO** Input Output (also I/O)
- **ISO** International Organization for Standardization (French) _____ www.iso.org
- **JEDEC** Joint Electron Device Engineering Council _____ www.jedec.org
- **LED** Light Emitting Diode
- **Li-Ion** Lithium Ion (rechargeable battery technology)
- **LVDS** Low Voltage Differential Signaling
- **M2.5** Metric 2.5mm
- **M3** Metric 3.0mm
- **MAC** Media Access Controller (e.g. logic circuits in GBE)
- **Mbps** Megabit per second
- **MIPI** Mobile Industry Processor Interface _____ www.mipi.org
- **MOD** Module (the OSM Module) (schematic notation)
- **NC** Not Connected
- **NXP** NXP Semiconductors - A semiconductor company _____ www.nxp.com
- **OS** Operating System
- **OSM** Open Standard Module™ _____ www.sget.org
- **OTG** On the Go (USB term – device can be host or client)

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

- **PCB** Printed Circuit Board
- **PHY** Physical (transceiver) – drives cable or other physical media
- **PICMG** PCI Industrial Computer Manufacturing Group _____ www.picmg.org
- **PCI** Peripheral Component Interface _____ www.pcisig.org
- **PCIe** PCI Express _____ www.pcisig.org
- **PCI-SIG** PCI Special Interest Group _____ www.pcisig.org
- **PCM** Pulse-Code Modulation
- **PD** See USB PD
- **PLL** Phase Locked Loop
- **POE** Power Over Ethernet
- **PWM** Pulse Width Modulation
- **RGB** Video data in Red Green Blue pixel format
- **RS232** Recommend Standard 232 (asynchronous serial ports)
- **RS485** Asynchronous serial data, differential, multidrop
- **RTC** Real Time Clock (battery backed clock and memory)
- **SAR** Successive Approximation Register
- **SATA** Serial ATA (serial mass storage interface) _____ www.sata-io.org
- **SD** Secure Digital (memory card) _____ **www.sdcard.org**
- **SE** Single Ended (signal, as opposed to differential)
- **SGeT** Standardization Group for Embedded Technologies _____ www.sget.org
- **SOC** System On Chip
- **SPI** Serial Peripheral Interface
- **SSD** Solid State Drive
- **TI** Texas Instruments – semiconductor company _____ www.ti.com
- **UART** Universal Asynchronous Receiver Transmitter
- **USB** Universal Serial Bus _____ www.usb.org
- **USB PD** USB extension specification for Power Delivery _____ www.usb.org
- **VESA** Video Electronics Standards Association _____ www.vesa.org
- **WiFi** **Wireless connection IEEE 802.11**
- **X5R** Ceramic capacitor dielectric – good quality (-55 °C…85 °C)
- **X7R** Ceramic capacitor dielectric – better quality (-55 °C…125 °C)
- **x86** Intel architecture (80x86) CPUs

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1.7 Document References

1.7.1 SGeT Documents

- ***Open Standard Module Hardware Specification***, V 1.0, Dec. 09, 2020 © SGeT (Standardization Group For Embedded Technologies) www.sget.org

1.7.2 Industry Standards Documents

- ***CAN*** ("Controller Area Network") Bus Standards
  ISO 11898-1:2015 Road vehicles - Controller area network (CAN) - Part 1: Data link layer and physical signaling, (https://www.iso.org)
  ISO 11992-1:2019 Road vehicles - Interchange of digital information on electrical connections between towing and towed vehicles - Part 1: Physical and data-link layers (https://www.iso.org)
  SAE J2411: Feb 14, 2000, Single Wire CAN Network for Vehicle Applications (https://www.sae.org)
- ***MIPI CSI-2*** (Camera Serial Interface version 2) The MIPI CSI-2 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (www.mipi.org)
- ***MIPI CSI-3*** (Camera Serial Interface version 3) The MIPI CSI-3 standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (www.mipi.org)
- ***DisplayPort and Embedded DisplayPort*** These standards are owned and maintained by VESA ("Video Electronics Standards Association") (www.vesa.org)
- ***MIPI DSI*** (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance ("Mobile Industry Processor Alliance") (www.mipi.org)
- ***eMMC*** ("Embedded Multi-Media Card") The eMMC electrical standard is defined by JEDEC JESD84-B51A and the mechanical standard by JESD84-C44 (www.jedec.org)
- ***eSPI*** ("Enhanced Serial Peripheral Interface") The eSPI Interface Base Specification is defined by Intel (https://www.intel.com)
- ***GBE MDI*** ("Gigabit Ethernet Medium Dependent Interface") this is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- ***HDMI Specification***, Version 2.1, November 28, 2017 (www.hdmi.org)
- ***I2C Specification***, Version 6.0, April 4th 2014, NXP Semiconductor (now NXP) (www.nxp.com)
- ***I2S Bus Specification***, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- ***IEEE1588 - 2008***. IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems
  (*http://standards.ieee.org*)
- ***JTAG*** ("Joint Test Action Group") This is defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture
  (https://ieeexplore.ieee.org)
- ***PCI Express*** Specifications (www.pci-sig.org)
- ***RS-232*** (EIA "Recommended Standard 232") this standard for asynchronous serial port data exchange dates from 1962. The original standard is hard to find. Many good descriptions of the standard can be found on-line, e.g. at Wikipedia, and in text books.
- ***Serial ATA*** Revision 3.1, July 18, 2011, Gold Revision, © Serial ATA International Organization (www.sata-io.org)
- ***SD Specifications*** Part 1 Physical Layer Simplified Specification, Version 3.01, May 18, 2010, SD Group and SD Card Association
  ("Secure Digital") (www.sdcard.org)
- ***SM Bus*** – "System Management Bus" Specification Version 3.1, March 19, 2018, System Management Interface Forum, Inc.
  (http://www.smbus.org)
- ***SPI Bus*** – "Serial Peripheral Interface" – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- ***UL 1642 Lithium Batteries –*** safety standard governing the use of lithium batteries (www.ul.com)
- ***USB Specifications*** (www.usb.org)

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

- ***VESA Enhanced Extended Display Identification Data Standard,*** Rev. 1, Feb 9, 2000, VESA (www.vesa.org) See also the "EDID" page on Wikipedia.

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1.8 Schematic Example Correctness

The schematic examples shown in this Design Guide are believed to be correct, but correctness cannot be guaranteed. Most of the examples have been pulled from designs that have been built, tested, and are known to work. Most of them have been re-formatted to fit better in this design guide.

Note: Designer should consider datasheet, user-guides and reference schematics of components used in own Carrier Board designs. In case of conflicts with schematics shown in this document than manufacturer documents have higher priority.

Note: The selection of the proper power domain (Sleep/ Standby/ RunTime) may not be reflected in the schematic parts. Please make sure to connect the needed power source in your design as your application requires it. If in doubt, please also consider the OSM Hardware Specification for additional input and to prevent back powering to the Module.

1.9 Software Support

Many hardware examples and suggestions are given in the following pages. OSM Carrier hardware design is generally straightforward. However, before committing to a particular hardware selection, it is wise to check out the software driver support. A particular device may be supported in particular OS systems for example, in Linux but not in Windows. Your overall project may go smoother if you pick out hardware that already has software support in your target OS.

There are various possible sources for software drivers for a particular IC: the IC vendor, the OS vendor, the OS community, your Module vendor, your Carrier design partner, other independent sources and of course writing your own.

Most OSM Module vendors offer a BSP (Board Support Package) for their Module. Your target Carrier device may be supported in the BSP – check this angle out as well.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1.10 Schematic Example Conventions

This part will be released in future revision of this documentation.

V_IN_RAW	Power-In to the overall system, before any filtering, fusing, polarity or rise time protection.
V_IN	Power-In to the overall system, after (optional) filtering, fusing, polarity or rise time protection.
V_MOD_IN_3V3	Power into the OSM Module VCC_IN_3V3 contacts. Primary used for Size-0 modules.
V_MOD_IN_5V	Power into the OSM Module VCC_IN_5V contacts. Primary used for Size-S, Size-M and Size-L modules.
V_CARRIER_IN	Power into the Carrier Board. It may be the same as V_MOD_IN, depending on the design at hand. On OSM Evaluation Carrier boards, V_CARRIER_IN is sometimes kept separate from V_MOD_IN to allow easier measurements and tracking of where the power goes.
V_5V0	5V supply on the Carrier Board
V_3V3	3.3V supply on the Carrier Board
V_1V8	1.8V supply on the Carrier Board
V_1V5	1.5V supply on the Carrier Board

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2 INFRASTRUCTURE: SIZES, LGA-PACKAGE, POWER DELIVERY, SYSTEM MANAGEMENT

2.1 Module Sizes

The Open Standard Module™ is made up of four different sizes that build upon each other:

- Size-0 – "Zero": 30 mm x 15 mm / with 188 contacts → shown below with red outlines
- Size-S – "Small": 30 mm x 30 mm / with 332 contacts → shown below with blue outlines
- Size-M – "Medium": 30 mm x 45 mm / with 476 contacts→ shown below with orange outlines
- Size-L – "Large": 45 mm x 45 mm / with 662 contacts → shown below with green outlines

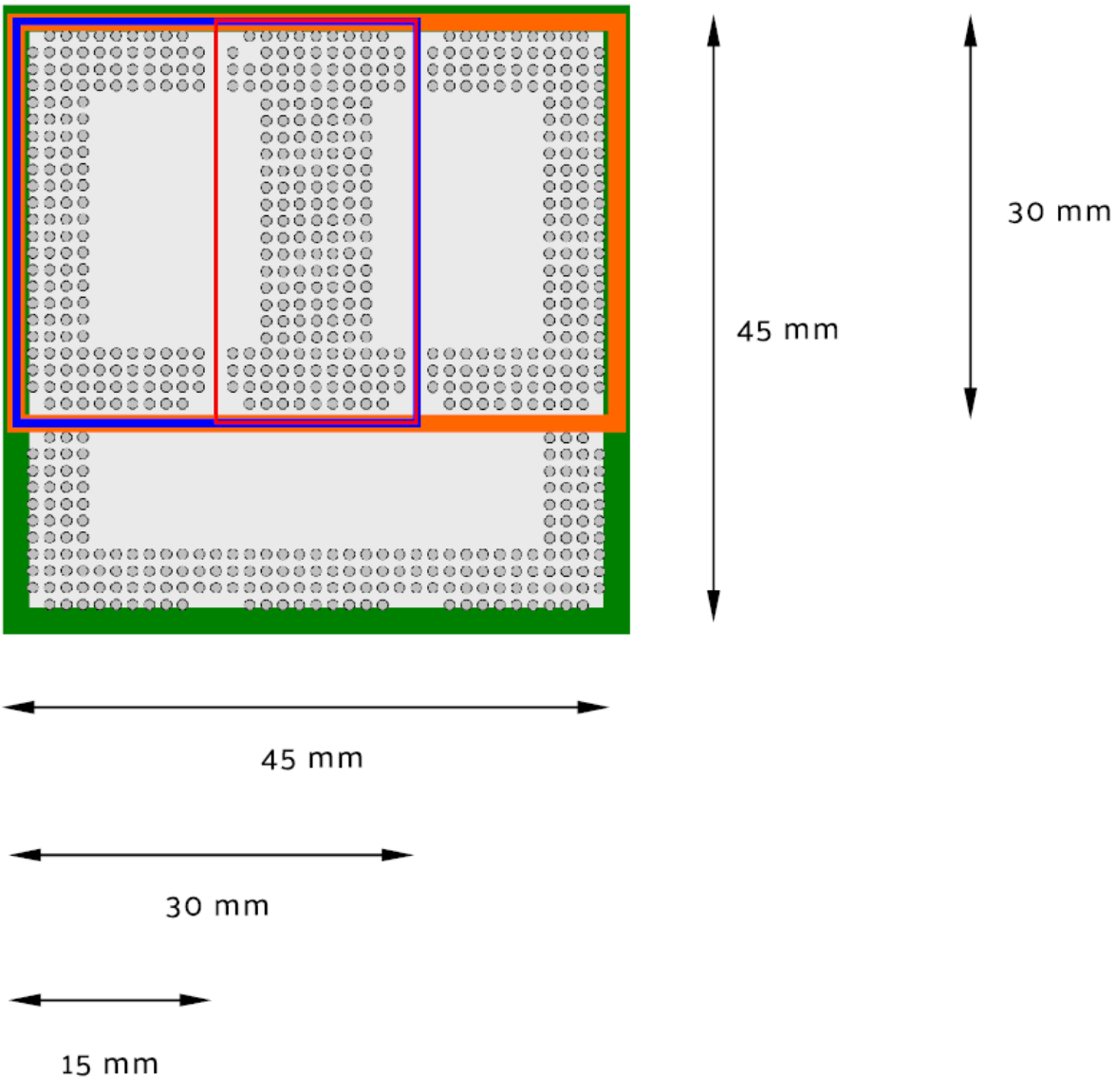


Figure 1 OSM Sizes (view from top, through the module)

Detailed contact descriptions are given within the OSM Hardware Specification.

2.2 LGA-Package

The OSM Modules are directly soldered on the Carrier Board PCB.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

The OSM Module contacts are well described in the ***Open Standard Module Hardware Specification V1.0*** and the complete description is not repeated here.

Briefly, the OSM Module footprint has up to 662 solder pads with 1,25 mm pitch.

The four different OSM Modules sizes has the same contact functions compared to the smaller sizes. This means a Carrier Board can be designed for more than one module size.

The detailed footprint is also described in the ***Open Standard Module Hardware Specification V1.0***

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.3 Module Power

2.3.1 Input Voltage Range

The primary supply voltage depends on the OSM Module size. A single supply of 5 V is recommended for Size-S, Size-M and Size-L on up to 17 contacts (VCC_IN_5V).

As OSM Module Size-0 is mostly relevant for low power microcontroller with single voltage supply of 3,3 V the recommended input voltage for Size-0 is 3,3 V at one single contact (VCC_IN_3V3).

This allows module vendors to follow SOC design guidelines by using integrated power management controllers supplied by a single supply voltage higher than all on-module supply voltages.

Both power inputs are available on all module sizes.

Note: There may be modules which does not follow the recommended power input given above. To allow flexible Carrier Board design the module supply can be designed for optional 3,3 V or 5 V per selection of the switching regulator output voltage. However, for modules using both power inputs there can be further sequence requirements to follow. Contact the module vendor in early design state to fulfill requirements and allowing compatibility for other vendors.

There are optional power inputs for battery voltage (V_BAT) which can be used for low power applications.

2.3.2 Input Voltage Rise Time

There are currently no limits in the OSM Module Hardware Specification on the Module power supply rise times. In general, it is not wise to expose the Module and Carrier electronics to extremely fast power supply rise times (as may be the case if a low impedance power source such as a battery pack or power brick is “hot-plugged”). Input power supply rise times faster than 50 V/ms to the Module should be avoided.

If a unit is to be “hot-plugged” to a low impedance power source, then the Carrier should implement functions to slow the power rise time that are seen by the Module and Carrier circuits. The Carrier can do this by implementing a FET and hot-swap controller in the input power path. This is discussed in section 9.3

2.3.3 Module Maximum Input Power

The OSM specification V1.0 document states that the allowable input voltage range is typ. 3.3 V (VCC_IN_3V3) or 5 V (VCC_IN_5V) for Modules that are using higher power CPUs/ SOCs.

The OSM Module physical contact consists of a soldered connection able to carry a current of minimum 0.5 A per contact.

Depending on the module size there are different amounts of contacts for the power input VCC_IN_5V thus the limited input power differs for each module size. The following table shows the amount of input power contacts and the allowed maximum input power.

Table 1 Limiting Input Power

Module Size	VCC_IN_3V3		VCC_IN_5V	
	Contacts	Input Power	Contacts	Input Power
Size-0	1	1.65 W	1	2.5 W
Size-S			5	12.5 W
Size-M			9	22.5 W
Size-L			17	42.5 W

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

There are up to 132 GND contacts for signal and power return (Size-L).

Depending on the use case of the product and Carrier Board it is suggested to develop the Carrier Board power supply for the OSM module with some overhead in order to be able and use multiple platform generations with one design. Please refer to the OSM module datasheet and manuals or contact your module vendor for more information.

Note: Table 1 in most cases will show much higher power values than one module vendor specifies for his own module. Values should be seen as highest power suitable in for the OSM concept.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.3.4 Power Path

The power path for a basic, fixed input voltage arrangement OSM Module and Carrier board system is shown in Figure 2 below. A number of features in the figure are optional and may be omitted (and bypassed) in a minimal implementation. The figure also shows Carrier power supply sections assuming a typical system powered by a power source of typ. 12 V.

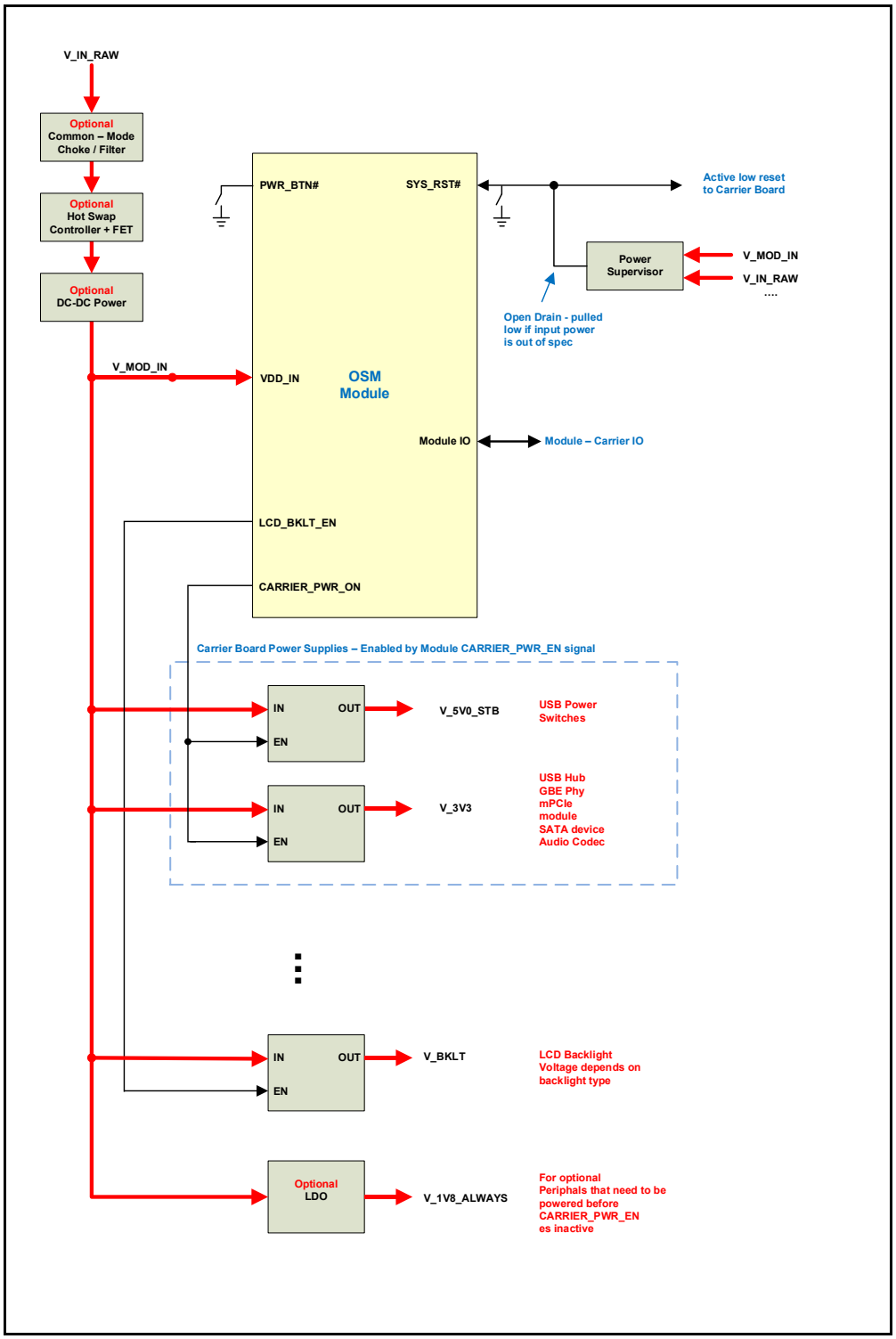


Figure 2 Basic Module and Carrier Power Path

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Note:

- The real implementation of the voltage rails is Carrier Board dependent. This figure shall only illustrate how the different signals are used to control the power rails.

2.4 Module I/O Voltage

The OSM Module Hardware Specification specifies a main I/O voltage level of 1.8 V. However there are further I/O voltages due to interface specifications like for USB or optional I/O Level of 1.8 V / 2.5 V / 3.3 V for Ethernet.

In addition only for Size-0 Modules the I/O level for all contacts are defined by the module itself and can be used by the Carrier Board on contact VCC_OUT_IO. For other sizes than Size-0 this contact is NC, thus the I/O level is defined by the OSM Module Hardware Specification (mainly 1.8 V). This feature is necessary as some of the microcontroller for Size-0 are expected to be not flexible in I/O voltage and directly using their single input voltage of 3.3 V for I/O as stated in 2.3.1.

The minimum current that an OSM Module must deliver for Carrier Board components at VCC_OUT_IO is 100 mA. This can be used for I/O Level shifter to connect OSM Modul to 1.8 V periphery or to be detected on Carrier Board to allow switching of I/O voltage supply on Carrier Board.

I/O at 1.8 V is used in general for low power interfaces. Many contemporary peripherals of interest are available with I/O interfaces that support 1.8 V and 3.3 V; some are available at 1.8 V only, and others at 3.3 V only. Specific examples are given in various document sections below.

If devices that support only 3.3 V are implemented, a level shifter must be used to interface them to the OSM Module. This is discussed in section 4.2.1. I2C Level Translation, Isolation and Buffering below.

Note: Some signals also might be in use on the OSM module so that Inputs (to the Module) that are not needed on the Carrier should be left floating from the Carrier side.

2.5 CARRIER_PWR_EN

The CARRIER_PWR_EN signal is driven by the module at 1.8 V level. It is a high active output to signal that the Carrier Board power supplies are allowed to be powered up. Normally this signal is integrated within the module internal power up sequence and is switched high within the last sequence before reset release.

Note: Implementation of this signal on the Carrier Board is strongly recommended as it prevents cross supplying through I/O domains that are powered down on the module. Cross supplying can result in boot failure, latch-ups and permanent device damage due overdriving the voltage protection of the IO pads on the CPU / controller die.

2.6 RESET_IN#

The RESET_IN# signal is driven by the Carrier Board and must only be pulled to ground or left floating. It has an internal on-module pull up to 1.8 V. This signal may be used to force the Module to stay in reset and can be forced to low at any time.

This allows a device on the Carrier to pre-load its content (such as an FPGA) and to setup strap options before the Module is latching the bootstraps or executes any code. If used, by the Carrier, then an open drain device or switch to GND should be used. A switch example is shown in Figure 3. The signal is ESD protected in this example, as the switch (and the switch interaction with humans) introduces an ESD hazard.

There is no restriction within OSM Specification about level or edge transitions. This must be specified by module vendor.

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

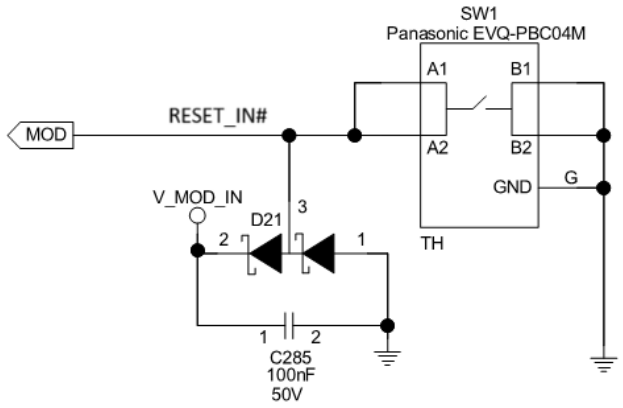


Figure 3 Reset Switch

Note: Repeatedly use of the RESET_IN# signal while the Module is already performing a reset cycle might lead to unknown behavior of the Module and therefore shall be avoided.

2.7 RESET_OUT#

Contact RESET_OUT# is an optional push-pull output and was added in OSM Specification V1.2. This contact can be used to perform a board reset by on-module components like Power Management Controller, Microprocessors or Watchdog.

Normally RESET_OUT# is connected to the reset inputs of different baseboard controller (PHYs, Hubs) to hold interface function in reset state while CPU is booting or in failure mode.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.8 PWR_BTN#

OSM defines a contact to allow the implementation of a Carrier based power button. However the OSM Hardware Specification does not define the power up behavior of a Module. The following possibilities exist after a cold power on:

a) Module boots

b) Module waits for a Power Button press to boot

c) The Module is configurable – either behavior a) or behavior b) may be configured

Users are advised to check with your Module vendor about this topic. A Power Button switch example is shown in the Figure 4. If your Module waits for a Power Button press on power up and you want it to always boot on power up, you have to arrange for a “power button press” on power up, using an open drain device to interface to the OSM Module.

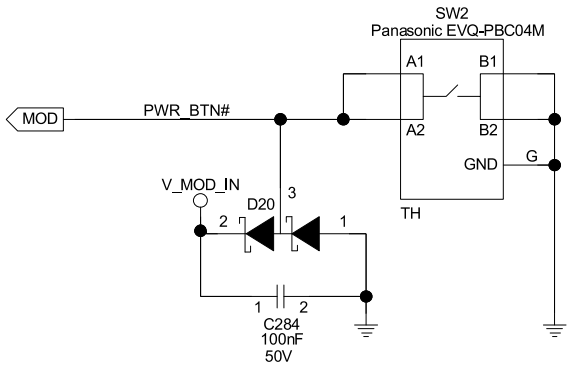


Figure 4 Power Button Switch

Note: Contact PWR_BTN# is not available for module size Size-0.

2.9 Power Up Sequence

The basic power up sequence for OSM Modules and Carriers is shown in the following two figures. There is a Module design and / or configuration dependence with regard to the power button behavior. Depending on design and / or configuration, the Module may always boot without waiting for a power button press, or it may wait for a power button press. These cases are shown in below figures.

It is recommended to arrange that the main Carrier power supplies do not come up until the Module asserts the CARRIER_PWR_EN signal (see section 2.5 CARRIER_PWR_EN). When this signal is high, you know that the Module power supplies are all up. If the Carrier power is up before the Module supplies are up, there is a risk that the Carrier circuits will back-feed power to the Module I/O pins, which might interfere with a Module boot.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

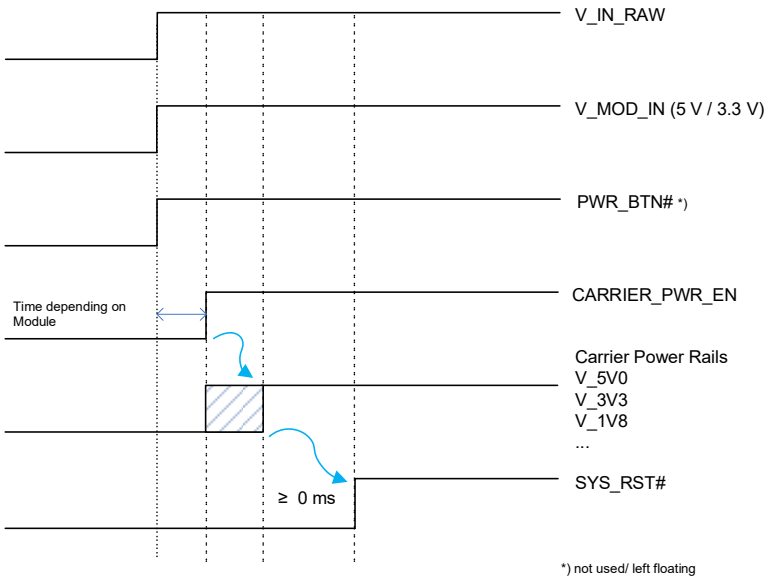


Figure 5 OSM Carrier Power Up Sequence – No Power Button Case

The diagram below reflects the case of a Module that is designed or configured to wait for a power button press before it comes up. When power is applied to the Module, in this case, only a small portion of the Module is using that power – typically, the Module Power Management section – and that circuitry waits for a power button press (PWR_BTN#). When it sees one, the Module proceeds with the boot. When the main Module power rails are up, the Module asserts CARRIER_PWR_EN. The Carrier should use this signal to enable the various Carrier power rails. However, the Carrier circuits that are involved in power management (battery charge level, reset monitors, etc.) may be powered ahead of CARRIER_PWR_EN, coincident with the Module power.

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

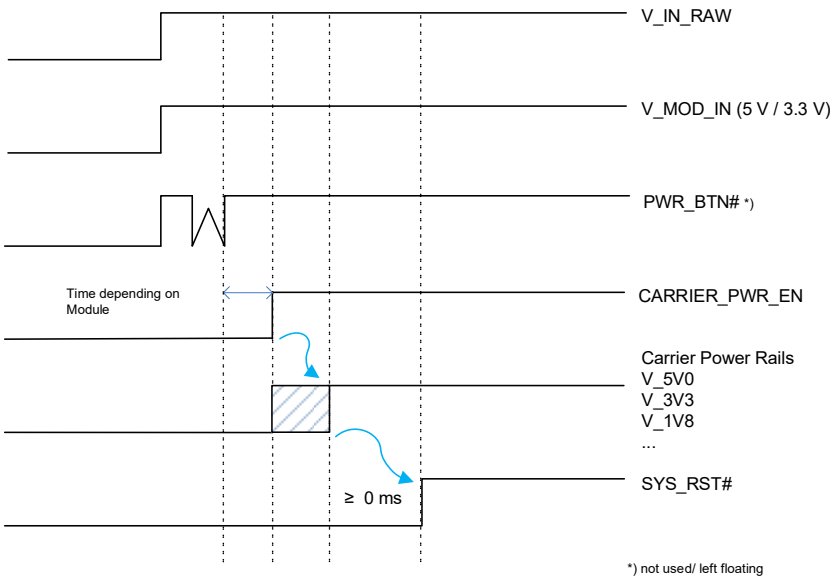


Figure 6 OSM Carrier Power Up Sequence – With Power Button Case

2.10 Sleep Mode

OSM doesn't specify Sleep Mode functions but there are two possible ways to implement these function if necessary:

- Using CARRIER_PWR_EN to signal standby and switch of all interfaces not needed – As stated in chapter 2.5 this will not allow to use any voltages applied to the module
- Using one of the vendor contacts to switching off portions of voltage domains to allow minimal Carrier Board functions

In Order to Wake from the Sleep Mode the PWR_BTN# and if implemented the SMB_ALERT# signals can be used. Please refer to your Module documentation about the implementation of your Module.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.11 Boot Selection

2.11.1 Boot Definitions

This part will be released in future revision of this documentation.

2.11.2 BOOT_SELx#

The OSM Hardware Specification defines two low active input contacts BOOT_SEL0# and BOOT_SEL1# which may be used to tell the Module what physical device to do a BCT boot from.

As allowed boot media differ between Module Vendors there is no fixed boot configuration within OSM Specification. How ever Module Vendor must specify the configuration necessary on Carrier Board.

An example of a boot table delivered by OSM Module Vendor is shown in Table 2. BOOT_SELx# only has to be pulled down or left floating as there are 10 kΩ on-module pull-ups.

Table 2 Example of Boot-Select Configuration

BOOT_SEL1# (R18)	BOOT_SEL0# (U19)	Boot Source	Boot Device
GND	GND	Carrier	SD-Card
GND	Float	Module	e-MMC
Float	GND	Carrier	SPI-Flash
Float	Float	Module	SPI-Flash

The Module BOOT_SELx# contacts may be set by jumpers on the Carrier Board, as shown in the Figure 7 below. The diodes and capacitors are for ESD protection, as the jumpers may experience ESD events.

Alternatively, the BOOT_SELx# contacts can be set by low value option resistors to GND on the Carrier. The resistors are either installed (for a GND connection) or not installed, per the Table 2 .

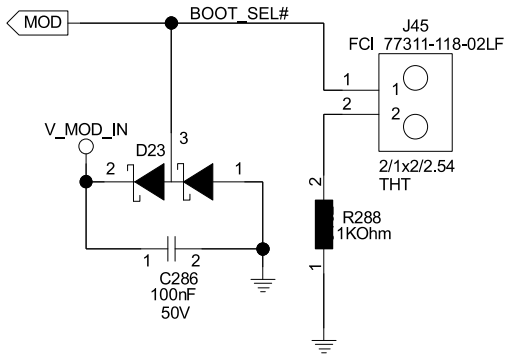


Figure 7 Boot Selection Jumpers

Note: The Boot Select implementation of the Modules may not be available on all Modules. It is platform and vendor specific if none, some or all of options mentioned above are available. Also it might be that the Boot Select will work so that the first code fetch from the Module is on the listed device or that the SOC is always fetching the first code lines from a fix device and only then reacts on the pin selection. Please get in contact with your Module vendor for more details about a specific product.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.11.3 FORCE_RECOVERY#

Some Modules support a “force recovery” function in which the primary boot media can be re-initialized over a designated I/O interface, such as a USB client interface, asynchronous serial port, or Ethernet port. This is Module specific; refer to your Module documentation for further details.

Implementation can be done as for BOOT_SELx# with jumpers, resistor configuration or push buttons as shown in 2.11.2.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

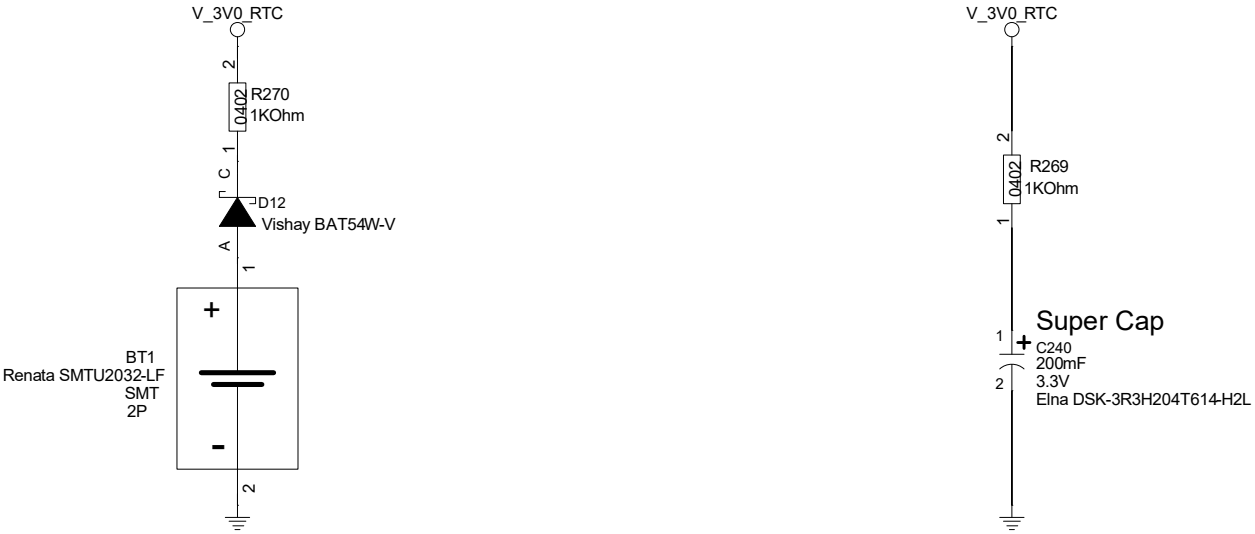
2.12 RTC_PWR

The Module RTC (Real Time Clock) circuit requires a backup power source if the Module RTC circuit is expected to keep time in the absence of the primary power source (i.e. the power to Module VCC_IN_5V or VCC_IN_3V3). The RTC backup power, if used, is applied to the Module RTC_PWR contact. The RTC backup power may be provided by a battery (coin cell) or by a large value capacitor, known as a "Supercap". The typical voltage is 3 V. The voltage range necessary for time keeping is vendor specific.

If a battery is used, the battery is typically a small lithium coin cell with a capacity of a few hundred mAh. Lithium coin cells offer a high energy density, low self-discharge rate, and are not rechargeable. For safety reasons, they must be protected against charging **on the Carrier board** by a redundant set of circuit elements – typically either two diodes in series or a diode and a resistor. The resistor, if used, must be large enough to limit the battery charging current to be equal to or lower than the amount specified as allowable by the battery vendor. The safety aspects of lithium battery use is governed by a UL document (***UL 1642 Lithium Batteries***, www.ul.com).

The Supercap solution differs from the lithium battery solution in that it needs to be charged by the Module (when the Module has its primary power source); hence a blocking diode should not be used with the Supercap.

The time period over which the RTC backup power is effective depends on the Module RTC backup current draw, the exact voltage range over which the Module RTC circuit is functional, on the capacity characteristics of the battery or Supercap, on the drops incurred across the Carrier board circuit protection elements, and on the operating temperature. In general terms, a suitable lithium battery solution can provide RTC backup current on a scale of years whereas the Supercap solution on a scale of days to weeks.



Coin Battery Holder, R/A, SMT

Figure 8 RTC Backup: Coin Battery / Supercap

2.13 Reserved

The Module RESERVED contacts (up to 36 contacts for Size-L) should normally be left unconnected and may be used in future revisions of the OSM specification.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

2.14 Vendor Defined Contacts

Because of SOC and architecture specific reasons there may be the requirement for module specific functions of power-management or interface signals. They may be not covered by known standards. OSM Hardware Specification fulfills this need by adding up to 17 vendor specific contacts.

Note: Please get in contact with your Module vendor for more details about a vendor specific function. Do not connect these contacts when specification is unknown.

2.15 Voltage Test Contacts

Up to 7 dedicated contacts (VCC_x_TEST) for voltage testpoints are specified. These contacts are intended to be used by module vendor for test procedures. Usage and voltages are vendor specific. See module specification if connection of these contacts on own Carrier Board is allowed or must be unconnected.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3 DISPLAY INTERFACES

The module can support display outputs with the standards parallel RGB, MIPI DSI, eDP/eDP++ and LVDS. All interfaces are using dedicated contacts.

The contacts for eDP/eDP++ interface can be configured for HDMI mode (see chapter 3.5).

3.1 LVDS Interface

This part will be released in future revision of this documentation.

3.2 Parallel RGB

This part will be released in future revision of this documentation.

3.3 Embedded DisplayPort (eDP)

This part will be released in future revision of this documentation.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.4 MIPI DSI

OSM modules can support one MIPI DSI (Display Serial Interface). DSI is a high-speed differential bus and includes one clock lane and up to four data lanes. There is no AC coupling required.

VDD and Backlight signals are not specified by the OSM Module Hardware Specification.

It is recommended to check with your OSM Module vendor if MIPI DSI is supported by the OSM Module and how much data lanes are used.

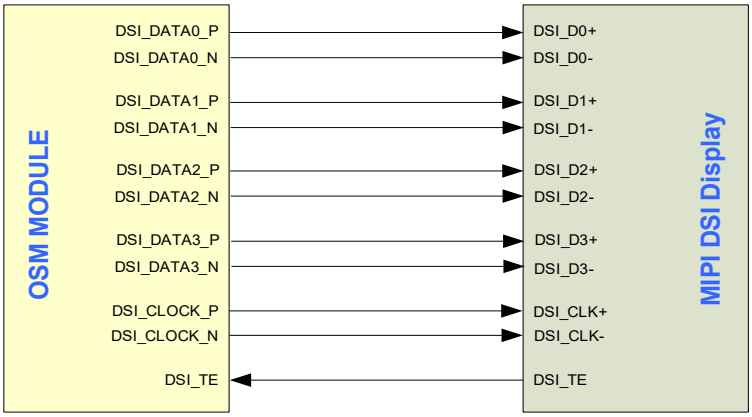


Figure 9 MIPI DSI

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.5 eDP/DP++ Interface

There are up to two eDP/DP++ interface specified that can be either used as eDP, DP or HDMI interface. It also allows the use of DP++ to HDMI dongles.

3.5.1 DP over DP++

DisplayPort is directly supported by a dual-source DDI. ESD protection, DC blocking capacitors and hot plug detect are the only components required.

The DisplayPort differential data pairs are AC coupled off Module with capacitors C19-C26. Place the AC blocking capacitors close to the DisplayPort connector. The Aux differential pair is AC coupled off the Module. ESD clamping diodes D1, D2 and D3 protect the Module from external ESD events and should be placed near the DisplayPort connector. The pin-out of the ESD clamp diodes allows for a trace to run under the chip connector to two pins.

The Carrier provides up to 500 mA of 3.3 V power to the DisplayPort connector. Diode D71 prevents back feeding of power in the event that the monitor is powered up when the Carrier is powered down.

Config lines 1 and 2 are pulled to ground per the VESA specification.

The DisplayPort Hot Plug Detect signal is buffered by U50 which prevents back feeding of power from the display to the Module as well as level translation to 3.3 V levels on the connector side.

R14 connect logic and chassis ground together. Other techniques may be used depending on the overall grounding strategy.

Note: The reference schematics assume that the Module's DisplayPort is dual-source capable – dual source indicates that the Module can output DisplayPort or HDMI/DVI based on the eDP_x_AUX_SEL signal.

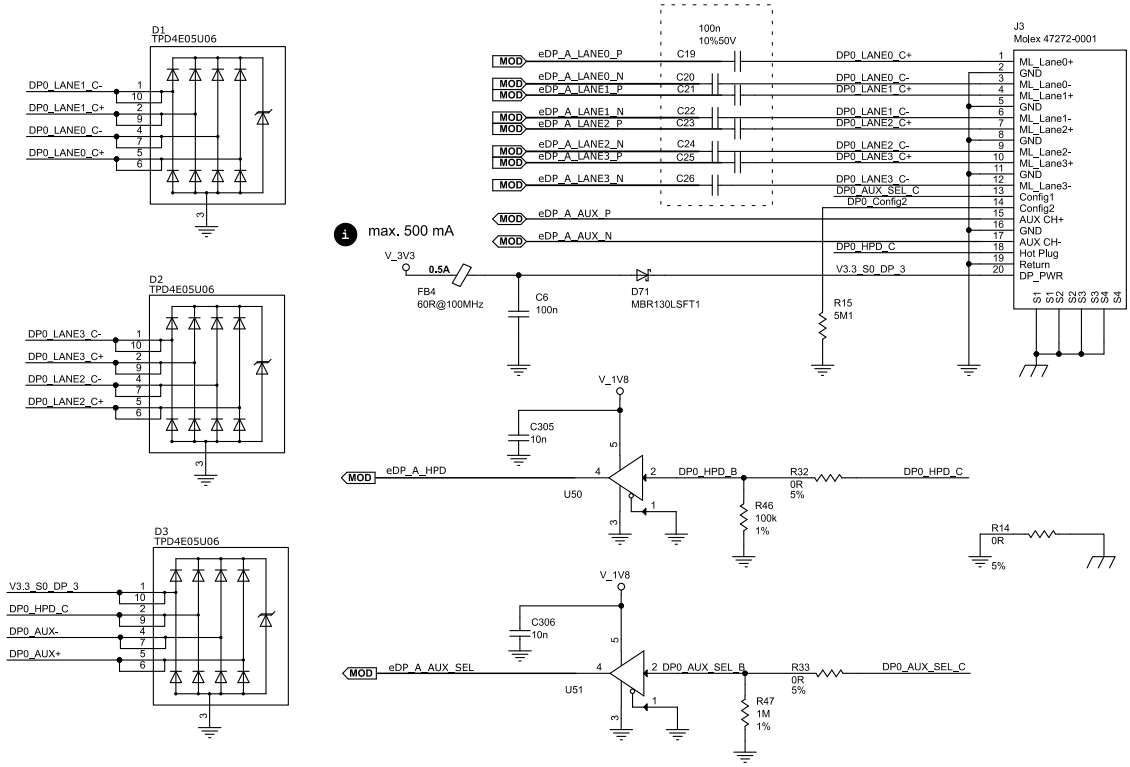


Figure 10 DisplayPort++

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3.5.2 HDMI over DP++

This part will be released in future revision of this documentation.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4 LOW / MEDIUM SPEED SERIAL I/O INTERFACES

4.1 Asynchronous Serial Ports (UART)

All OSM sizes supporting one low speed serial console (UART Console) and four general purpose serial interfaces (UART). Two of them supporting handshake signals as well. The asynchronous serial ports run at 1.8 V logic levels. The transmit and receive data lines from and to the Module are active high, and the handshake lines are active low, per industry convention.

Electrically UART Console and general purpose UART are the same. Most SOC using one dedicated serial interface as bidirectional console for OS commands. Preferred for this is UART Console. Typical implementation for this interface is a connecton to testpoints or pin header only for test and manufacturing purposes without accessibility to the user.

The following chapters showing two possible industry standard implementations for the general purpose serial interfaces.

4.1.1 RS232 Ports

If the asynchronous ports are to interface with RS232 level devices, then a RS-232 transceiver is required on the Carrier board. The logic side of the transceiver must be able to run at 1.8 V levels. The selection of 1.8 V compatible transceivers is a bit limited, although more are appearing with time. Two such devices are the Texas Instruments TRS3253E, and the Maxim MAX13235E, illustrated in the figures below. The TI part is more cost effective, but has a top speed of 1 Mbps. The MAX13235E can operate at maximum speeds over 3 Mbps (but your OSM Module may or may not - check with your Module vendor). The transceivers invert the polarity of the incoming and outgoing data and handshake lines.

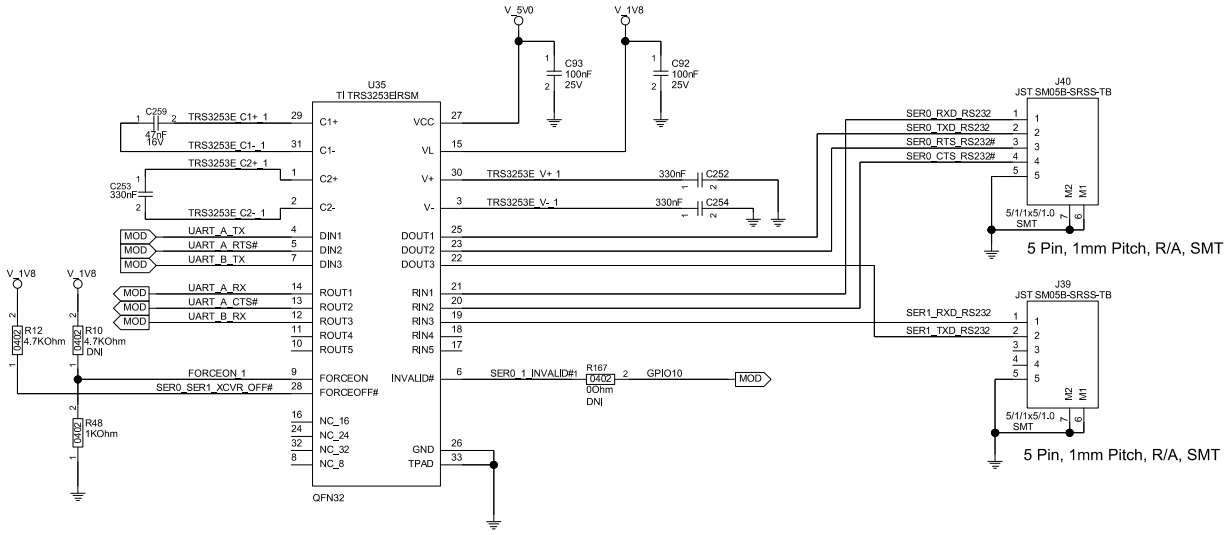


Figure 11 Asynchronous Serial Port Transceiver – RS232 – TRS3253E

Pin 6 of U35 (INVALID#) may be connected to a GPIO of the OSM Module (GPIO10 in this example) but it has to be checked if this GPIO is not needed for another function.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

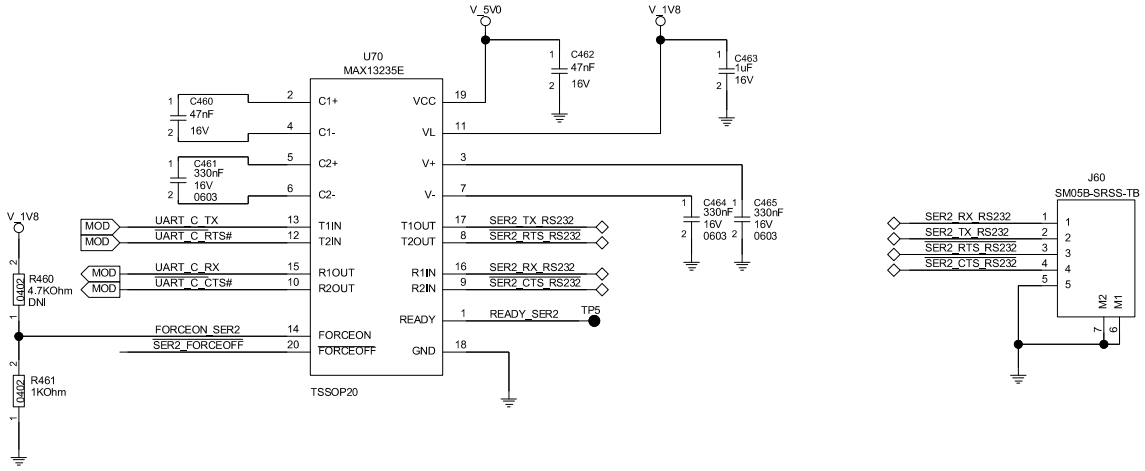


Figure 12 Asynchronous Serial Port Transceiver – RS232 – MAX13235E

4.1.2 RS485 Half Duplex

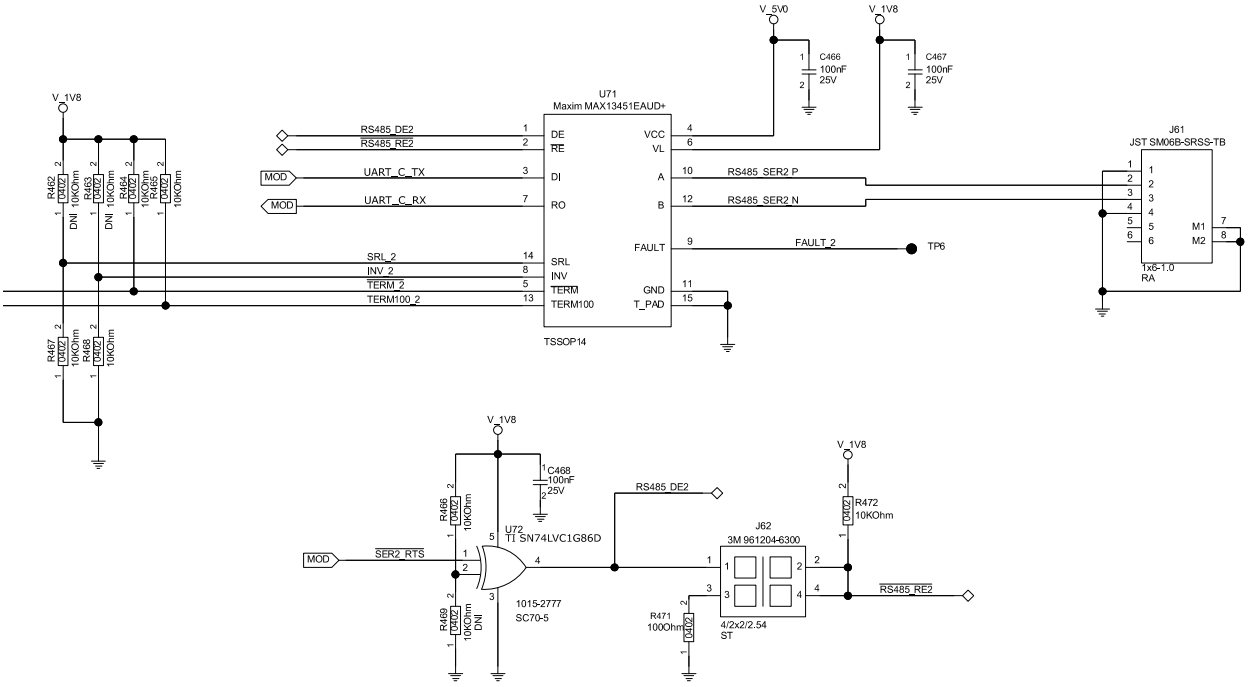
A half-duplex RS485 asynchronous serial port implementation is shown below. This hardware implementation is suitable for multi-drop RS485 networks. The Maxim MAX13451E transceiver accepts 1.8 V logic I/O and has other, flexible features of interest such as internal termination options. Other devices like TI THVD1450DGKR/THVD2450DGKR can be used when interfacing 3.3 V I/O voltage.

Multi-drop RS485 nodes should be strung together in daisy chain fashion using shielded twisted pair cable with a defined differential impedance (usually 120 Ω; sometimes 100 Ω cables are used). The two end-points of the system should be resistively terminated across the pair. The termination value should equal the differential impedance of the twisted pair cable used. The Maxim transceiver allows the termination to be enabled or disabled on the TERM# pin, and can be selected to be 100 Ω or 120 Ω via the TERM100 pin state. These pins can be controlled by Carrier Board GPIOs if desired.

The RS485 driver is enabled when the OSM UART_x_RTS# signal is asserted low (if the resistor options in front of the XOR gate are loaded as shown, such that the XOR gate inverts the UART_x_RTS# signal for the RS485_DE2 function).

A suitable, likely application specific, software driver is required to make the multi-drop RS485 network work.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000



Jumper 01-02	Jumper 03-04	State
Open	Open	RS485 receiver disabled
Open	Closed	RS485 receiver always enabled
Closed	Open	RS485 receiver enbled when transmitter disabled
Closed	Closed	Invalid

Figure 13 Asynchronous Serial Port Transceiver – RS485 – Half-Duplex

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.2 I2C Interfaces

The I2C bus is a versatile low bandwidth multi-drop bus originally defined by Philips (now NXP). It is a two-wire bus (clock and data) that relies on the use of open-drain drivers and passive pull-ups. The bus can be single master or multi-master. OSM Modules supporting two I2C interfaces in all sizes and are always I2C masters. Whether or not they allow other masters is Module implementation dependent. Most OSM systems use the I2C bus as a way for the OSM I2C Masters to interface to a variety of I2C Slave peripherals. The standard I2C interface operation speeds are 100 kHz and 400 kHz. Some implementations allow faster speeds.

All I2C ports run at 1.8 V logic levels and have internal on-module pull-ups.

Note: Be aware to prove all I2C addresses on one bus before selecting a I2C device to be used on Carrier Board. Module vendor may use devices like power management controller on I2C. Bus conflicts can result in mal function of the module.

4.2.1 I2C Level Translation, Isolation and Buffering

FETs may be used to perform I2C level translation, as shown in Figure 14. This arrangement provides no buffering. It can provide isolation to prevent one side of the bus dragging down the other if one of the rails is collapsed. The rail that is to collapse should be the rail driving the FET gates.

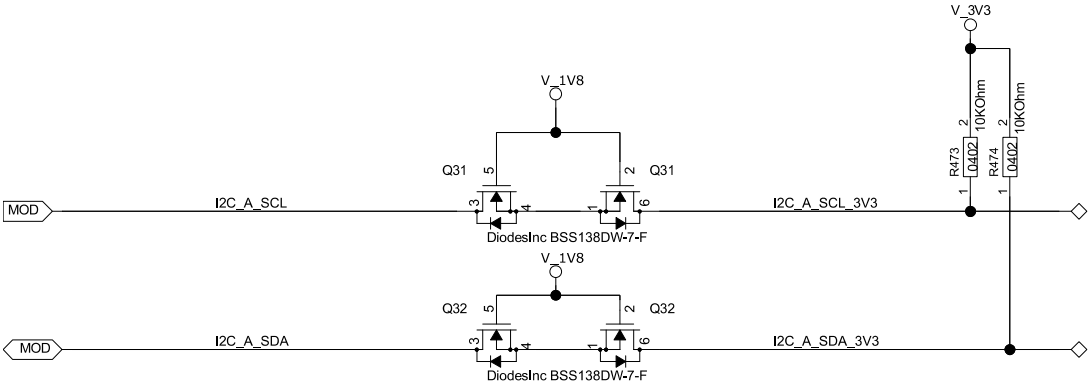


Figure 14 I2C Power Domain Isolation using FETs

The circuit shown in Figure 15 can provide power domain isolation, voltage level shifting and I2C bus buffering. The TI TXS0102 power rails VCCA and VCCB can be at the same voltage level or at different levels, over a range of 1.65 V up to 3.6 V / 5.5 V. Either rail can come up before the other.

If you have many I2C devices, it is a good idea to split them up into segments with up to about 6 devices on each segment and isolate the segments with a bi-directional I2C buffer such as the TXS0102. I2C bus performance degrades with too much capacitive loading.

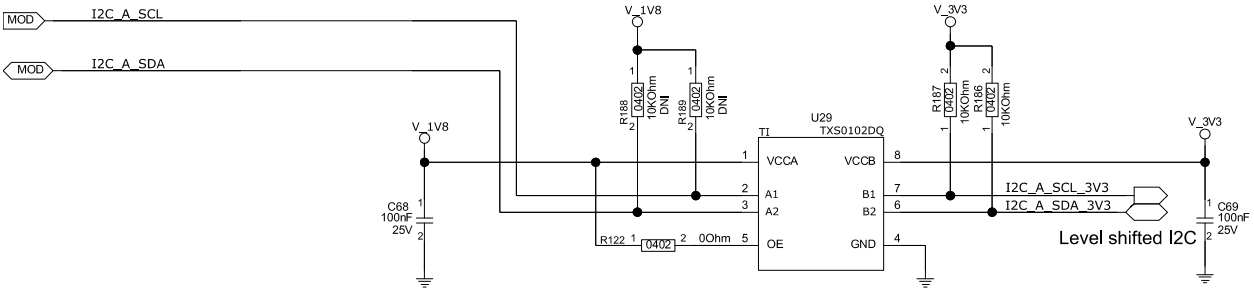


Figure 15 I2C Power Domain Isolation and Buffer

4.2.2 General I2C Bus EEPROMs

Both I2C buses (I2C_A, I2C_B) operate at 1.8 V. A simple EEPROM circuit is shown in Figure 16 for reference.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

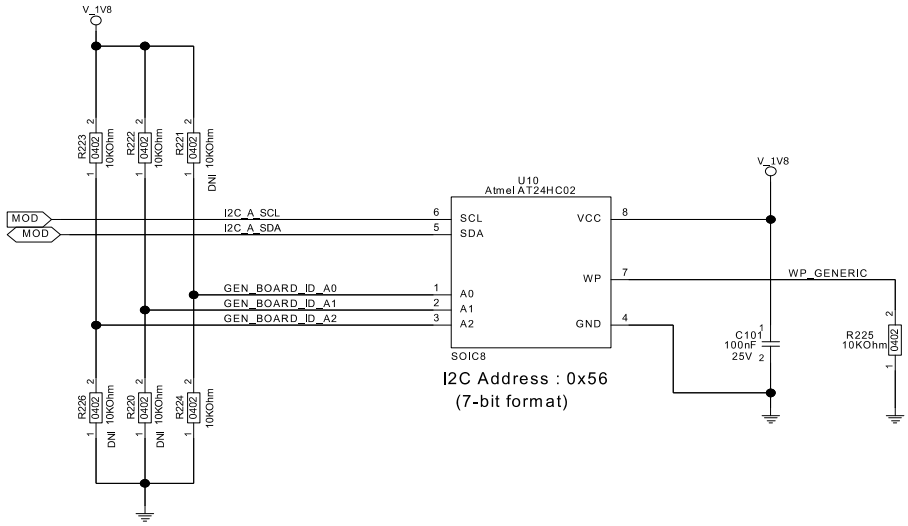


Figure 16 I2C EEPROM for general purpose

4.2.3 I2C Based I/O Expanders

I2C based “I/O Expanders” are available from Texas Instruments, NXP and others. Multiple expanders may be put onto the same I2C bus by configuring the I/O expander I2C address straps. These devices are an easy and cost effective way to realize additional I/O on OSM systems.

On the device shown in Figure 17, the I/O ports on the right are all in a high impedance “tri-state” mode when the device powers up. This allows the designer to tie the I/O lines through resistor pull-ups or pull-downs to define a power up state for these lines, before the I2C interface and before software are active. Wider (x16) devices are also available.

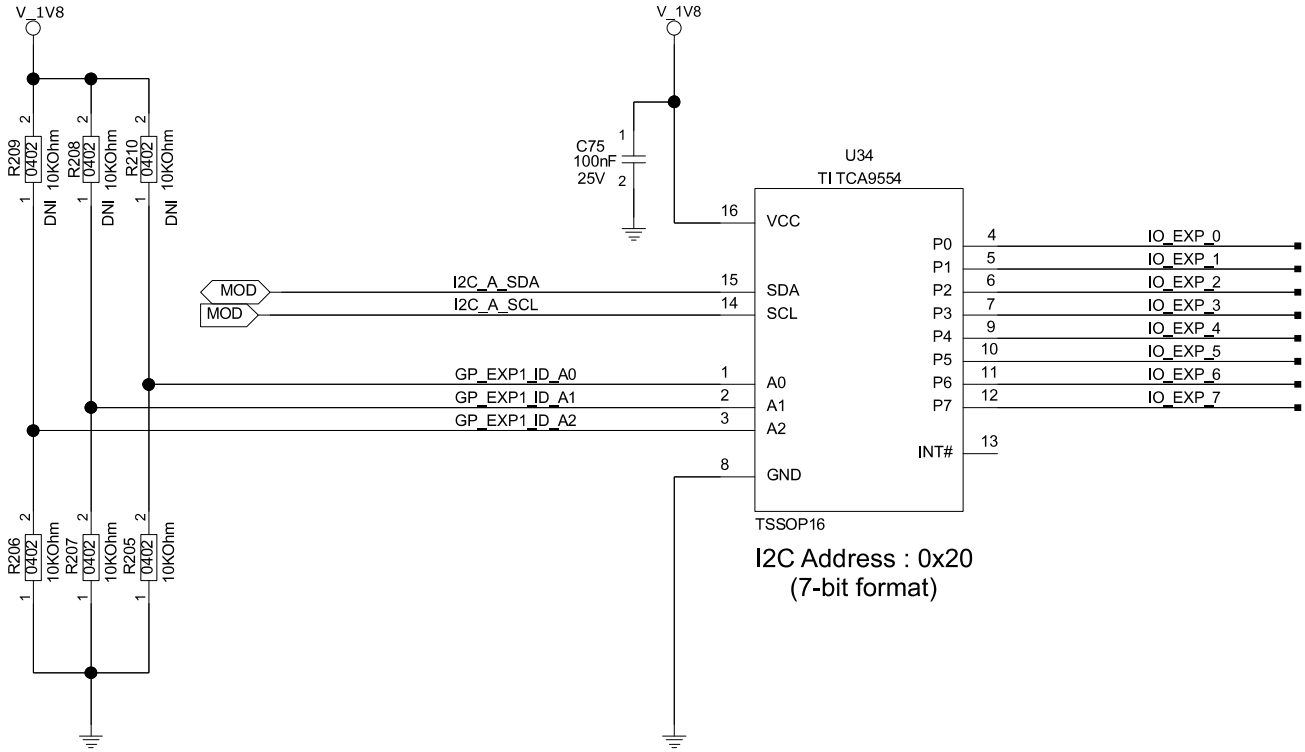


Figure 17 I2C Device: I/O Expander

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.2.4 Other I2C Devices

There is a very wide variety of I2C peripherals available on the market. Since OSM Modules offer up to two I2C buses (not counting the CSI / LVDS private I2C bus), it is easy to incorporate I2C devices into a OSM system. A few schematic examples are given here, and further suggestions are listed in the table at the end of this section.

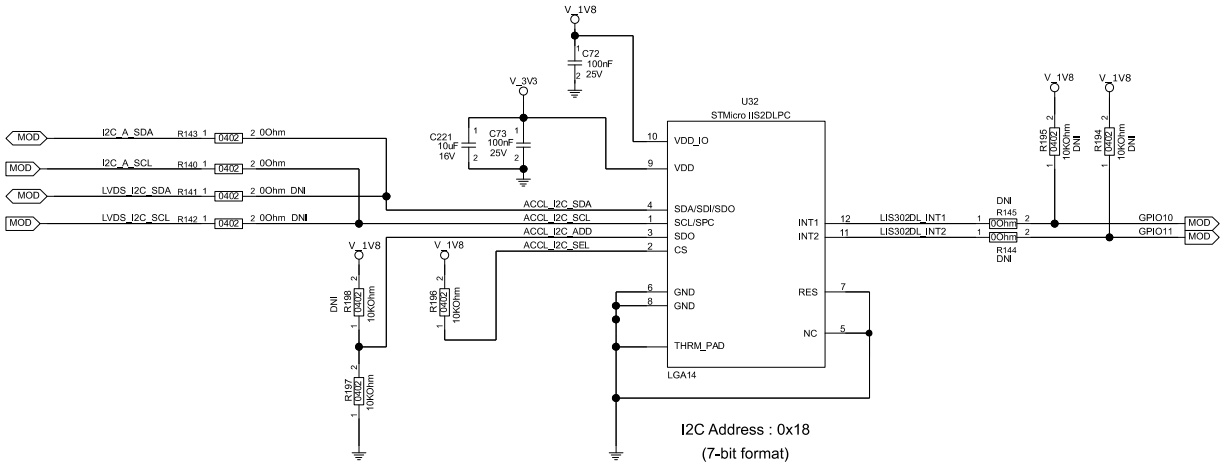


Figure 18 I2C Device: Accelerometer

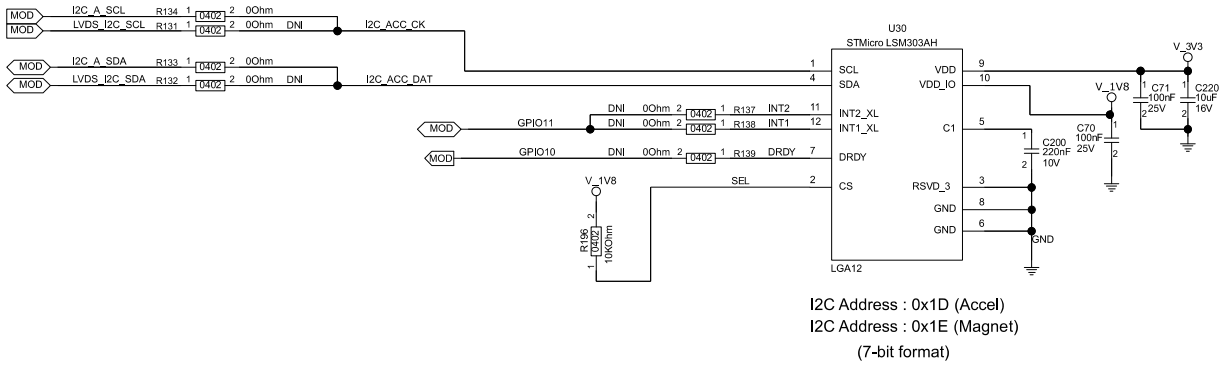


Figure 19 I2C Device: Accelerometer und Magnetometer

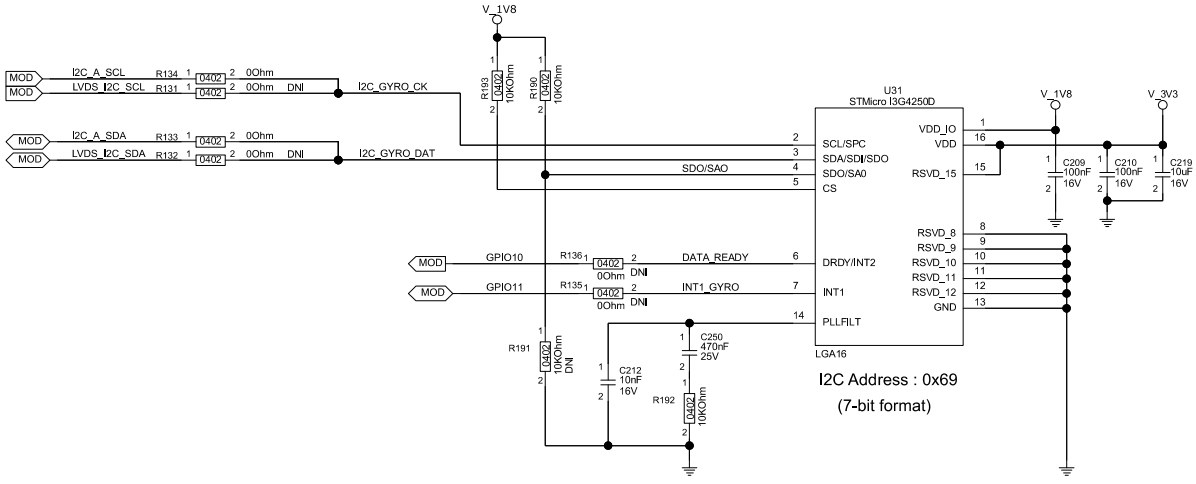


Figure 20 I2C Device: Gyroscope

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

The table below gives a small sampling of other 1.8 V I/O I2C devices that are available. The list is meant to just give the reader an idea of what types of devices are available. There are further devices that can be used if 3.3 V and level shifting are considered.

Table 3 I2C Device Examples

Function	Device Description	Vendor	Vendor P/N
ADC	8-channel, 12-bit SAR ADC with temperature sensor	Analog Devices	AD7291
DAC	Quad, 16-bit DAC	Analog Devices	AD5696R
LED driver	7-bit LED driver with intensity control	Texas Instruments	TCA6507
Proximity / Button sensor	Four Channels, Capacitive Proximity/Button Solution	Semtech	SX9500
Temperature Sensor	Temperature Monitor, ±1° C	On Semiconductor	NCT72
UART	128 Word FIFOs	Maxim Integrated	MAX3108

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.3 Touch Screen Controller Interfaces

This part will be released in future revision of this documentation.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.4 I2S Interfaces

The I2S (Inter IC Sound) bus specification was initially released in 1986 by Philips (NXP) and later revised in 1996. I2S is a synchronous serial bus used for interfacing digital audio devices such as Audio CODECs and DSP chips. Generally, PCM audio data is transmitted over the I2S interface. The I2S bus may have a single bidirectional data line or two separate data lines. The signals constituting the I2S bus are a serial clock/ bit clock (output from the master), a left right clock (output from the master) that indicates the channel being transmitted and a single bidirectional data line or two data lines - one input and one output. A OSM Module can generally be configured as I2S master or slave. OSM Modules may support up to two independent I2S interfaces each having separate input and output data lines.

4.4.1 Cirrus Logic I2S Audio Example

An example of an I2S based audio circuit using the Cirrus Logic WM8904 CODEC is given in Figure 21.

The circuit uses a OSM I2S A interface for the audio PCM data, and a OSM I2C B interface to allow a path for software setup of registers within the CODEC.

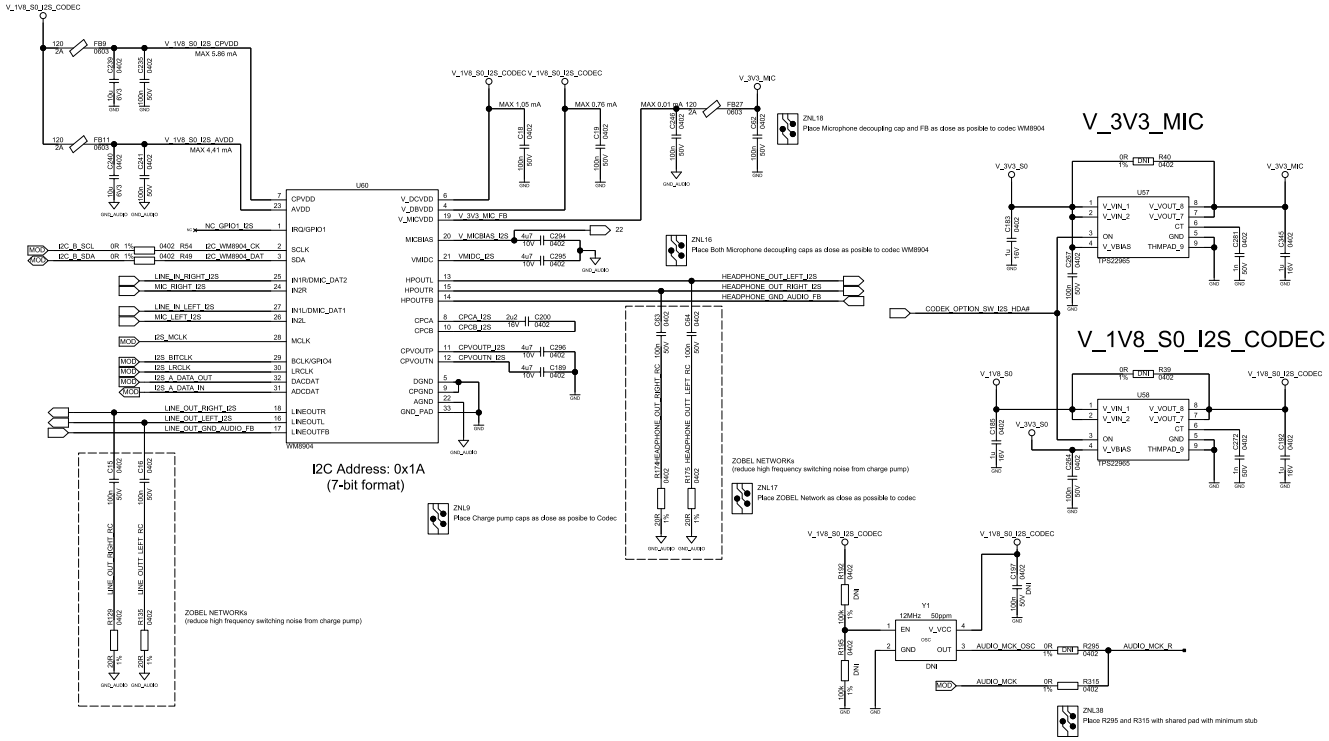


Figure 21 I2S Audio Codec Cirrus Logic WM8904

4.4.2 Texas Instruments TLV320AIC3105 I2S Audio Example

An alternative I2S audio CODEC with external amplifier from TI is shown in Figure 22 and Figure 23 below. As in the WM8904 example, the I2S carries the PCM audio from and to the OSM Module, and the I2C is used for chip setup parameters.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

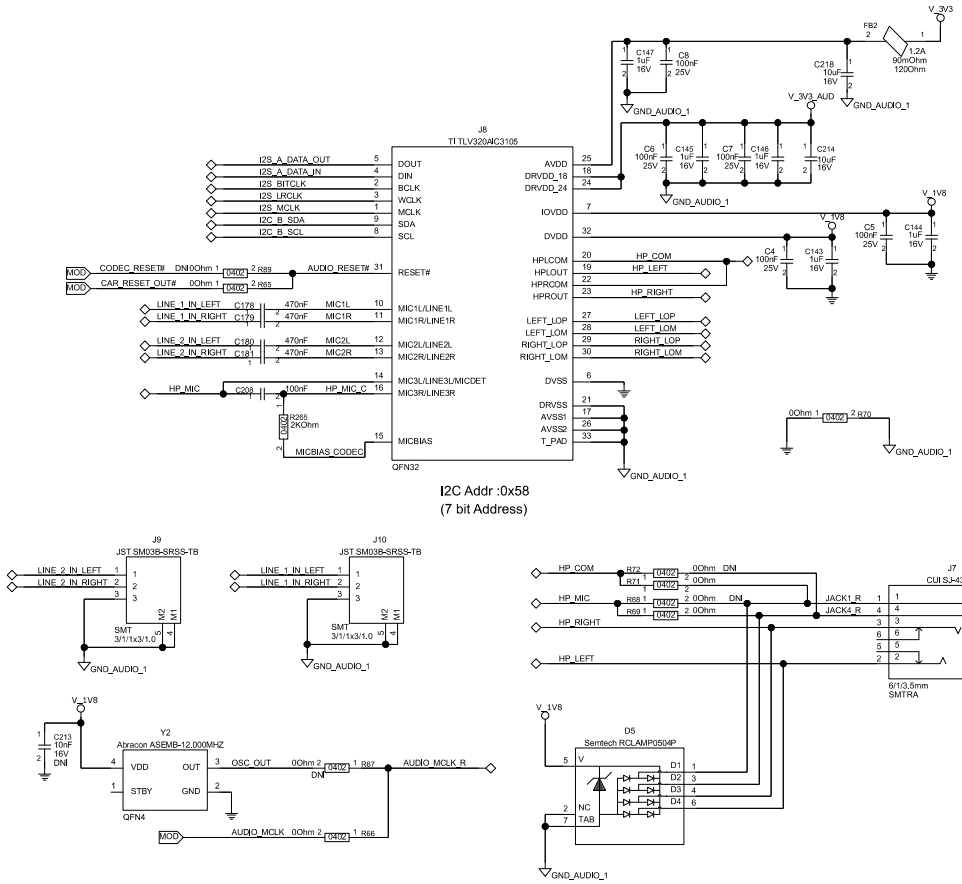


Figure 22 I2S Audio CODEC TI TLV320AI

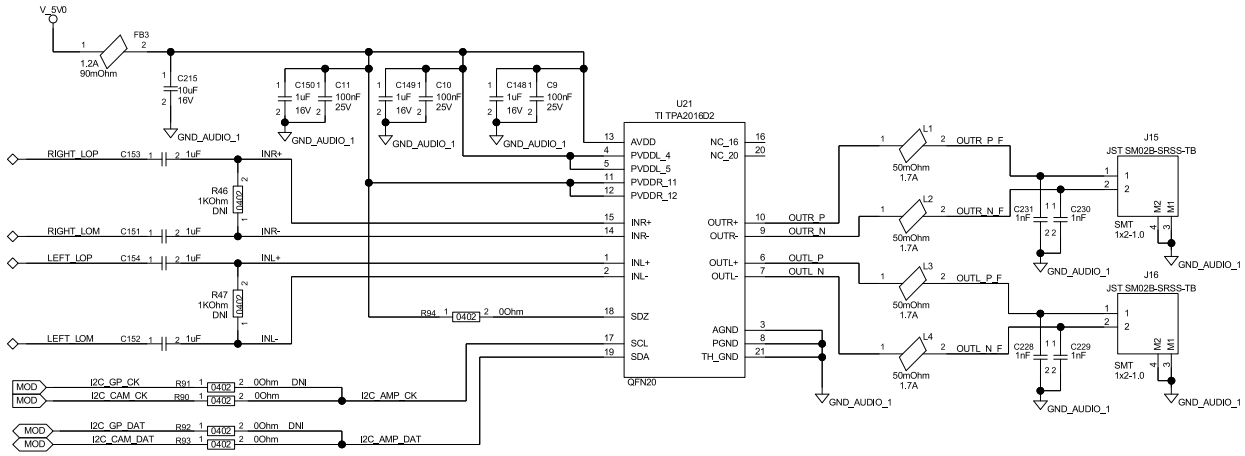


Figure 23 Audio Amplifier TI TPA2016D2

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.5 SPI Interfaces

The SPI (Serial Peripheral Interface) is a full duplex synchronous bus supporting a single master and multiple slave devices. The SPI bus consists of a serial clock line (generated by the master); data output line from the master; a data input line to the master and one or more active low chip select signals (output from the master).

Clock frequencies from 1-100 MHz may be generated by the master depending on the maximum frequency supported by the components in the system. OSM Modules running a 1.8 V I/O interface on all three SPI interfaces.

The OSM Module will always be the SPI master. OSM Modules may support a Carrier SPI Boot option.

4.5.1 OSM Implementation

Each SPI device requires a chip select, a clock, a data in line and a data out line. The device I/O level must of course be compatible with the OSM Module I/O level of 1.8 V.

The Winbond W25Q64JV is an example of a 1.8 V I/O compatible SPI Flash device. The Figure 24 below illustrates a socket implementation for a SPI Flash memory.

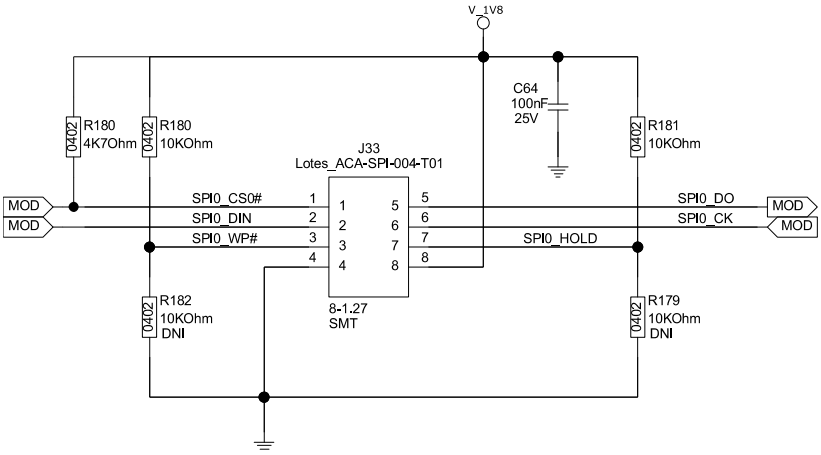


Figure 24 SPI Flash Socket

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.5.2 SPI Device Examples – 1.8 V I/O

The Table 4 below shows a small sample of the devices available on the market with a 1.8 V SPI interface. It is only a sample and is meant to give an idea of the type of devices available. Remember to check the software driver situation before settling on a particular device.

Table 4 SPI Device Examples

Functionality	Device Description	Vendor	Vendor P/N
ADC	8-channel, 12-bit SAR ADC with temperature sensor	Analog Devices	AD7298
DAC	Quad, 16-bit nano DAC	Analog Devices	AD5686R
Flash Memory	64 Mbit SPI Flash memory	Winbond	W25Q64JV
IO Expander	8-bit GPIO expander with integrated level shifters	MaxLinear (formerly Exar)	XRA1404
Temperature Sensor	Digital thermometer ▪ ±2 °C resolution ▪ Range -55 °C to +120 °C	Maxim Integrated	DS1722
Touch Screen Controller	4 wire resistive touch screen controller	Texas Instruments	TSC2008 TSC2008-Q1
UART bridge	UART with 128 Word FIFOs and support for 9-bit multi-drop mode data filtering	Maxim Integrated	MAX3108

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

4.6 CAN Bus

The CAN (“Controller Area Network”) bus is a differential half duplex data bus used in automotive and industrial settings. A CAN bus uses shielded or unshielded twisted differential pair wiring, terminated in with a differential impedance of 120 Ω at the endpoints of the bus. Nodes on the bus are arranged in daisy-chain fashion, although stubs of up to 0.3 meters are allowed at each node. The standard allows data rates of up to 1 Mbps, with a maximum bus length of 40 meters at that rate. Various slower rates are defined, along with longer and longer bus lengths allowed as the data rates go down. A bus rate of 250 kbps is common use in automotive application. With CAN FD also faster baud rates are possible.

The two lines in a CAN twisted pair are referred to as CAN_H and CAN_L (for CAN High and CAN Low). There are two bus states on the CAN physical layer: the Dominant state and the Recessive state. In the Dominant state, CAN_L is pulled to GND through an open drain driver and CAN_H is pulled to the CAN Vcc through an open drain driver. In the Recessive state, CAN_L and CAN_H are not actively driven and they are pulled to a voltage of (Vcc / 2) by passive components. Hence the CAN bus is essentially a differential open-drain bus. On the system logic side of a CAN transceiver, the CAN Dominant state is a logic low and the Recessive state a logic high.

The CAN protocol has features important to a real time environment:

- Nodes are prioritized: CAN nodes are assigned an 11 bit identifier
  - The lower the ID number, the higher priority
- Latency time is guaranteed
- Data packets are limited to 8 bytes maximum
  - Higher level protocols take care of handling large data sets
- The bus has Multi-master capability
- There are error detection and signaling features

The CAN bus base standard is defined by ISO 11898-1:2003, available for a fee from the ISO (www.iso.org). There are some very helpful CAN application notes from Texas Instruments (a vendor of CAN MAC and transceiver devices) available for free. These include “***Introduction to the Controller Area Network (CAN)***”, TI document number SLOA101A, and “***Controller Area Network Physical Layer Requirements***”, document number SLLA270. The original CAN bus protocol definition by Bosch is also freely available on the web (***CAN Specification***, Version 2.0 © 1991 Robert Bosch GmbH).

Various connectors are used in CAN bus implementations. The use of DB-9 connectors is fairly common. The TI application note (SLLA270) referenced above has pin-out information for a couple of common CAN connector implementations.

4.6.1 OSM Implementation

The OSM specification allows for up to two logic level CAN ports. The ports run at the Module I/O voltage (typically 1.8 V) and consist of an asynchronous CAN TX line and an RX line from and to the OSM Module CAN protocol controller.

A Carrier based CAN transceiver is required to provide a CAN bus from the Module signals. CAN PHYs are available from Texas Instruments, On Semiconductor, NXP, Microchip and numerous other vendors. The logic interface for CAN PHYs is typically suited for 3.3 V logic I/O, so level translation is required.

Precautions must be taken to prevent a CAN system from sending out frames or blocking a CAN-Bus unintentionally, for example during reset and power down. During power down, CAN Transceivers are designed to be HIGH-Z. During power up or reset, they must be put into a “listen only mode”. It is the responsibility of the application software to activate the CAN-transceiver after all initialization is done. If no GPIO connection is possible or wanted this signal also could be connected to the system reset. Please check your design carefully if this ensures that no unwanted frames are sent in your design.

A OSM Carrier board CAN transceiver implementation is shown below. This example shows two 60 Ω terminations (or 120 Ω across the CAN pair). This is appropriate only if the node is an end-point, and intermediate nodes should not be terminated.

The example transceiver TJA1051 has a “silent input pin”. If left open, the transceiver enters “listen only mode”. Using a GPIO allows the application software to set the can transceiver into “normal mode = able

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

to send" by pulling "silent" low. A pull-down resistor on the gate of T1 is necessary to disable the transceiver in case of a CPU reset or power fail.

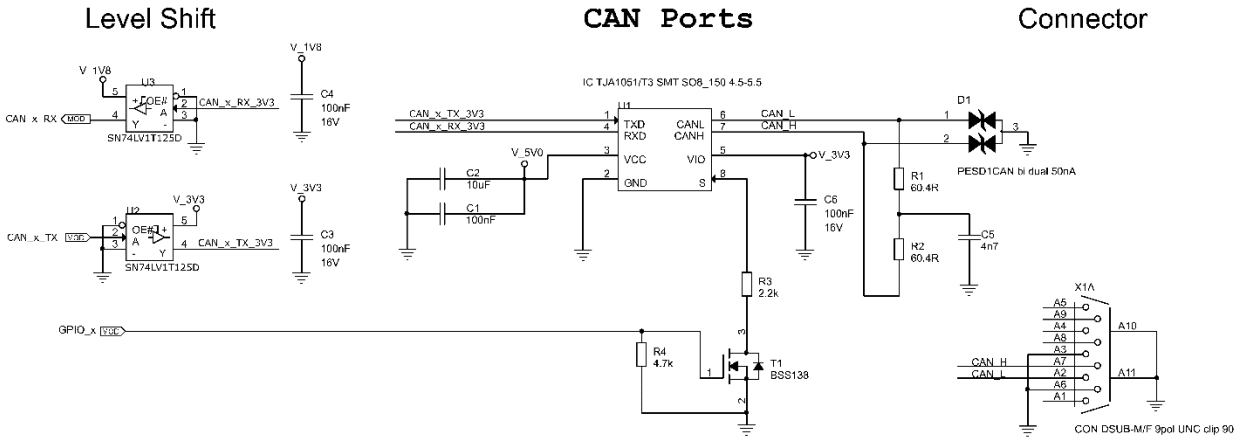


Figure 25 CAN Bus Implementation

4.6.2 Isolation

Some CAN transceiver application notes show optical isolation between the CAN protocol controller and the CAN transceiver. See, for example, NXP application note AN96116 for the PCA82C250 CAN transceiver. They suggest using the 6N137 optical transceivers. Be careful to take into account the I/O levels and current sink / source requirements of the various devices in the chain.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5 HIGH SPEED SERIAL I/O INTERFACES

5.1 USB

The USB (Universal Serial Bus) is a hot-pluggable general purpose high speed I/O standard for computer peripherals. The standard defines connector types, cabling, and communication protocols for interconnecting a wide variety of electronic devices. The USB 2.0 Specification defines data transfer rates as high as 480 Mbps (also known as High Speed USB). A USB host bus connector uses four pins: a power supply pin (5V), a differential pair (D+ and D- pins) and a ground pin. Additionally a fifth pin, USB ID (mostly used in devices supporting USB-OTG), may also be used which indicates whether the device operates in Host mode or a Client/Device mode.

OSM Modules support up to two independent USB 2.0 buses, designated USB A and USB B. Further two USB 3.0 buses including USB 2.0 signals are available on USB C and USB D.

OSM USB A can be configured as a host, client or OTG port. OTG and client operation are optional. Common scenario for USB A is using it as an interface for serial downloader for the SOC. USB Boot or client function in case of special boot configuration are specific to the SOC used on the module.

OSM USB B is defined as always host.

OSM USB C and USB D may supporting USB 3.0 or only USB 2.0. USB3.0 Super Speed defines data rates up to 5 Gbps (also referred to as USB 3.2 gen1). Therefore these ports have two additional differential signal pairs SSRX and SSTX. In case of USB 3.0 implementation USB Dual Role is supported and in case of USB 2.0 than USB OTG is supported.

See OSM Hardware Specification for full Support Matrix of USB depending on the module size.

All USB interfaces have dedicated contacts for over current detection (OC#), VBUS power enable (EN) and VBUS power detection (VBUS) which are able to be using 1.8 V or 3.3 V I/O voltage.

Note: Interface OSM USB C references to the name of interface specified by OSM Hardware Specification and not USB Type-C defined by USB Org.

5.1.1 USB A Client / Host direct from Module (USB 2.0)

The Figure 26 shows a USB-OTG implementation on the USB A port terminated on a USB micro Type A/B connector

The ESD diodes should be placed close to the connector, and the USB traces routed as differential pairs in “no stub” fashion – the traces should go through the pads of the ESD protection devices, without introducing a stub. If the client device is bus powered, the Carrier can supply 5 V, 500mA power to the client device. The Module USB_A_EN signal controls the power switch Diodes Incorporated AP22615, which in turn supplies power to a bus-powered client device. USB_A_OC# is an open drain output of the Carrier Board to the module and signals an overcurrent event. Per the USB specification, bus powered USB 2.0 devices are limited to a maximum of 500 mA. The AP22615 limits the current and can stand an indefinite short circuit to GND. The current limiting is somewhat imprecise, and kicks in between 500 mA and 1 A.

Note: Most USB power switches do not disconnect the VBUS from internal supply in an overcurrent situation but limiting the current to the specified limit value until thermal shutdown. Ensure that Carrier Board supply concept is capable to deliver the limit value.

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

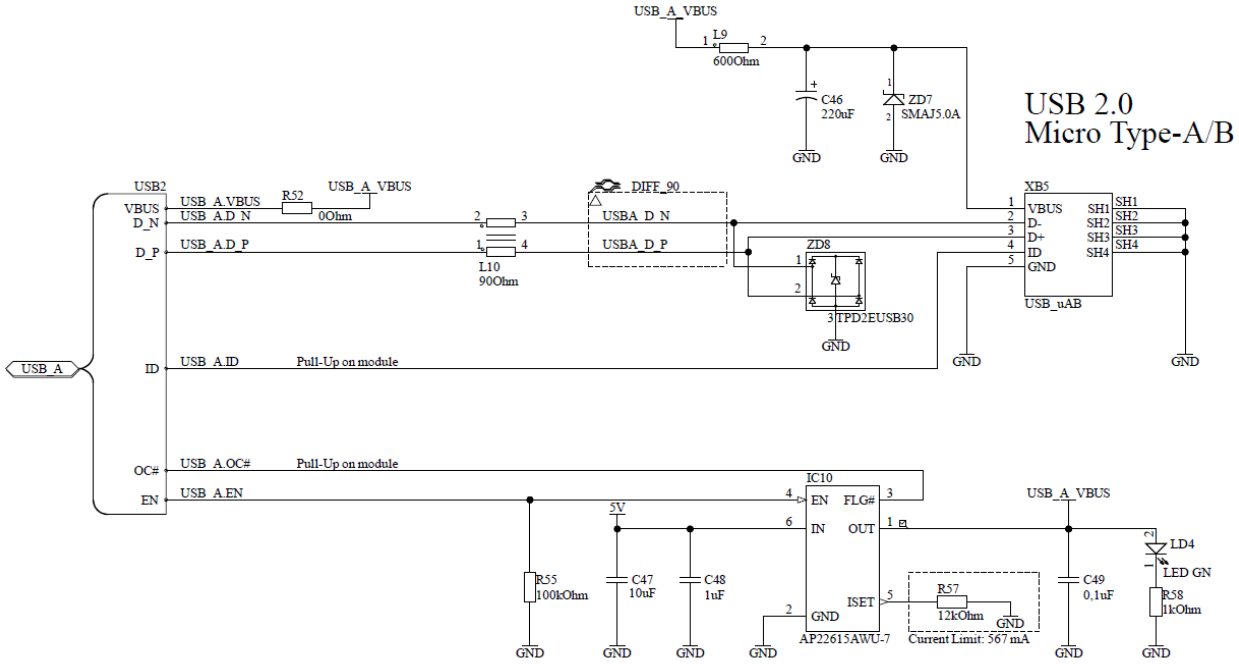


Figure 26 USB A Client / Host direct from module

Note: If the Module doesn´t support USB ID Pin for OTG / Host-Client function the USB VBUS supply control can be manipulated directly (please refer to Figure 27). A Micro USB type A plug at the Carrier receptacle pulls the ID pin signal to ground so that the Module acts as a Host. With ID signal low the Carrier may drive USB VBUS.

If in doubt, ask your Module vendor for details of OTG and bus power control support.

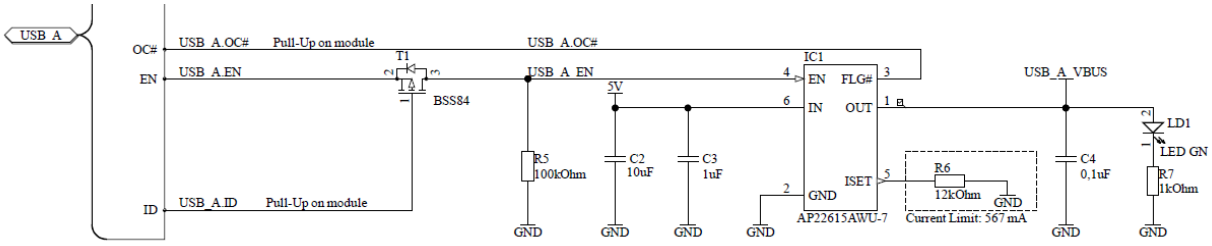


Figure 27 USB OTG – Discrete VBUS Enable through ID-Pin

USB_A_ID is pulled low (< 10 Ω to GND) for Host mode within the USB cable if a Micro USB type A plug is used. In case of Device mode is required a USB cable with a Micro USB type B plug is needed. In that case the USB_A_ID signal is floating (> 100 kΩ to GND). This results in a “high” signal for the ID pin.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.1.2 USB B Host direct from Module (USB 2.0)

Carrier board implementation of USB host port from OSM USB B is straightforward. An implementation of a single USB Type A host port header is shown in the figure below.

The ESD diodes should be placed close to the connector, and the USB traces routed as differential pairs in “no stub” fashion – the traces should go through the pads of the ESD protection devices, without introducing a stub.

If the target USB devices are “down” on the Carrier, then much or all of this circuit may be omitted. The OSM USB pairs are routed directly to the target device. The ferrite choke in the USB lines, the ESD diodes, and the AP22615 power switch and associated passives may be eliminated. However, in some cases, it is desirable to have the capability to “power cycle” a USB peripheral under software control. If this is the case, it might be desirable to retain the AP22615 power switch, or a similar device for 3.3 V power switching, with the power control function performed by the USB_A_EN.

USB_B_ID ist not used in this application.

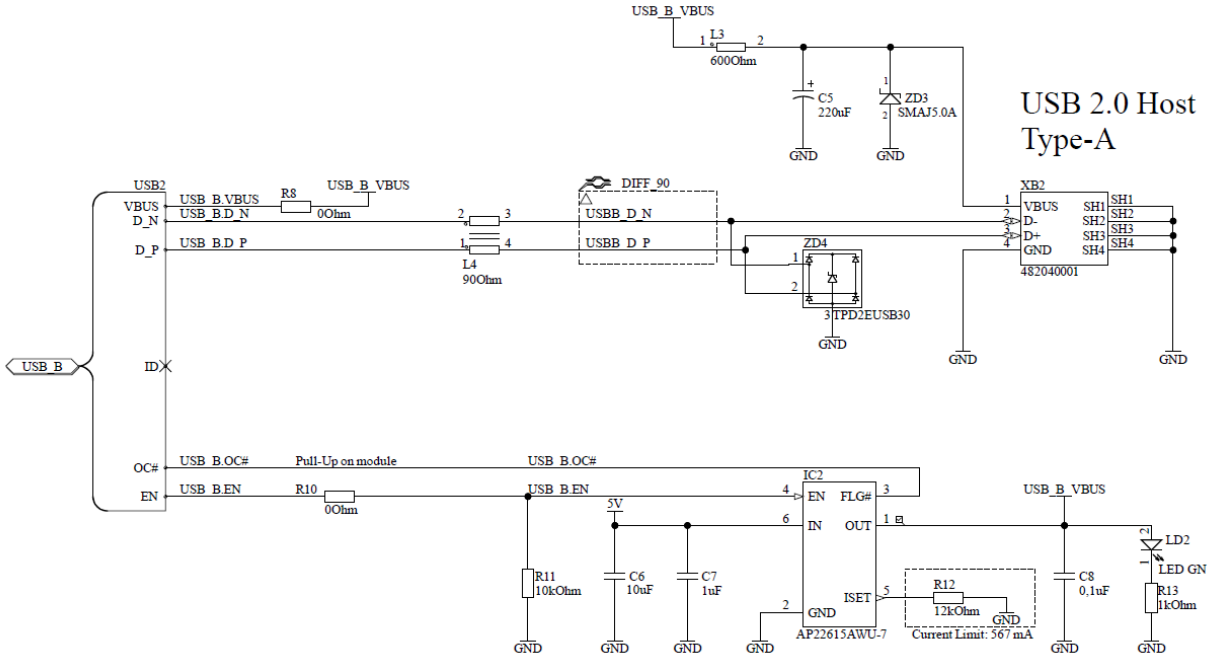


Figure 28 USB B Host direct from Module

5.1.3 USB C and USB D Host direct from Module (USB 3.0)

The USB C and USB D ports can be USB 3.0 ports and each consists of a USB 2.0 port and a set of unidirectional SuperSpeed differential pair signals (SSTX / SSRX). The following example shows an implementation of a single USB 3.0 connector that is utilizing USB2 or / and USB3 without using the optional OTG or dual role function.

Place the ESD diodes as close as possible to the connector. For SuperSpeed Signals, ESD diodes with optimized package and low I/O capacitance should be used to create only minimal impact on signal integrity. Also the common mode chokes should be selected carefully. Ensure that their differential mode cutoff frequency is well above the maximum frequency of 2.5 GHz of a USB3.0 signal.

Each USB 3.0 port should be able to supply up to 900mA and should be decoupled with at least 120µF of low ESR capacitance. Not including any USB PD capabilities.

USB_x_ID ist not used in this application.

Note: Most USB power switches do not disconnect the VBUS from internal supply in an overcurrent situation but limiting the current to the specified limit value until thermal shutdown. Ensure that Carrier Board supply concept is capable to deliver the limit value.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

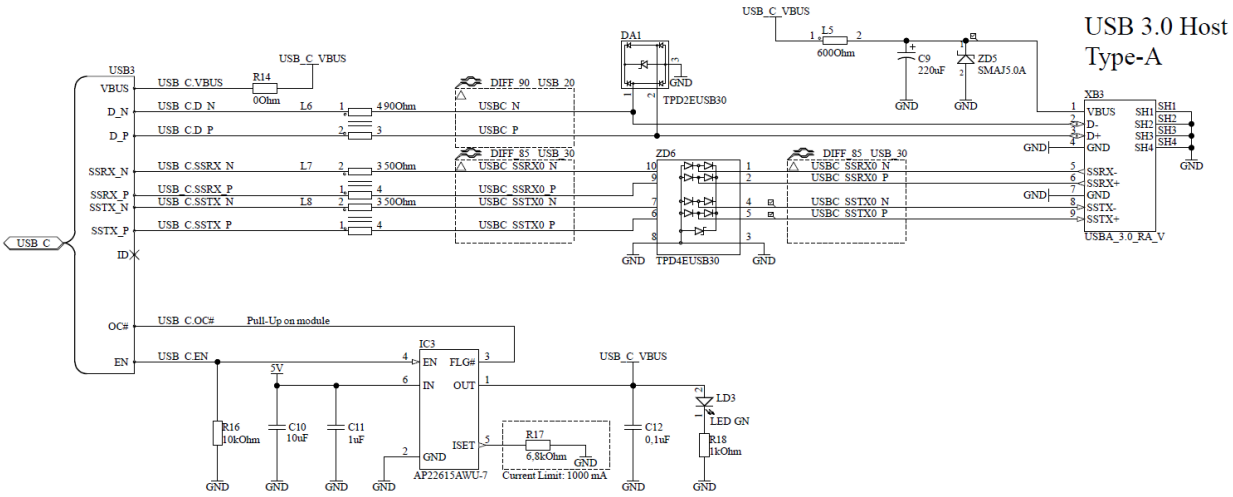


Figure 29 USB C / USB D as USB 3.0 Host Port

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.1.4 USB Hub

Additional USB ports may be implemented on a OSM Carrier board using a USB hub to interface with one of the OSM USB ports (usually USB B or USB C, saving the OSM USB A for possible client or OTG use). The USB 2.0/3.0 compliant family of hubs from Microchip (USBxxxx) or Texas Instruments (TUSBxxxx) is recommended. Parts with two, three, four or seven downstream ports are available.

If available use UCB C including USB 3.0 signals to connect to a hub.

A Carrier Board hub implementation example using the four port Microchip USB5744 is shown in Figure 30 below. In this case the downstream ports 1 and 2 are used for USB 3.0 and downstream ports 3 und 4 are used for internal Carrier Board periphery without any power enable or overcurrent detection.

The boot strapping of any hub must be considered carefully. It is wise to keep all boot strapping options open and have all strap options accessible for re-configuration by option resistors or other means. It may keep you out of trouble and save an additional board spin.

Since the hub operates at 3.3 V, the signals from the OSM Modules that are at 1.8 V levels (RESET_N and the I2C signals, if used) need to be level shifted to 3.3 V to interface to the hub. Check datasheet of the USB hub that may allow 1.8 V I/O voltage for data signals.

The implementation of the downstream ports can be adapted from previous chapter 5.1.1 to 5.1.3 and is not showed in this chapter.

The behavior of a USB port, at least initially, may differ slightly depending on whether that port is direct from the OSM Module or whether the port is through a hub. With software adjustments, or “tweaking”, the direct and through hub ports may appear virtually identical to a client device.

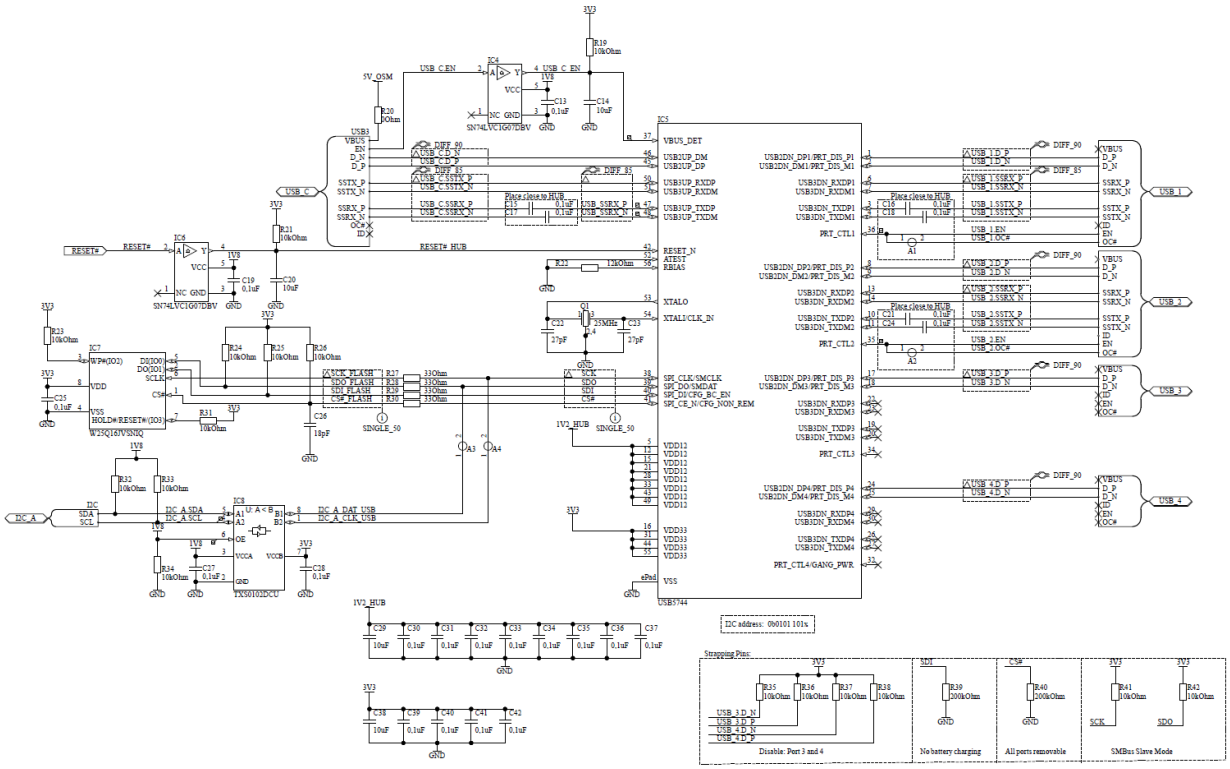


Figure 30 USB 3.0 Hub

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.1.5 USB Type-C – Parade PS8750B

USB Type-C together with USB PD is a great achievement from the USB consortium to simplify the interfacing between devices and the usage of technology for users. The more complex it is for possible implementations.

To demonstrate that all these features are also available by designing Carriers with OSM modules a Type-C connector implementation with USB 3.0 (or 3.2 gen1) with DP alternate function is shown in Figure 31. It doesn´t include a specific power controller to support enhanced PD functionality but can support up to 3 A at 5 V to the connector.

Level shifters are implemented to interface the 3.3 V signals from the PS8750 to the OSM Module requiring 1.8 V signals.

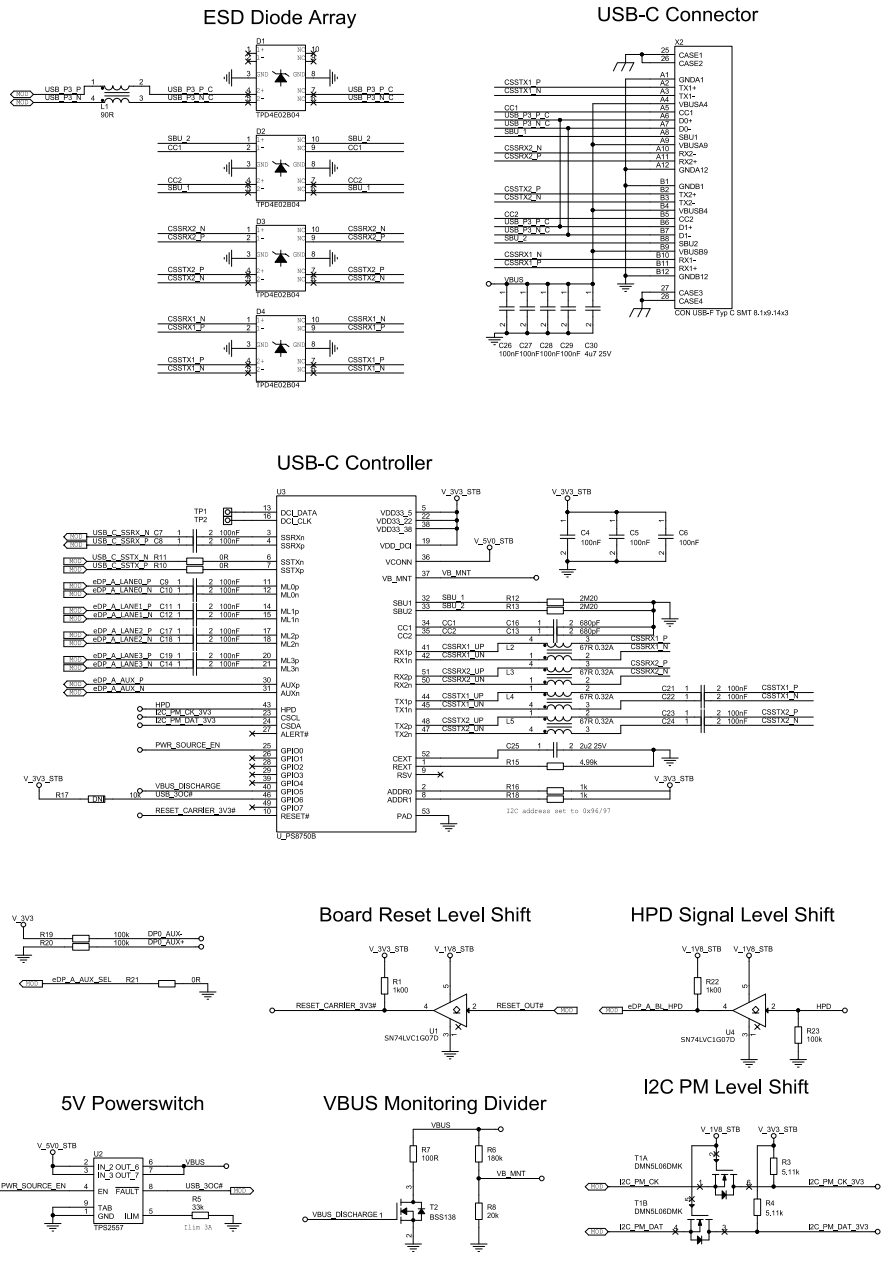


Figure 31 USB Type-C – Parade PS8750B

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.1.6 USB Control Signals

All USB interfaces USB A up to USB D supporting dedicated contacts for overcurrent detection (USB_[A:D]_OC#), device detection (USB_[A:D]_ID) and VBUS power enable (USB_[A:D]_EN). All contacts are referenced to 1.8 V.

Carrier designer should not use external pull ups on USB_[A:D]_ID or USB_[A:D]_OC# as these are placed on-module.

Normally USB_[A:D]_EN is connected directly to the Enable-Input of a power switch that supplies the VBUS voltage.

There are a lot of power distribution switches that are able to be switched by 1.8 V level of the module.

Table 5 USB Power Distribution Switch Examples

Device Description	Vendor	Vendor P/N	Enable-Voltage (min.)
Single Channel Switch with Overcurrent-Output and configurable current threshold	Diodes Incorporated	AP22815 / AP22615	1.2 V
Dual Channel Switch with Fault-Output and configurable current threshold	Texas Instruments	TPS2560 / TPS2561	1.1 V
Single Channel Switch with Fault-Output and configurable current threshold	Texas Instruments	TPS2559	1.1 V

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.2 Ethernet

OSM supports up to five MAC interfaces to implement Ethernet ports on the Carrier Board. The interface is used to connect an on-module MAC to an off-module PHY placed on the Carrier Board. Supported interfaces are MII, RMII, RGMII, SGMII allowing speeds from 10 Mbit/s up to 1000 Mbit/s.

The OSM Hardware Specification allows using 1.8 V / 2.5 V / 3.3 V as the I/O voltage depends on the MAC interface, SOC and Ethernet PHY. Interface mode and I/O voltage can be used separate for each of five interfaces. See datasheet of Module vendor for specification.

Note: Ethernet PHY has to be selected depending on supported MAC interface mode and I/O voltage. See datasheet of Module vendor for specification.

5.2.1 MAC-Interfaces

As given in OSM Hardware Specification the contacts for ETH A up to ETH E are depending on the Ethernet MAC interface used by the OSM Module. In general there are following supported interface types:

- MII and RMII supports 10/100 Mbit/s only
- RGMII and SGMII supports 10/100/1000 Mbit/s
- SGMII using low amount of differential signals for reduced EMI restrictions

The contacts used for MAC to PHY connection differs for each of these types. An overview is given within the OSM specification.

SGMII consists of differential 1.25 Gbps LVDS lanes which using clock recovery within the MAC. Typical SGMII PHYs like Texas Instruments DP83867IS are capable of working as 4-wire (RX/TX) or 6-wire (RX/TX/CLK) interface. OSM only supports 4-wire mode which means on-module MAC must be capable of recovering clock from the data.

Note: Optional function of TX_ER in MII or RMII-Mode is not supported.

Note: Contact direction of MII and RGMII-Clock must be checked with specific PHY. Most devices allowing different clock modes like external oscillator or internal clock from MAC. Specific OSM Module may supporting different clock modes. Contact your OSM Module vendor for specific information.

5.2.2 SMI-Interface

There are three SMI-Interfaces for serial management interface to the PHY. As this bus allows addressing different devices one can use this SMI for all five Ethernet ports. The developer of the Carrier Board needs to assign unique PHY addresses for each Ethernet PHY.

In case of more complex SOCs, where more than one SMI-Interface must be used, for example because of SOCs internal power management or clock gating features by the OS, use ETH_B_MDIO/MDC or ETH_CDE_MDIO/MDC for additional SMI-Interface as shown in following table:

Table 6 SMI Interfaces

MDIO contacts	MDIO contact used
ETH_MDIO, ETH_MDC	ETH_A
ETH_B_MDIO, ETH_B_MDC	ETH_B
ETH_CDE_MDIO, ETH_CDE_MDC	ETH_C
	ETH_D
	ETH_E

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

OSM Module is the master on SMI-Bus. As I/O voltage is not fixed there is no on-module pull-up. Place pull-up on Carrier Board in range of 2.2 kΩ to 10 kΩ at MDIO contacts towards used I/O voltage.

5.2.3 OSM Implementation

5.2.3.1 RGMII

Figure 32 showing a schematic example for a typical Gigabit Ethernet Interface using Texas Instruments DP83867IS. This PHY can be configured for RGMII and SGMII by boot strapping.

RGMII using 125 MHz clock for each TX and RX single ended data lanes. Data is sampled on both rising and falling edges. Length matching should be done for each data to their corresponding clock. As per RGMII specification the edges of clock and data are aligned by transmitter but must be delayed by half pulse width for receiver. MAC output delay differs between vendor types. DP83867 can be configured for aligned or shift mode and can introduce additional delay in 0.5 ns steps. See datasheet of DP83867 how to configure delay skew.

There are some application depending configuration not shown in Figure 32 like LED outputs. Texas Instruments also provides user guides and a reference design schematic for this PHY that should be considered.

Note: Boot Strapping is necessary for correct function and done by connecting a resistor divider to dedicated pins of DP83867. Selection of correct values are given within datasheet. Its strongly recommended to review and double check all strapping options before manufacturing.

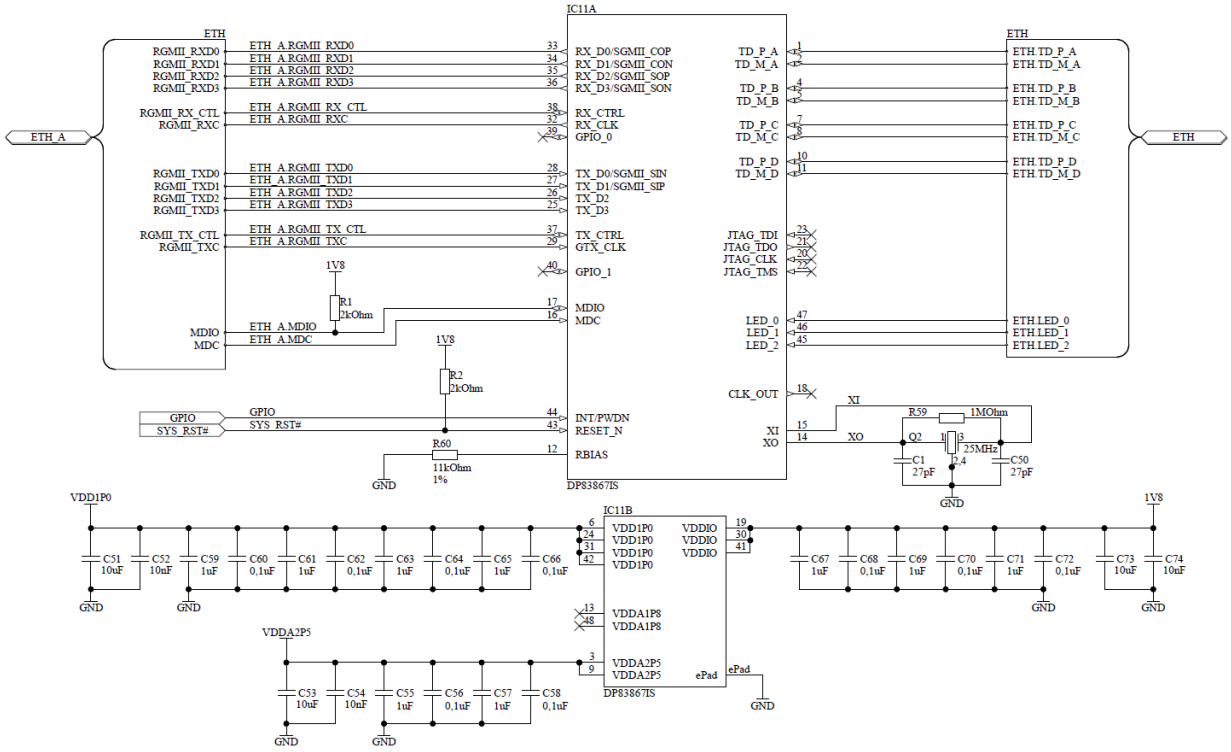


Figure 32 RGMII PHY Implementation

5.2.3.2 SGMII

This part will be released in future revision of this documentation.

5.2.3.3 RMII

This part will be released in future revision of this documentation.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.2.4 Ethernet MAC I/O Voltage Output

As OSM Specification allows 1.8 V, 2.5 V and 3.3 V for ETH A/B/C/D/E contacts Carrier Board implementation may need to detect which I/O voltage is delivered by OSM Module. Contact M17 (ETH_IOPWR formerly VCC_1_TEST) is a reference voltage output.

At the moment there is no recommended use case for this contact as this depends on combination of MAC, PHY and power design of Carrier Board.

5.2.5 GBE Carrier Connector Implementation Example

This part will be released in future revision of this documentation.

5.2.6 GBE Mag-Jack Connector Recommendations

This part will be released in future revision of this documentation.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.2.7 GBE LEDs

This part will be released in future revision of this documentation.

5.2.8 GBE software-defined contacts

The Precision Time Protocol (PTP) (according to IEEE 1588) is used to synchronize clocks throughout a computer network. If it is implemented in the hardware of the Ethernet controller clock accuracy in the sub-microsecond range can be achieved.

The Ethernet controller usually has several GPIO pins whereof one can be connected to one of the five ETH_x_SDP contacts. This contact can be used as output and distribute synchronized clocks or trigger impulses. When used as input it can synchronize the internal clock of the controller to external clocks for example from GPS receivers. Such a system could serve as a master clock.

These functions depend highly on the used Ethernet controller and wiring – check with your Module vendor.

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.3 PCIe

PCI Express (or PCIe) is a scalable, point-to-point serial bus interface commonly used for high speed data exchange between a PCIe host, or root, and a target device. It is scalable in the sense that there may be link widths, per the PCIe specification, that are x1, x2, x4, x8, x16 or x32. OSM currently calls out x1, x2 and x4 operation. Up to ten PCIe x1 links may be implemented on a OSM Module. There are four generations of PCIe defined, with each successive generation offering a speed increase, per the table below. The PCIe generation that may be supported on a particular OSM Module is design and SOC dependent.

Table 7 PCIe Data Transfer Rates

PCIe Generation	Link Speed (x1 link)	Encoding / Overhead	Net Data Transfer Rate (per lane)
1	2.5 GT/s	8b/10b 20%	250 MB/s
2	5.0 GT/s	8b/10b 20%	500 MB/s
3	8.0 GT/s	128b / 130b 1.54%	985 MB/s
4	16.0 GT/s	128b / 130b 1.54%	1,969 MB/s

PCI Express is defined in a series of documents maintained by the PCI Special Interest Group (www.pci-sig.org). The three most important documents to obtain are the Base Specification, the Card Electromechanical (CEM) Specification (which describes slot cards) and the Mini Card Electromechanical Specification (which describes the small format cards commonly referred to as Mini-PCIe cards).

The four possible PCIe links on a OSM Module are designated with net name prefixes PCIe_A_, PCIe B_, PCIe_C_ and PCIe_D_. Further there are management signals that are not associated to one of this four interfaces. The following table shows these contacts.

The I/O voltage of the digital PCIe signals is 1.8 V. See OSM Hardware Specification for details.

Note: As for all other differential signals there are no on-module AC coupling. This components must be placed on the Carrier Board.

Table 8 PCIe Management Contacts

Signal	Description	Notes
PCIe_REFCLK_P PCIe_REFCLK_N	Differential PCIe reference clock output	No caps needed
PCIe_CLKREQ#	PCIe reference clock request	Pull-Up to 1.8 V on-module
PCIe_WAKE#	PCIe Port wake up interrupt input	Pull-Up to 1.8 V on-module
PCIe_SM_ALERT#	SMBus Alert# (interrupt) signal	Pull-Up to 1.8 V on-module
PCIe_SMDAT PCIe_SMCLK	System management I2C bus DATA / CLK	Pull-Up to 1.8 V on-module

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

The interfaces PCIE A and PCIE B have a single PCIe (x1) lane each and the following signal set:

Table 9 PCIe Interfaces Contacts (PCIE A & B)

Signal	Description	Notes
PCIe_x_HSI0_P PCIe_x_HSI0_N	Data into Module	Capacitive coupled off Module
PCIe_x_HSO0_P PCIe_x_HSO0_N	Data out Module	
PCIE_x_PERST#	PCIe Port reset output	Place Pull-Up on Carrier Board

The interfaces PCIE C and PCIE D have a PCIe x4 lane each and the following signal set:

Table 10 PCIe Interfaces Contacts (PCIE C & D)

Signal	Description	Notes
PCIe_x_HSI[3:0]_P PCIe_x_HSI[3:0]_N	Data into Module	Capacitive coupled off Module
PCIe_x_HSO[3:0]_P PCIe_x_HSO[3:0]_N	Data out Module	
PCIE_x_PERST#	PCIe Port reset output	Place Pull-Up on Carrier Board

5.3.1 PCIe x1 Device Down on Carrier

An example of a PCIe x1 “device down” on the Carrier is shown below. Coupling caps on the OSM PCIe reference clock pairs are not needed on the Carrier. Coupling caps on the OSM PCIe TX & RX pairs are needed. They should be placed close to the source. Use 0402 package (or smaller) 200 nF X7R or X5R dielectric discrete ceramic capacitors. Do not use a capacitor array. Place the parts in a way to preserve the symmetry of the differential pair.

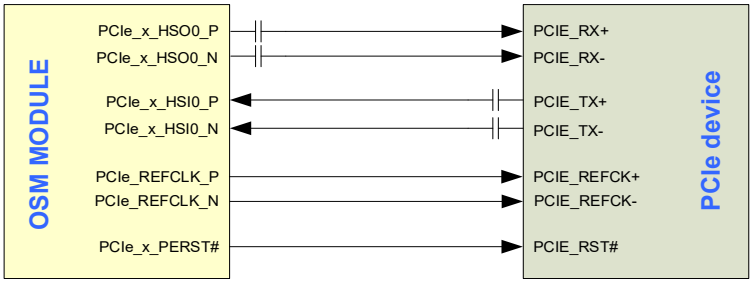


Figure 33 Interfacing a PCIe x1 Carrier Board Device

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.3.2 Mini-PCIe

A OSM Mini-PCIe implementation example is shown Figure 34. Mini-PCIe cards are defined to have pins for PCIe x1 and also a USB interface. A given card generally uses only one or the other. If you know exactly what Mini-PCIe card you plan to use, it is possible to omit either USB or PCIe. Generally, Mini-PCIe 802.11 WiFi cards use the PCIe interface and cellular modem cards use the USB interface.

In this example the reference clock is connected directly from OSM module. If more than one PCIe device is used a clock buffer is necessary to generate individual clock sources for each device. See chapter 5.3.3.

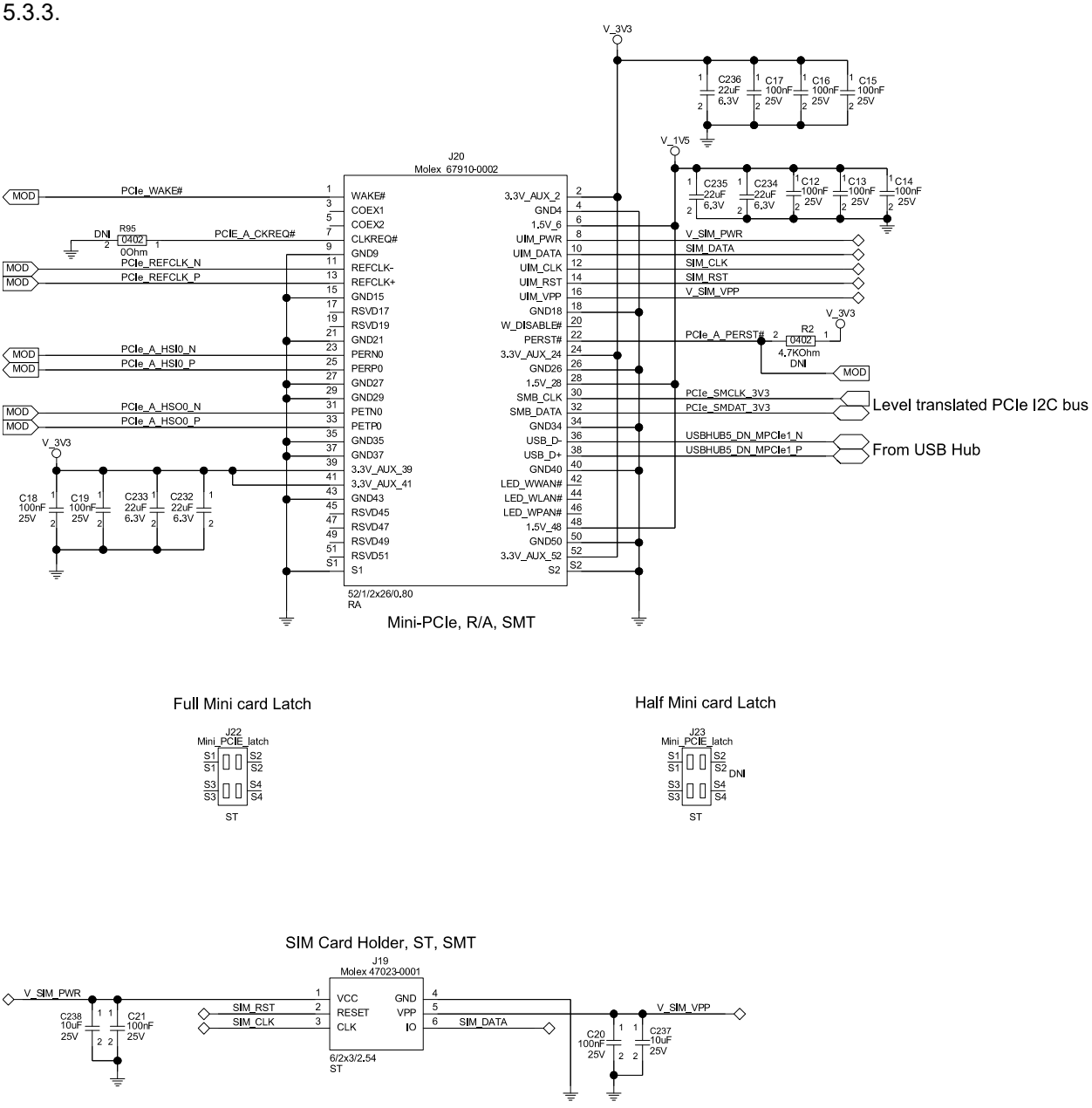


Figure 34 Mini-PCIe Slot

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.3.3 PCIe Reference Clock buffer

The OSM Hardware Specification defines one differential PCIe reference clock brought out of the Module. This clock is a 100 MHz differential pair and is sometimes known as a "hint" clock. The clock allows the PLL in the target PCIe device to lock faster onto the embedded clock in the PCIe bit stream.

If the Carrier board implements only one PCIe devices or slot, then the PCIe reference clock pair from the Module may be routed directly to that devices or slot. However, if there are more than one PCIe devices or slots on the Carrier Board, then the Module's PCIe reference clock should be buffered and distributed separately to the devices.

Note: A device which meets the jitter requirements for the intended PCI Express generation must be used.

There are a lot of clock buffers for PCIe applications that meet different PCIe specifications. First selection criteria should be the supported PCIe Generation to meet and the amount of clock outputs. Each target device (PCIe "device down" chip, slot, Express Card slot, Mini-PCIe device, M.2 device, PEG slot) should get an individual copy of the reference clock.

The 9DB233, 9DB433, 9DB833 have two, four and eight differential output copies of the input clock, respectively. Similar parts may be available from other vendors like Texas Instruments CDCDB400 or Diodes Incorporated PI6CDBL401B shown in the example in Figure 35.

The PCIe Clock buffers have both PLL and bypass modes. In some situations, it is preferable to operate the clock buffer in bypass mode.

The reference clock pairs should be routed as directly as possible from source to destination but there is no length matching between each reference clock pair neither between the PCIe data streams necessary.

Implementation of AC coupling and termination is depending on driver used in the clock buffer. As LP-HCSL outputs are used like in PI6CDBL401B or CDCDB400 there is no external termination or AC coupling necessary. Other types with traditional HCSL outputs like 9DB mentioned above may need parallel termination. Follow the vendors recommendations.

The following notes apply to the example of a clock buffer design in Figure 35**:**

- Each clock pair is routed point to point to each connector or end device using differential signal routing rules.
- SMBUS software can enable or disable clock-buffer outputs. So the SMBUS pins of the clock buffer should be connected to one I2C interface of the OSM Module. Configuration resistors or alternatively the SMBUS also allow software to put the clock buffer into "Bypass Mode", which experience has shown is needed in some Carrier situations.
- After power up all outputs are disabled per Pull-up. A PCIe-Card or device connected to the clock output pulls low the corresponding OE#-Pin by CLKREQ#-Signal from the device. (not shown in the example)
- PCIe_SMCLK and PCIe_SMDAT need to be level shifted to a 3.3 V I2C bus as described in 4.2.1 I2C Level Translation, Isolation and Buffering.

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

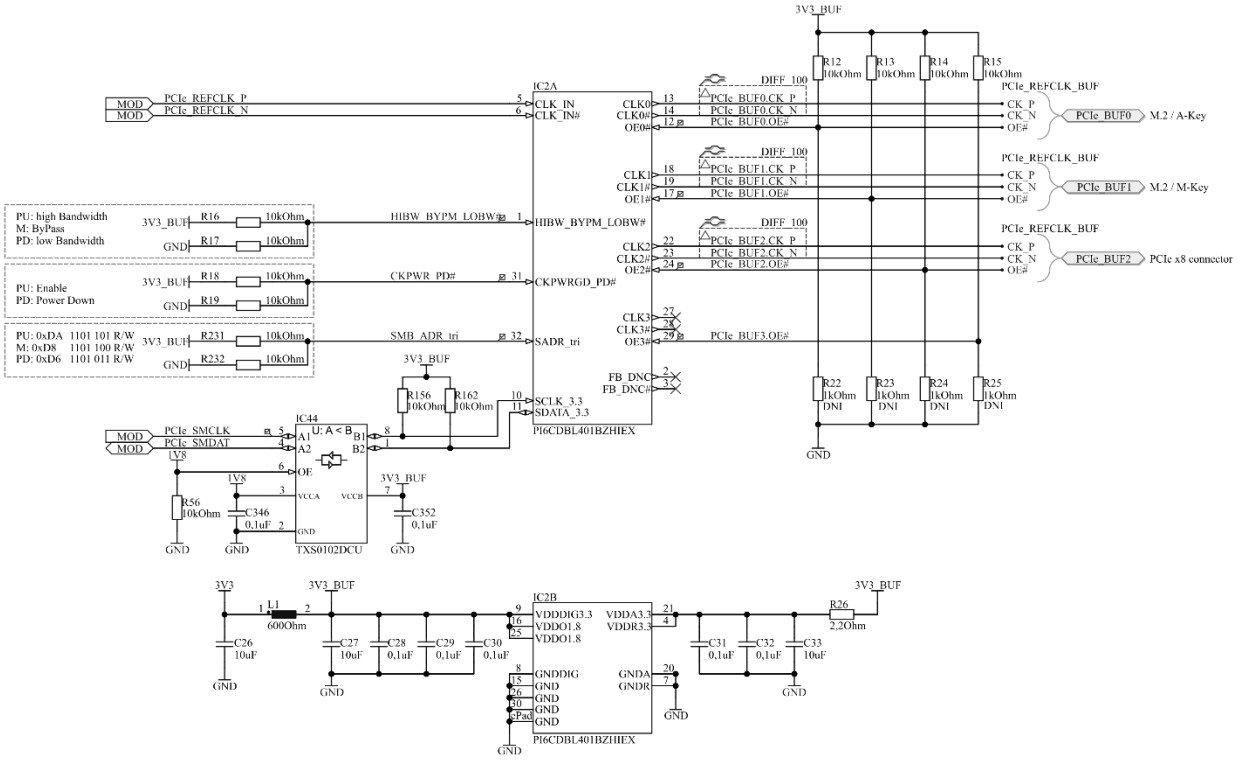


Figure 35 PCIe Clock Buffer

Note: The example in Figure 35 is supporting PCIe gen 3.

5.4 M.2

The M.2 form factor is a specification for mobile expansion cards and is supposed to replace the Mini PCIe cards and mSATA cards. The M.2 is a smaller form factor in both size and volume. It is a family of form factors that will enable expansion, contraction, and higher integration of functions onto a single form factor module solution.

PCIe, SATA, USB 3.0 and SDIO are provided through the M.2 connector. It is up to the manufacturer of the M.2 host or device to select which interfaces are to be supported. The M.2 connector has different keying notches that denote various purposes and capabilities of M.2 hosts and modules, preventing plugging of M.2 modules into feature-incompatible host connectors.

M.2 cards are available in various physical sizes, starting from 1630 wireless cards, up to 22110 or 25110 SSDs.

Carrier Board designers must provide a stand-off for each physical card size they would like to support.

The module stand-off should be directly connected to Carrier board's GND, as it is part of the M.2 Electrical and Thermal Ground Path.

The M.2 standard defines different pinouts that are separated by keys to avoid miss-plugging of cards. Some of the most widely used keys given in the following chapter.

5.4.1 B keying

M.2 Key B sockets support a wide range of add on cards, like SSDs, GPS and WiFi devices.

Some high-speed interfaces like SATA and PCIe share the same pins at the M.2 Key B connector.

The desired interface configuration can be decoded by CONFIG_[3:0] which are either tied to GND or left floating by the M.2 card.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

At the time of writing, a majority of medium-speed (SATA) SSDs implement dual-keying which allows to plug them into Key B and Key M sockets.

High-End SSDs often come in a Key-M only format, as they rely on a PCIe x4 link.

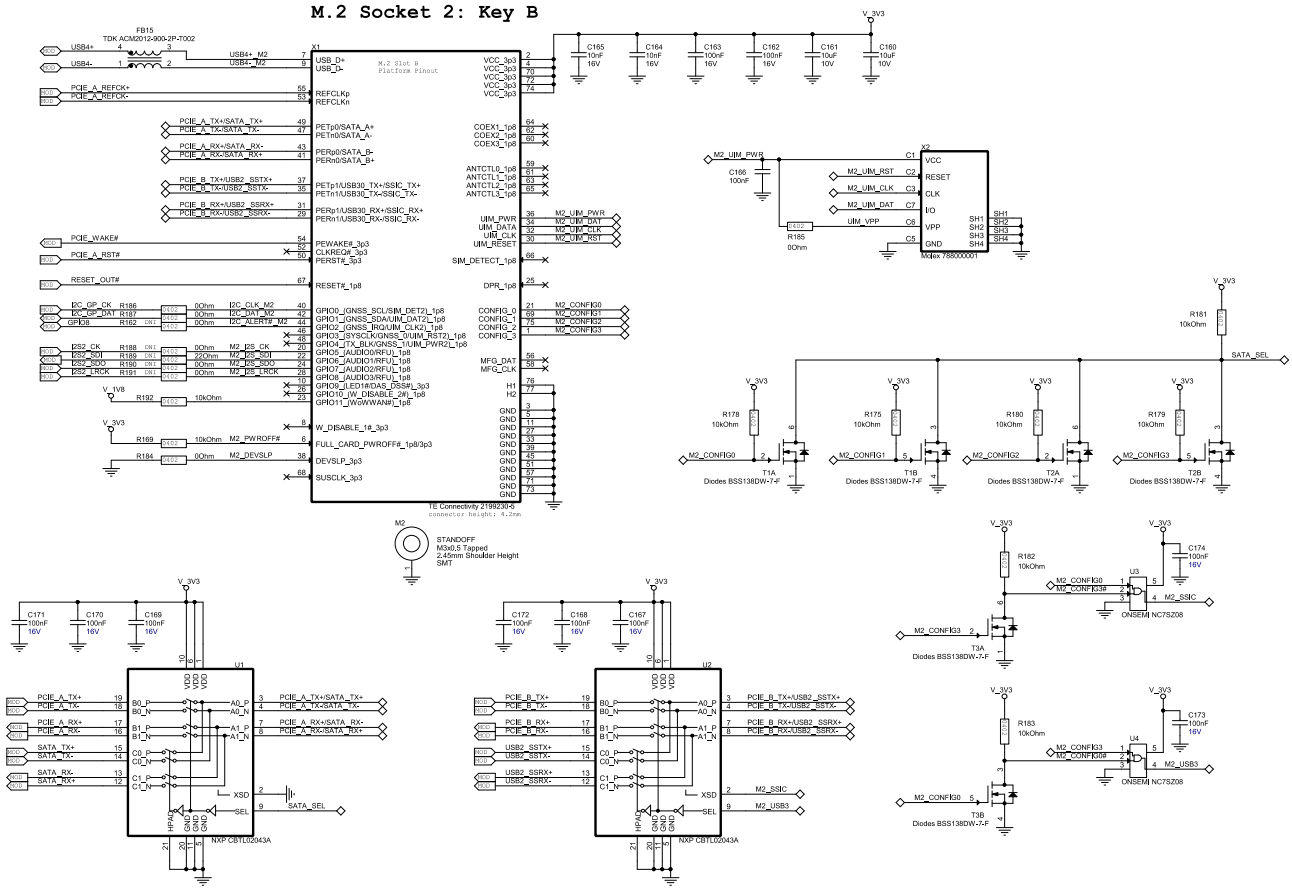


Figure 36 M.2 Key B

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.4.2 M keying

M.2 Key M is intended for use with SSD Cards. The connection can either be done by PCIe x4 or a single SATA lane.

In this example schematic both PCIe and SATA is connected to the M.2 socket according to the M.2 specification.

The M.2 SSD decides with configuration pins, which interface should be used for the inserted SSD.

It is recommended to check with your OSM Module vendor if PCIe x4 is supported by the used OSM Module, if PCIe x4 SSD will be connected. This usage would consume all available PCIe lanes from the Module. Other PCIe devices could only be used if a PCIe bridge is implemented on the Carrier board. Both used interfaces by the M.2 SSD and the OSM Module must match.

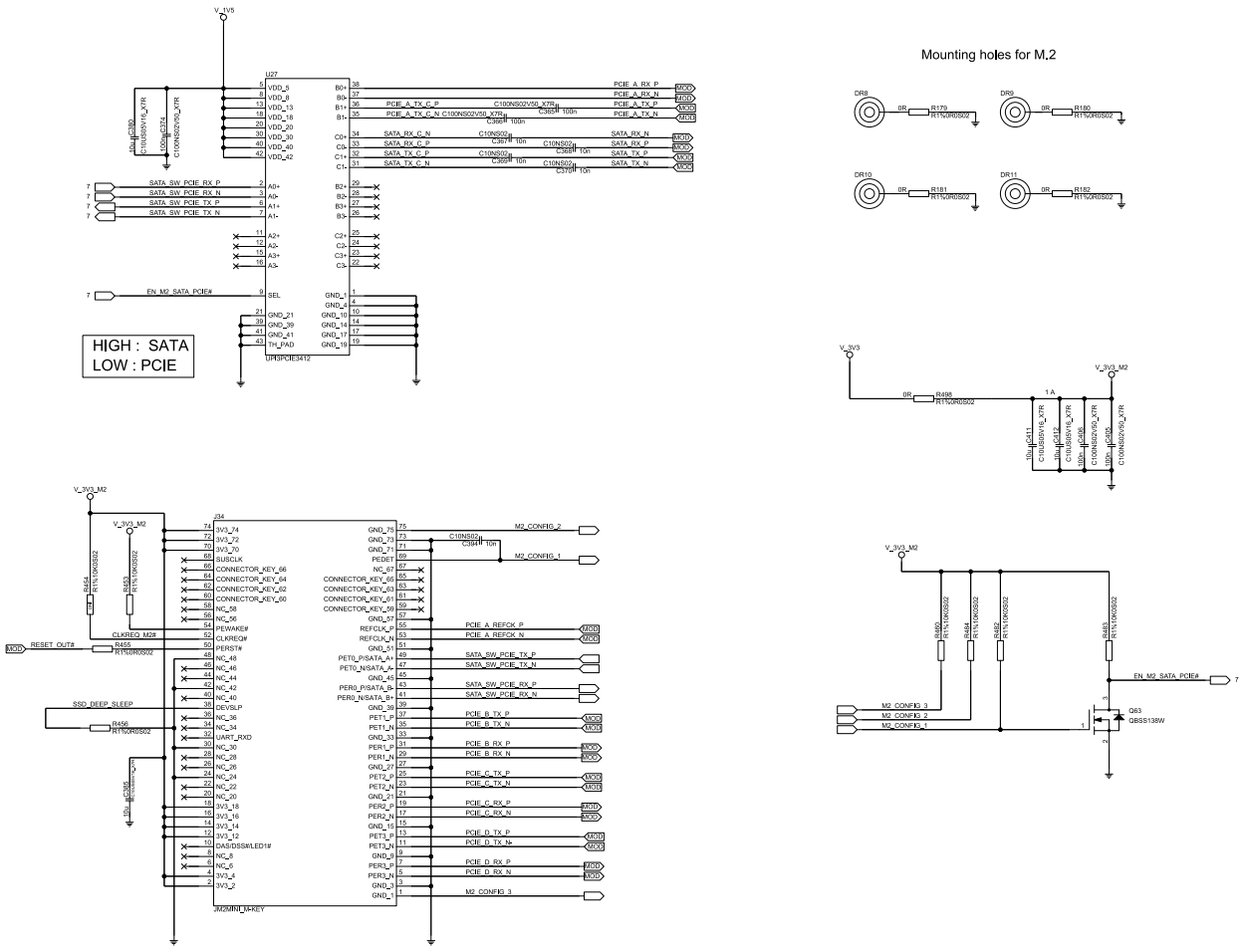


Figure 37 M.2 Key M

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

5.4.3 E keying

M.2 Key E is intended for use with Wireless Connectivity cards, which are WiFi / Bluetooth cards in most of the cases. WiFi is utilizing either PCIe or SDIO connection to the host system. It is recommended to check with your OSM Module vendor if SDIO could be used for WiFi devices as well.

USB or UART+I2S are used to connect the Bluetooth Interface IC to the Host system. NFC capable add-in cards may also require an I2C connection. Please be aware that the I/O voltage of I2C was changed from 3.3V to 1.8V per ECN after the official M.2 specification release.

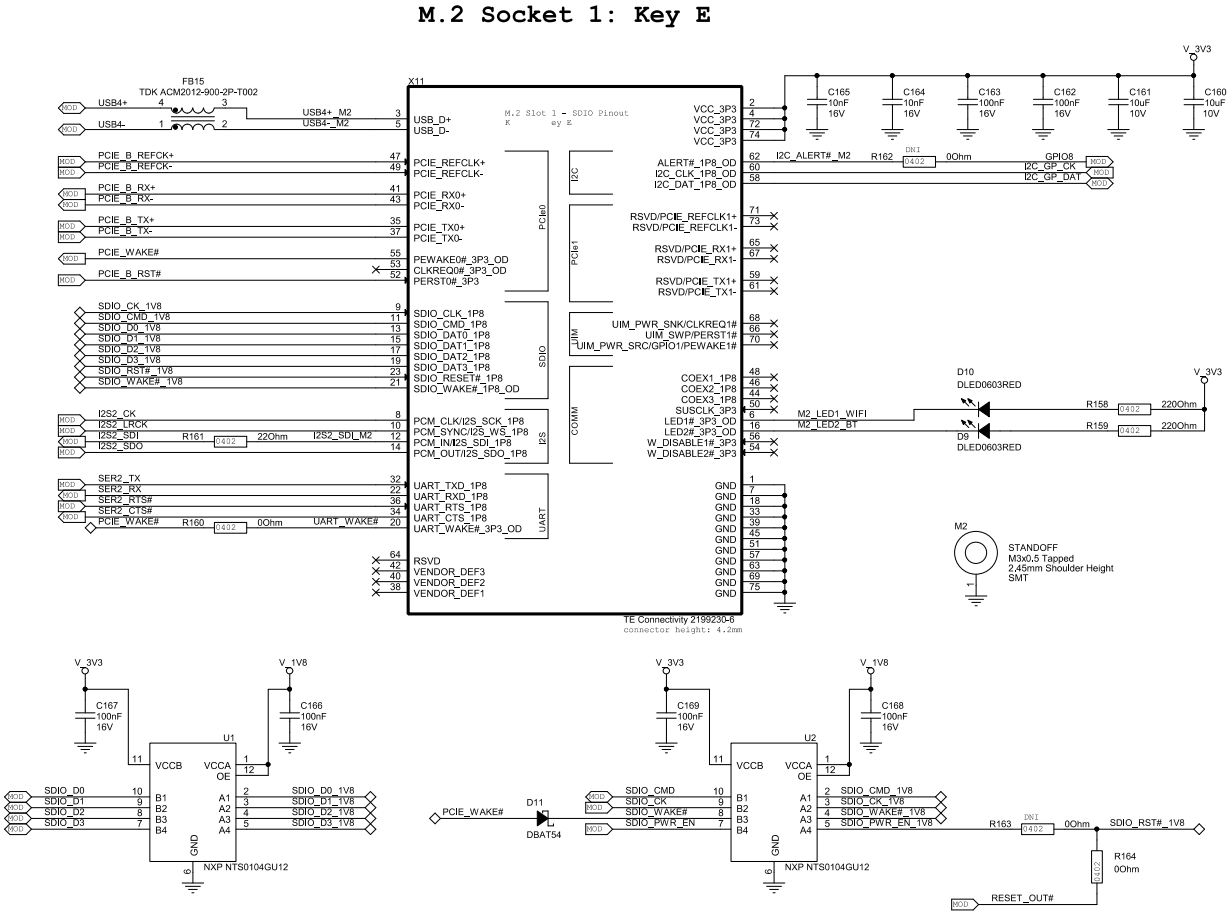


Figure 38 M.2 Key E

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

6 SDIO INTERFACE

The SD (Secure Digital) Card is a non-volatile memory card format used as mass storage memory in portable devices. The SD standard is maintained by the SD Card Association. OSM Modules support SD cards over the OSM SDIO interface. The interface may be used in a 4 bit or 1 bit mode with up to 208 MHz. If used in 1 bit mode, the least significant bit (DATA0) should be used. Most OSM Modules offer a SDIO BCT boot and an SDIO OS boot. Since SD cards can (usually) be inserted and removed by the user, it is important to implement ESD protection on all the SD lines.

OSM specifies two SDIO-Interfaces. SDIO A with 4 bit data lanes is intended to be connected to SD Card whereas SDIO B may be connected to an e-MMC or other SDIO periphery like wireless modules.

6.1 SD Card Implementation

The example below shows a standard connection for a Micro SD Card. This works for standard SD Card as well.

Supply voltage of the SD Card is fixed 3.3 V but signaling voltage can be 3.3 V or 1.8 V depending on selected speed mode by the host controller. The fastest SD-Card Bus Interface that is supported is UHS-I with 104 MB/s (SDR104) initially specified by SD standard Version 3.01.

For a total reset of the SD Card its necessary to switch off the supply voltage. Some SOC on the OSM Module may support dedicated contact SDIO_x_PWR_EN for an SD Card power cycle but some may use reset signal. Ensure that the SD Card supply voltage is switched on per default without any boot or OS function to allow boot from SD-Card.

Note: There are power switches available with bleed out feature to ensure that SD Card power supply is discharge to a specific voltage level. For example, see On Semi NCP45520.

Both Card Detect (CD#) and optional Write Protect WP (not used on Micro SD Card) already have a Pull-Up to 1.8 V or 3.3 V on the OSM Module. Ask your Module vendor if additional Pull-Ups are recommended.

In most cases Pull-Ups on DATA and CMD signals are implemented on Carrier Board as well. However, SOC on the OSM Module may use internal Pull-Up that are sufficient in most applications. When using additional pull-ups for DATA and CMD signal on the carrier board, use SDIO_x_IOPWR as pull-up voltage.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

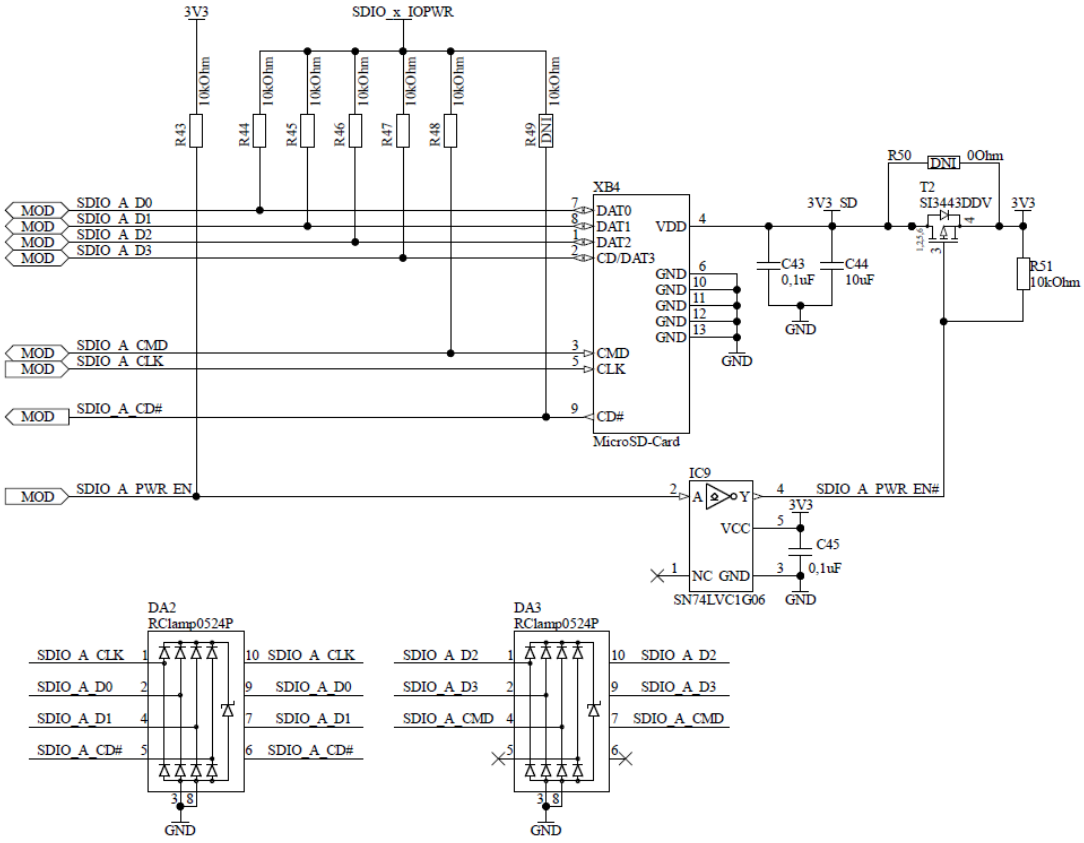


Figure 39 SD Card Interface

6.2 SDIO / Wireless Modules

Depending on the OSM Module the SDIO interface can be used to connect to a wireless module (WiFi, Bluetooth). There are a lot of vendors with different types and solutions. Texas Instruments WL18x7 has built in Dual-Band WiFi and Bluetooth Front-End.

Carrier Board designer should select the right SDIO interface regarding the OSM Module features and application requirements. For example, if OSM Module uses SDIO A as primary boot interface for SD-Card, SDIO B should be used for wireless module. SDIO B than only uses 4 bit mode if supported by SOC. As described in section 6 SDIO B is intended but not must-have for wireless modules.

The I/O voltage of the SDIO module should be considered to decide whether a level shifter is needed or not. For example, WL18x7 use 1.8 V signaling for SDIO signals and therefore to be fully compatible for different OSM Modules a level shifter is recommended. An example solution is shown in Figure 40.

Further design examples and development notes can be found within the online design resources of the SDIO module vendors.

6.3 SDIO I/O-Voltage

All contacts of the SDIO interfaces are specified for 1.8 V or 3.3 V but there are some basic rules that differ for SD-Card interfaces compared to SDIO interface.

6.3.1 SD-Card

For both SDIO A and SDIO B the I/O voltage of contacts CMD, CLK and D[3:0]/D[7:0] are switched between 1.8 V and 3.3 V by the OSM Module as part of the SD-Card protocol when implemented as shown in Figure 39. Voltage switching does not conflict with any Carrier Board design.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Regarding WP and CD# the voltage is not switched depending on speed mode, but for some SOC they are also part of the voltage domain for SDIO signals on the OSM Module. For that reason this inputs thresholds may are relative to 1.8 V or 3.3 V. Ask your Module vendor for details of used I/O voltage. Further Pull-Ups for both voltages can be used as alternatives.

Do not use SDIO_x_IOPWR to supply an SD Card. This will cause malfunction and conflicts with minimum allowed VCC voltage of SD Card. This voltage is intended for voltage level shifting and/or DATA/CMD pull-ups.

Note: Do not connect 1.8 V to VCC of SD-Card. 3.3 V is the only allowed voltage for standard High-Voltage Cards up to UHS-I cards shown in Figure 39.

Note: The SDIO_x_WP is used on the OSM Module with a Pull-Up. If not considered at the Carrier the uSD/ SD card will be automatically write protected. To enable write access to the card it is suggested to use a Pull-Down resistor with a value of 1 kΩ or below on the Carrier.

Note: Some SD card connectors do not offer a card detect switch. If the signal SDIO_x_CD# is interpreted by the Module software, it is necessary to pull this signal to GND at the Carrier with a Pull-Down resistor of 1 kΩ or below.

6.3.2 Other interface types

For SDIO interfaces the I/O-Voltage is specified by module vendor and there will be likely one fixed voltage. To be flexible on Carrier Board all SDIO signals can be connected to level shifter with independent reference voltages. SDIO_x_IOPWR than can be used as the reference voltage between OSM-Module and level shifter. Figure 40 shows an example how to solve a compatible design with an Texas Instruments TXS0108 bidirectional level shifter.

Contact SDIO_x_IOPWR is a power output where Carrier Board can sink 100 mA from. Higher currents may be specified by Module vendor. This contact allows to connect voltage translators or other periphery that need to know the SDIO voltage.

Typically SDIO_x_IOPWR carries out the I/O voltage of the SOCs SDIO voltage domain.

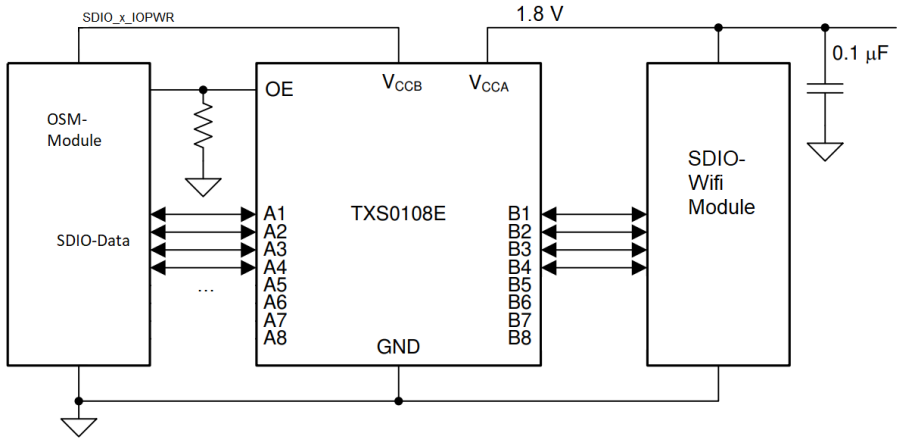


Figure 40 Voltage translation for SDIO voltage

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

7 CAMERA INTERFACES

This part will be released in future revision of this documentation.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

8 GPIO

It is possible to use up to fourty GPIOs coming from the OSM Module depending on Module size. If these are not sufficient additional IO expander can be used to generate additional GPIOs.

8.1 OSM Module Native GPIO

OSM Modules support up to fourty general purpose I/O contacts grouped into 5 bytes: GPIO_A_[7:0] to GPIO_E_[7:0]. Each of these can be configured as an input or output contact and have an optional interrupt capability.

GPIO_C_6 and GPIO_C_7 have a dual function for CAM_PWR and CAM_RST#. Ask your Modul vendor if these functions are implemented.

OSM Modules generally allow the GPIO to be configured to generate an interrupt.

GPIO_A_[7:0] and GPIO_B_[7:0] should always be present. All other GPIO contacts are optional. Please check the Module documentation for support or contact your OSM Module vendor.

OSM Modules use a GPIO voltage level of 1.8V. The maximum output current per contact is defined by Module vendor as this depends directly on the electrically specification of the SOC.

8.2 GPIO Expansion

For a low cost, easy way to implement additional GPIO ports, see section 4.2.3 I2C Based I/O Expanders.

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

9 CARRIER POWER CIRCUITS

9.1 Power Budgeting

One of the early steps in a OSM Carrier design is to develop a power budget and a strategy for meeting that budget. All the power rails need to be identified and worst-case current consumptions listed. A spread-sheet is usually developed. The power circuits should be designed to meet the worst case numbers, but the actual system power consumption will usually turn out to be quite a bit less than the total indicated by the total worst case numbers for each individual rail. Once there is an understanding of the amount of power required, a plan can be developed for meeting the requirements. A sample power budget sheet is shown in the table below. This example is hypothetical and serves to illustrate the process. It assumes that the OSM Module is to be supplied by a fixed 5 V DC source. A variable battery power source would result in a different sheet.

Table 11 Hypothetical Power Budget Example

Function	12 V Current	5 V Current	3.3 V Current	1.8 V Current	1.5 V Current	Power	Notes
Display Backlight	0.6 A	-	-	-	-	7.2 W	
USB	-	2.0 A	-	-	-	10.0 W	4 devices each 0.5 A
USB 3.0	-	1.8 A	-	-	-	9.0 W	1 device
OSM Module	-	2.0 A	-	-	-	10.0 W	Module under heavy load
Mini PCIe Module	-	-	1.0 A	-	1.0 A	4.8 W	
Audio Circuits	-	0.3 A	-	0.1 A	-	1.68 W	
Misc. Carrier Circuits	-	-	0.25 A	0.1 A	-	1.0 W	
Current Subtotals	0.6 A	6.1 A	1.25 A	0.2 A	1.0 A	-	
Power Totals	7.2 W	30.5 W	4.12 W	0.36 W	1.5 W	43 W	

The total shown is a worst case value, and power circuits should be designed to handle the worst case. However, experience shows that typical average system power consumptions are significantly less, on the order of 50 % of worst case. The total above does not account for power conversion losses. These are added in a later section, when this hypothetical example is continued.

Many OSM Module vendors offer evaluation platforms, and it is worth the time and effort to roughly prototype the target system with available hardware and software. This can validate power estimates and have other benefits, such as allowing performance benchmarks to be carried out before committing to the full system design.

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

9.2 Carrier Input Power Sources

For a typical Carrier Board design with USB and Display functions a voltage of typ. 12 V or 24 V is suggested. Fixed 5 V supply is also suitable for cost optimized Carrier Boards supporting Size-0 / Size-S modules only. The following table shows some different input voltages.

Table 12 Carrier Input Power Source Possibilities

Power Source	Voltage	Notes
3.3 V Fixed	3.3 V +/- 5%	Possible, but not a common choice, as often there are significant power requirements for USB (5 V at up to 500 mA for each external USB 2.0 port) and the display backlight supply (12 V at up to 600 mA is common), requiring up (boost) conversion. Most OSM Modules may not support 3.3 V power input.
5 V Fixed	5.0 V +/- 5%	Allows some of the higher power consuming devices (USB, OSM Module) to be fed directly without conversion. Other, lower current devices require power conversion. Be aware that modules specification
12 V Fixed	12 V +/- 5%	Common choice – Allows display backlight to be powered directly, without conversion (if the display backlight accepts 12 V). Requires buck conversion of 12 V to 5 V for Module and for Carrier USB and other functions.
Battery - Single Level Lithium Ion Cell	3.6 V nominal	4.2 V fully charged; 3.0 V discharged. Buck/Boost Converter is used to fed OSM-Module.
Battery - Two Level Lithium Ion Cells	7.2 V nominal	8.4 V fully charged; 6.0 V discharged. Step-Down Converter is used to fed OSM-Module.
Battery - Three Level Lithium Ion Cells	10.8 V nominal	12.6 V fully charged; 9.0 V discharged. Step-Down Converter is used to fed OSM-Module.
Wide Range DC	10 V – 30 V (Typical)	Wide range input power supply is possible. Note that to handle higher voltages, parts rated for use at the higher voltages must be used.
Power Over Ethernet	48 V	IEEE802.3af POE standard allows 12.5 W load power IEEE802.3at POE standard allows 25.5 W load power IEEE802.3bt POE standard allows up to 71 W load power The POE supply output is transformer isolated from the GBE lines, with 1500 V DC isolation. POE supply output voltages are design specific – 24 V, 12 V and 5 V outputs are common.
Automotive	12 V nominal	When the engine is off, the supply battery voltage is 12 V nominal. During engine cranking, the supply can dip to 6 V. When the engine is running, the DC level can be up to about 16 V, with a 14.4 V level being typical. Transients in excess of +/- 100 V are common. A user may disconnect the battery and reconnect it with the polarity reversed. All in all, it's a harsh environment that needs careful attention. A basic strategy is to have an input network with good transient and reverse polarity protection, and then use a rugged switching

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

		supply that can handle an input range from 6 V to 24 V, and deliver a 5 V output to the OSM Carrier.

9.2.1 5 V Input

The power entry connector for this fixed 5 V power source example is shown in the figure Figure 41 below. There are two paths, given net names V_MOD_IN and V_CARRIER_IN. Both carry 5 V in from a single bench supply. The nets are separated to allow separate current (and power) measurements of the OSM Module and the Carrier board. If this separate measurement capability is not needed, then the separate entries could be combined into a single net.

Note: Figure 41 shows a solution for prototypes or test scenarios. For mass production both nets should be connected in PCB layout.

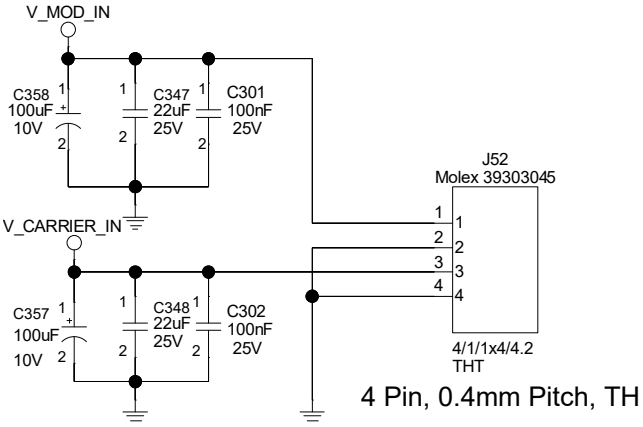


Figure 41 Input Connector

When supplying the OSM module directly with V_CARRIER_IN, which in this case is 5 V, its important to hold off the Carrier Board circuits from being powered by 5 V until the module asserts CARRIER_PWR_EN signal. Figure 42 illustrates a power switch used for this.

Some Carrier circuits, such as those involved in power management and those that are in the “Module Power Domain” as defined by the OSM Module specification, may be powered whenever the Module has power, before (and after) the assertions of CARRIER_PWR_EN.

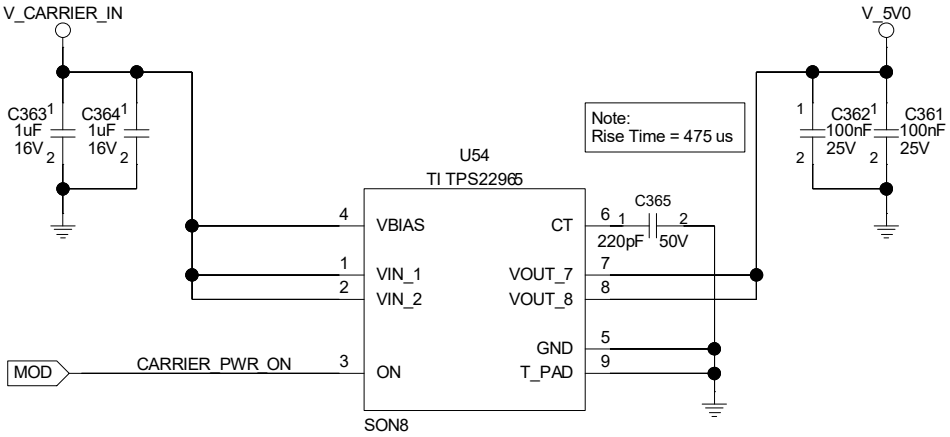


Figure 42 Carrier Power Switch for 5 V / 6 A

The following three figures illustrate buck (or step-down) switching converters that create 3.3 V, 1.8 V and 1.5 V from the V_CARRIER_IN (5 V) power source. Since the power needs on these rails are modest,

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

integrated switchers with internal power FETs are well suited to the job. They are physically small and robust. The parts shown are from Texas Instruments, although similar parts exist from other vendors.

The figures show three separate enables for the three supplies, with net name designations V_3V3_EN, V_1V8_EN and V_1V5_EN. Sources for these nets are not shown. These enable pins should be driven to the “enabled” state when signal CARRIER_PWR_EN is high. They could be driven by CARRIER_PWR_EN directly, by V_5V0, or by other Carrier circuitry. If the situation demands aggressive power management, it may be desirable to have Carrier I/O circuits that allow the various enables to be brought low if the power rail is not needed. If this is done, the designer should arrange that the enables do not go high before CARRIER_PWR_EN is high.

The LEDs and signal FETs on the right side of the three figures are optional. The LED lights up as a status indicator when the power rail (V_3V3, V_1V8 or V_1V5) is up. The FET prevents leakage from the main power rails (V_MOD_IN and V_CARRIER_IN) when the switchers are powered down. Rail V_MOD_IN_LED ties to V_MOD_IN through a removable jumper. Removing the jumper prevents the LEDs from burning power in standby states (and in all states).

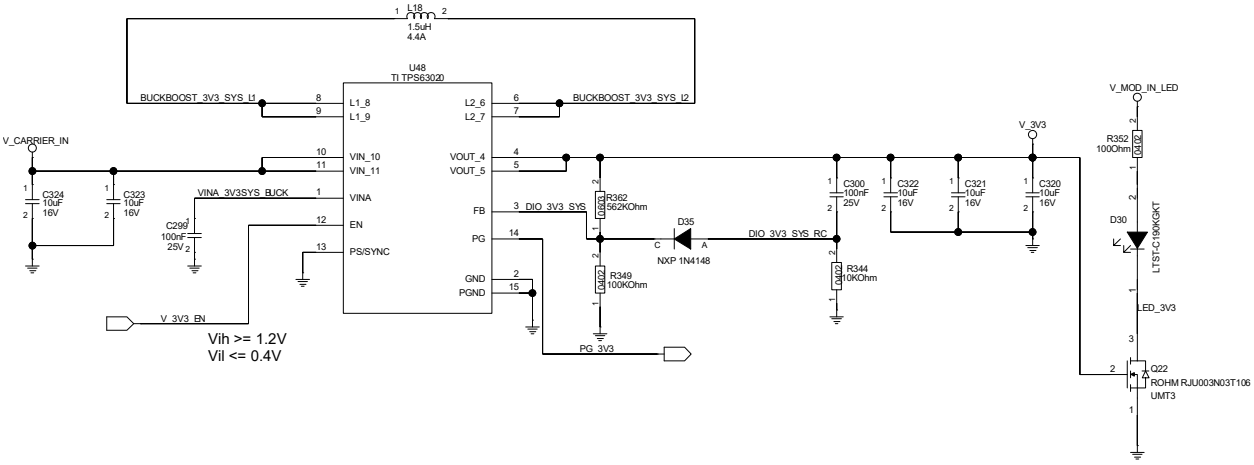


Figure 43 Buck Converter 3.3 V / 2 A

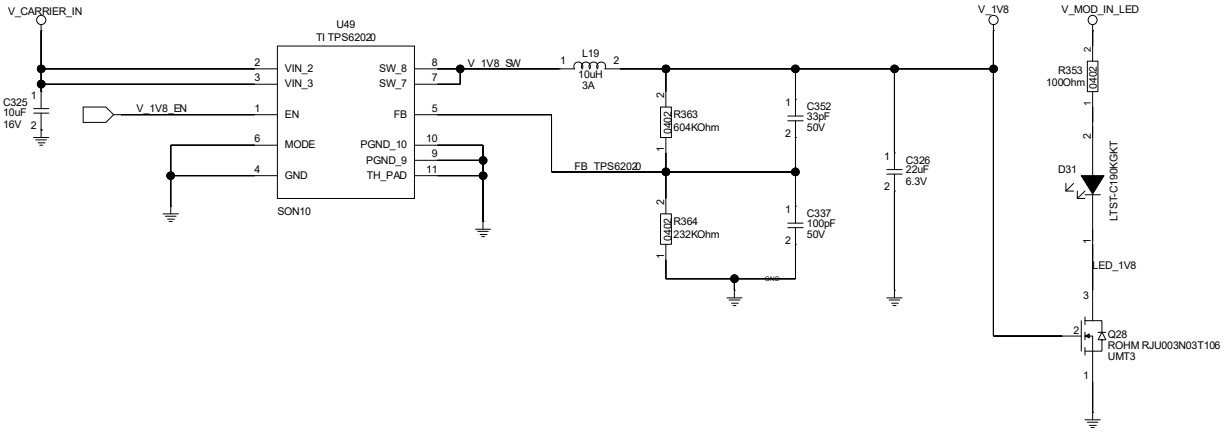


Figure 44 Buck Converter 1.8 V / 0.6 A

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

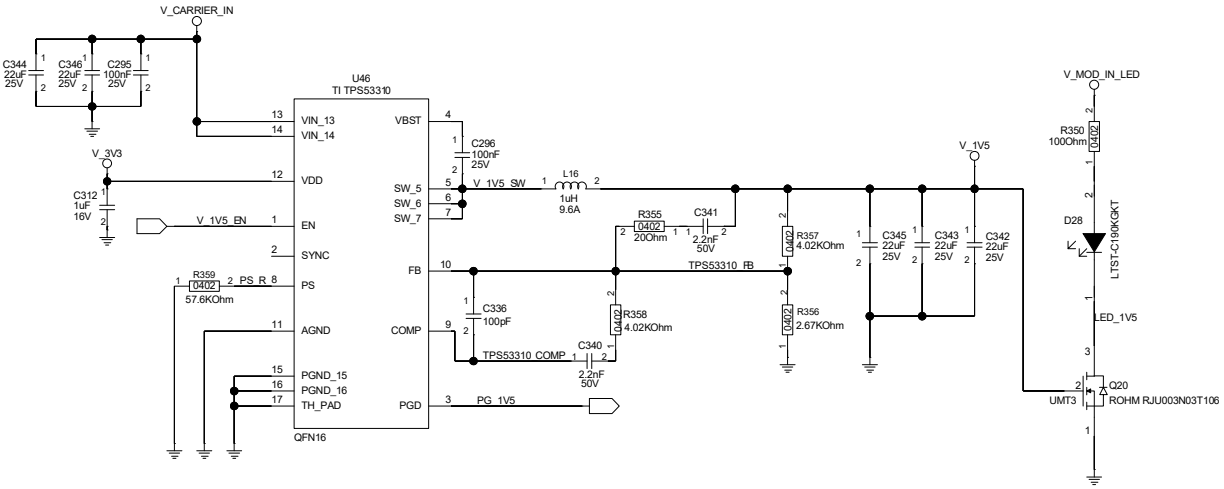


Figure 45 Buck Converter 1.5 V / 3 A

Many LCD backlights require a 12V power source. If the system power source is a fixed 5V supply, or a battery supply well under 12V, then a boost converter circuit is needed. An example is shown here:

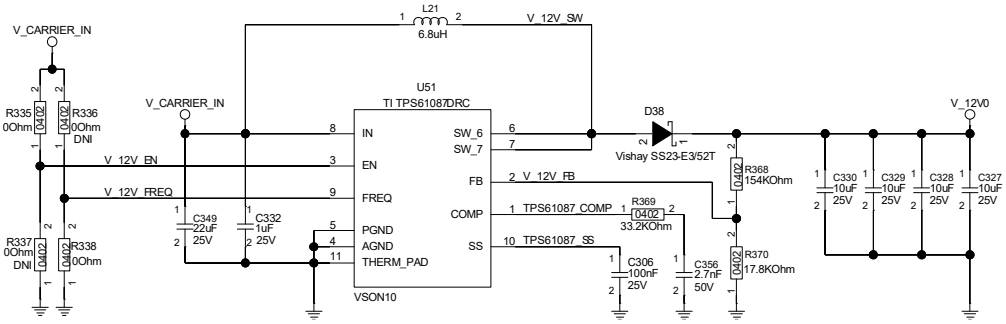


Figure 46 Boost Converter for Backlight-Power 12 V / 3.2 A

9.2.2 12 V Input

There are many choices for switching power supply circuits to step a 12 V input down to lower voltages for OSM Module and Carrier use. An integrated switcher possibility from TI is shown in the following figure.

Note: Regulator shown in Figure 47 has an internal switch limiting the efficiency of the regulator. Depending on application one can use regulator with external switch.

Depending on the module the regulator can be changed to be configures for 3.3 V output voltage which is recommended input voltage of a Size-0 module.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

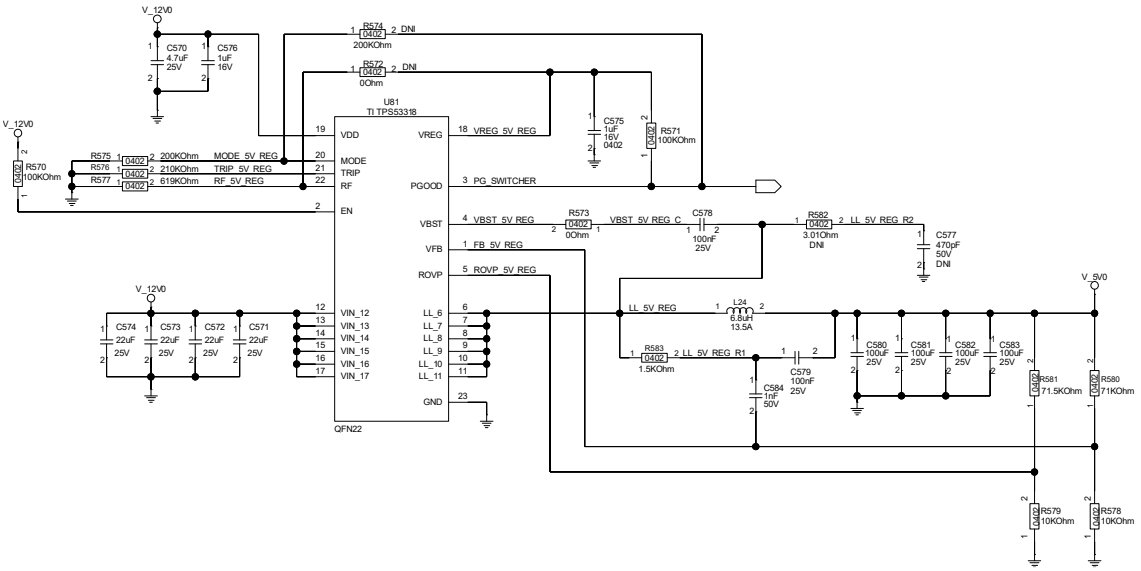


Figure 47 Step Down Switcher 12 V to 5 V / 8 A

9.2.3 Wide Range Power Input

In some applications it is desirable to allow for a wide range power input. This is the case in certain industrial and automotive settings. Since OSM systems operate at low voltages (5 V and under, apart from LCD backlight considerations), it is straightforward to implement a wide range buck converter. The figure below shows an example implemented with the Linear Technologies LTC3879 with an input range from 10 V to 30 V. Similar parts are available from other vendors. The Texas Instruments TPS40170 is another part to consider for this application. The TPS40170 allowable input range spans 4.5 V to 60 V. If you are targeting the higher input ranges, be sure that components exposed to the input voltage are adequately rated for that high voltage.

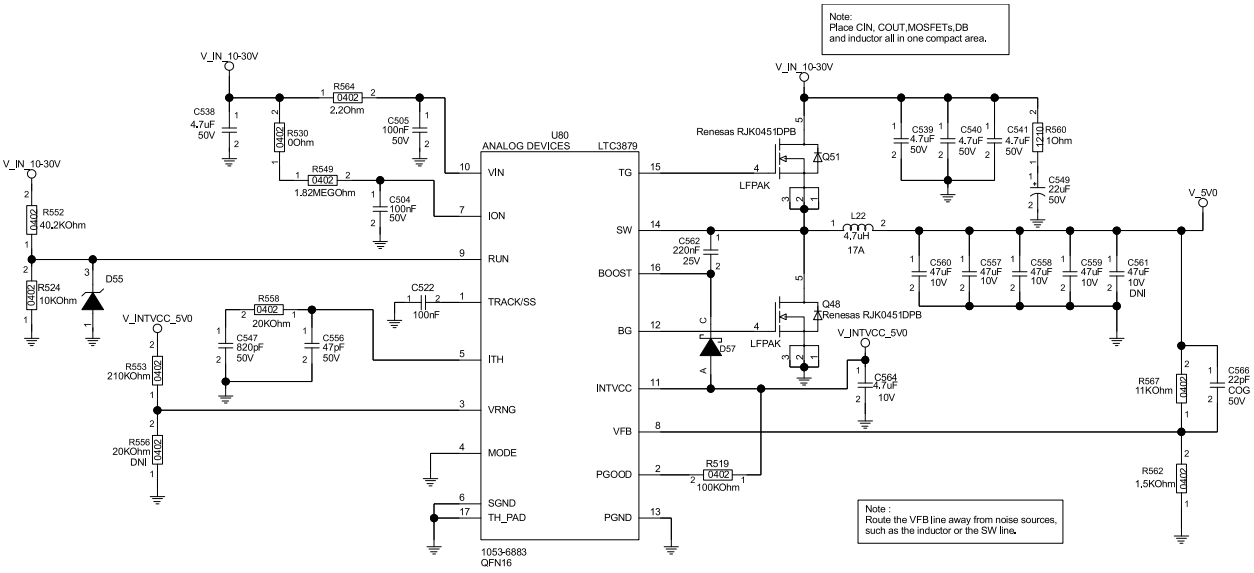


Figure 48 Wide Range 10 V - 30 V to 5 V / 12 A

If the load on the Carrier 3.3 V is high, it may be worth having a second wide input range switcher per the above figure, configured for the 3.3 V output.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

9.3 Power Hot Swap Controller

Hot swap controller circuits can be used to control the system power supply rise time. This may be desirable when plugging circuits in live to low impedance sources, such as a battery. The figure below illustrates a high-side protection controller circuit using TI LM5060. The N-Channel MOSFET isolates the input supply (V_CARRIER_IN) from the rest of the board (V_HTSWP_OUT). The circuit limits the in-rush current and provides a power good signal once the output voltage reaches the input voltage. An option is provided to enable LM5060 (HTSWAP_EN) from a CPLD or other source as well as using a switch / jumper.

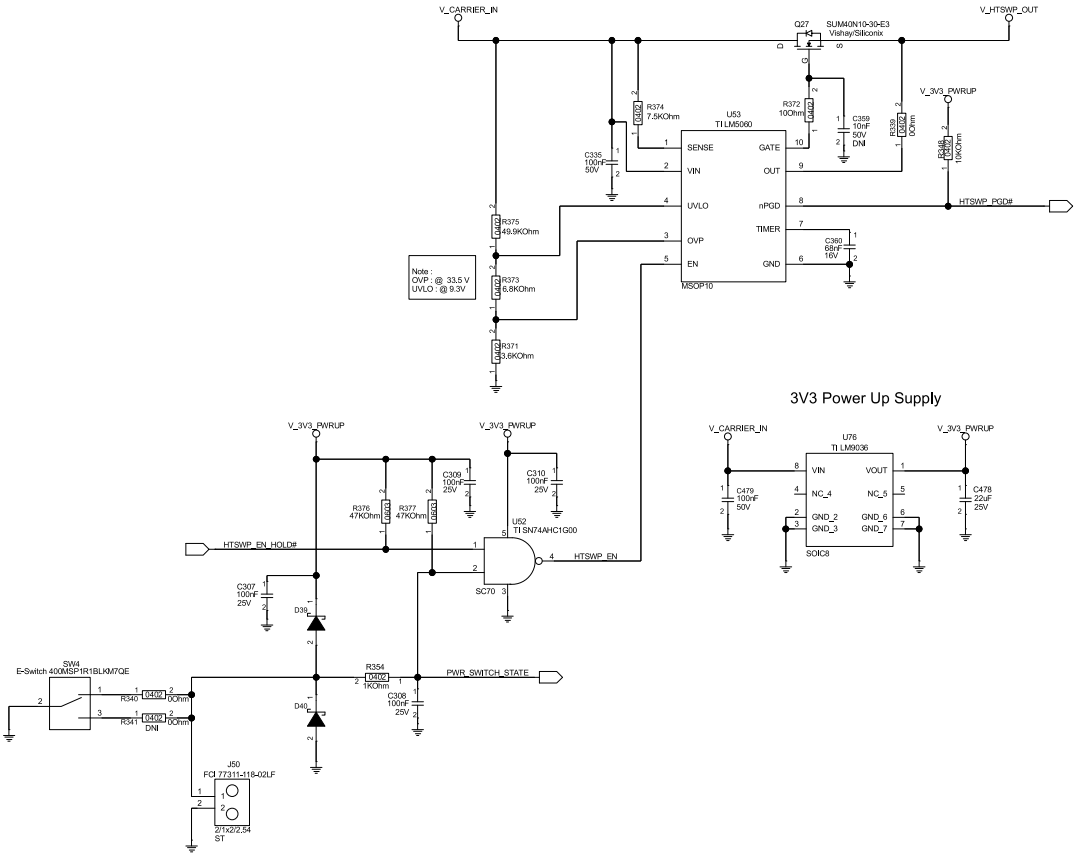


Figure 49 Hot Swap Controller

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

9.4 High Voltage LED Supply

Some LCD panels have multiple sets of series LED strings that are driven by a high voltage LED supply. Vendors such as TI and Analog Devices provide the ICs for these supplies. A schematic example using a TI high voltage LED supply is given below.

The LED brightness can be controlled either using PWM control (if the IC VDDIO pin is set LOW) or by I2C (if VDDIO is HIGH). A level translator needs to be used for signals VSYNC and PWM.

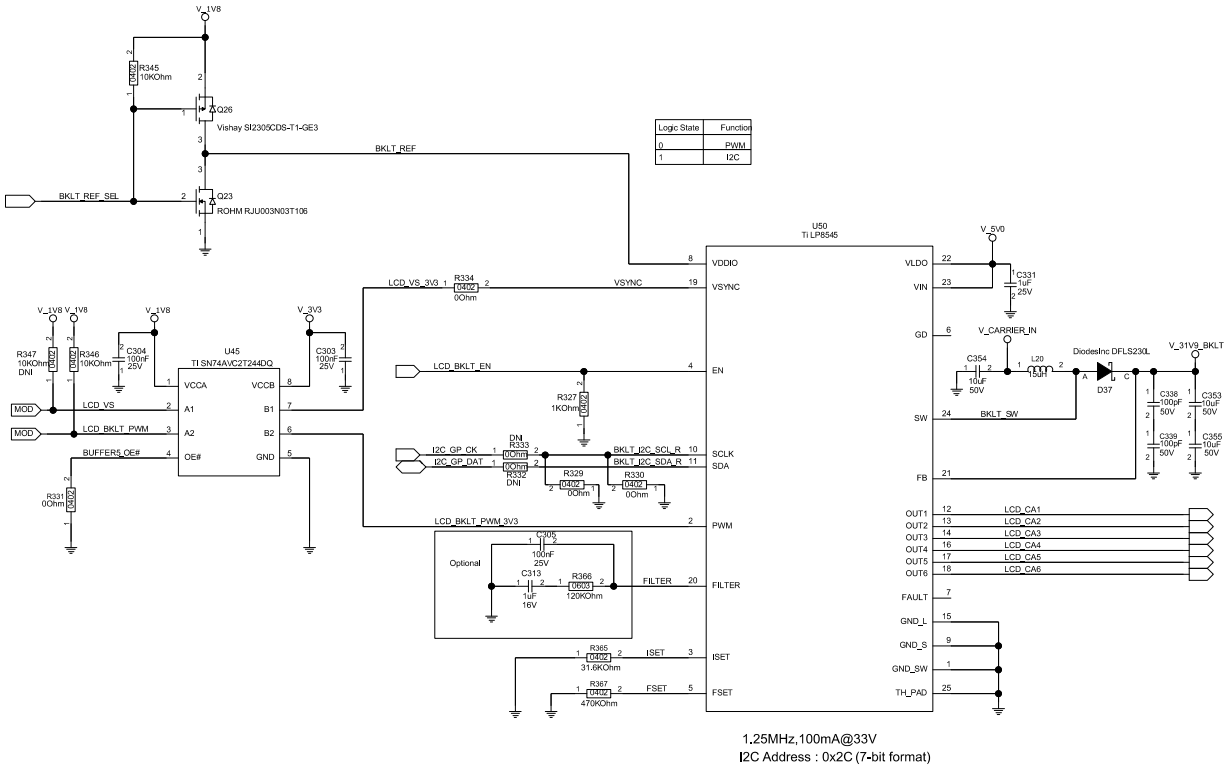


Figure 50 LP8545 LED Backlight Power

Note: The output voltage and current need to be defined for the related backlight. In this example 33 V and 100 mA is selected.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

9.5 Voltage Monitoring

Monitoring the main voltages on Carrier Board may be necessary to allow reliable function after power up. The OSM module may monitors its own internal voltages. All carrier voltages need to be monitored by the carrier.

Typically, in case of a failure of monitored voltages a reset of the system will be asserted by pulling RESET_IN# low by the Carrier Board.

Carrier designer should ask module vendor for specification of the contact configuration in reset state.

Pulling RESET_IN# low is typically generated by a voltage monitor / Supervisor IC on the Carrier assuming that further operation of the system is not safe. See Figure 51 for an example. This shows a Supervisor IC with internal delay, which is necessary to prevent short reset pulses on RESET_IN# or repeated reset cycles.

Note: Not all failure cases on the Carrier Board can be handled by pulling RESET_IN# low. If an overcurrent situation on the Carrier Board occurs independently of module function the failure state will not be interrupted by the reset state. Carrier designer may should switch of the main voltage regulator for module power which also will result in a shutdown of Carrier Board voltages by CARRIER_PWR_EN.

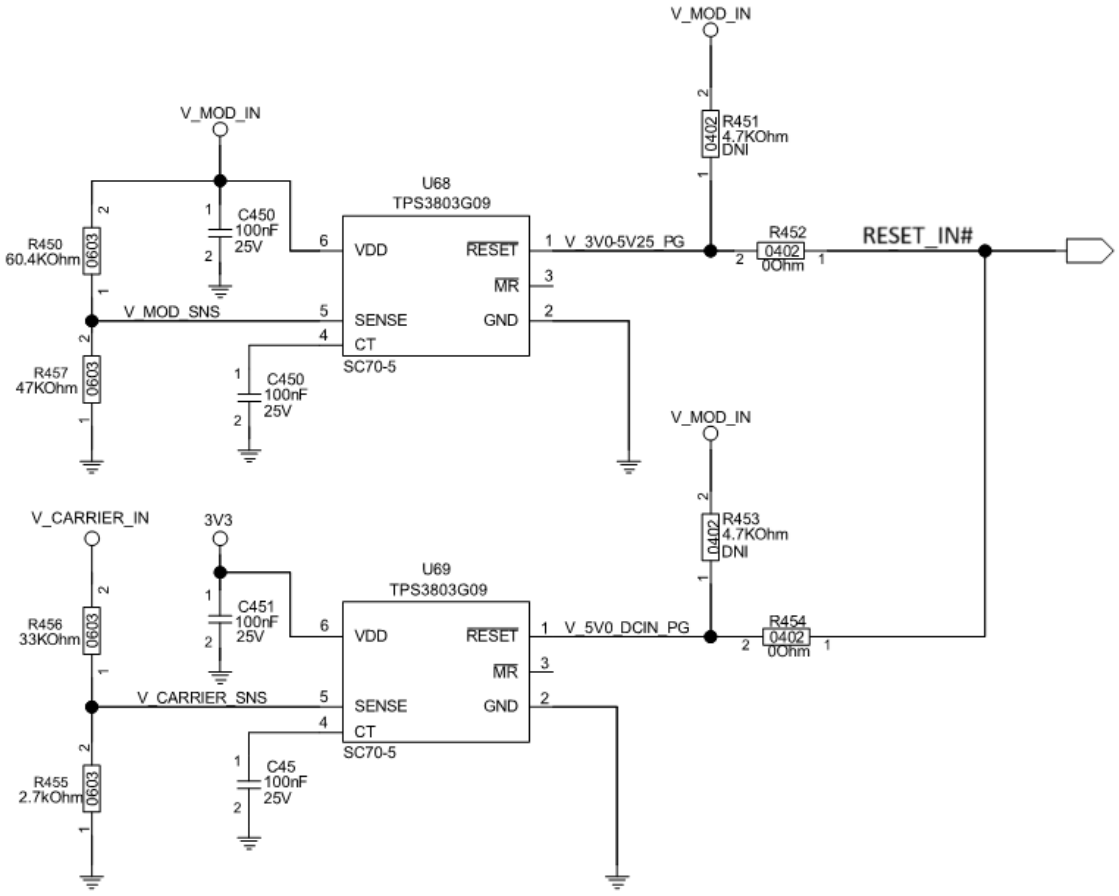


Figure 51 Voltage monitor with Supervisor and Delay

Note: There is no pull-up placed on RESET_IN# as the module has a pull-up to internal 1.8 V.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

9.6 Power Over Ethernet

This part will be released in future revision of this documentation.

9.7 Li-ION Battery Charger

This part will be released in future revision of this documentation.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

10 THERMAL MANAGEMENT

This part will be released in future revision of this documentation.

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

11 CARRIER PCB DESIGN RULE SUMMARY

11.1 Decoupling for power contacts

The OSM module already implements the most critical components of the power supply. Independently of this, coupling capacitors and bulk capacitors are usually required on the mainboard.

Each VCC_5V_IN and/or VCC_3V3_IN power contact used, generally requires additional capacitors. The quantity and capacity values must be determined based on the manufacturer's specifications and depend on the type of SOC used, the module size, the memory size and other performance parameters.

The following schematic shows an example of power decoupling for a Size-S module. Use the values given in the example as starting values for the design.

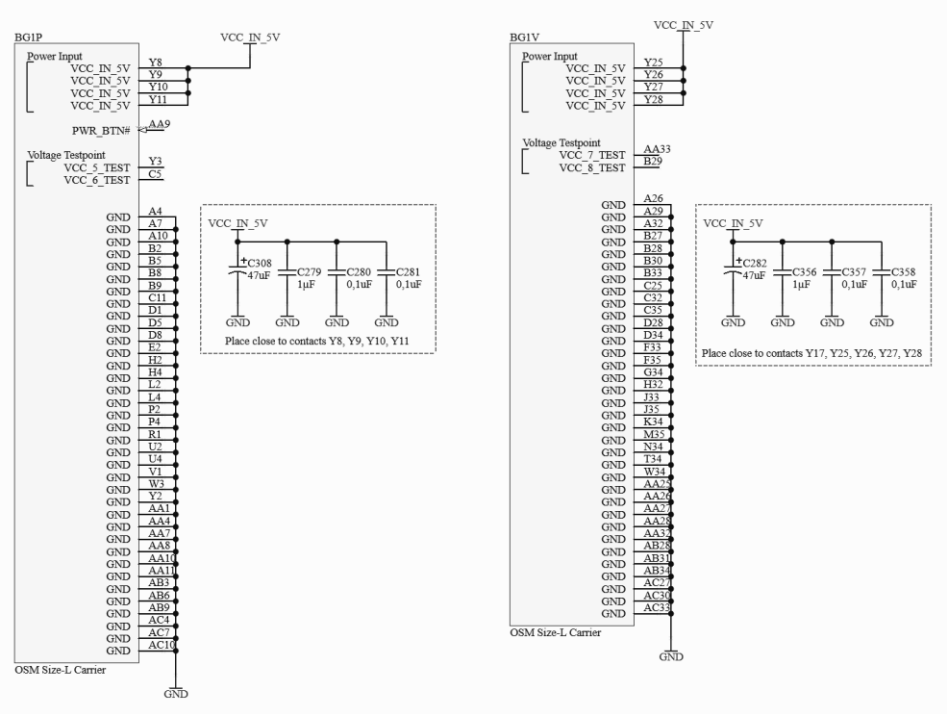


Figure 52 Power decoupling

Note: Ask the module vendor for recommendations of power decoupling and placement recommendations.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000