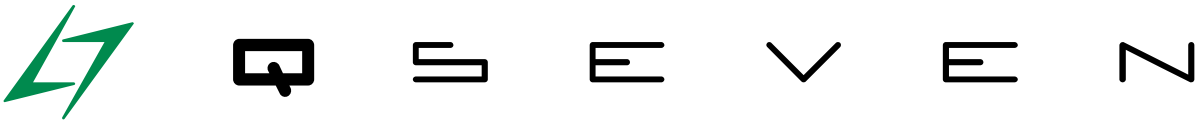
Qseven® Design Guide

Guidelines for designing Qseven® carrier boards



Version 2.0 of March 5, 2015



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Revision History

Revision	Date (dd.mm.yy)	Author	Revision History
0.1	02.02.09	Qseven® Consortium	Initial Draft
0.2	16.02.09	Qseven® Consortium	Updates throughout document.
0.3	19.02.09	Qseven® Consortium	English proofreading.
0.4	26.06.09	Qseven® Consortium	Added changes requested by the consortium members and updated schematics (SP30E90001_VC3)
0.5	09.07.09	Qseven® Consortium	Added PCB footprint of Qseven® module and MXM connector
0.6	04.08.09	Qseven® Consortium	Added changes requested by the consortium members
0.7	21.08.09	Qseven® Consortium	Created release candidate.
0.8	16.09.09	Qseven® Consortium	Updated to current schematics (SP31E90001). Changed component height value for carrier board components located under Qseven® module. Added Figure 2-1.
0.9		Qseven® Consortium	Changed naming convention of pin 91 from USB_HOST_PRES# to USB_CC, pin 92 from USB_HC_SEL to USB_ID in order to be compliant with OTG specification. Changed name USB_HOST_PRES# to USB_CC, USB_HC_SEL to USB_ID and changed the signal descriptions in Fehler: Referenz nicht gefunden for these signals. Updated signal names in pinout table Fehler: Referenz nicht gefunden. Updated signal descriptions in section “3.1 Signal Descriptions.” Added section USB Client Considerations and Fehler: Referenz nicht gefunden. Changed values in LAN Trace Routing Guidelines Fehler: Referenz nicht gefunden. Changed the values for Trace width (W) and Spacing between differential pairs (intra-pair) (S) in Fehler: Referenz nicht gefunden,Fehler: Referenz nicht gefunden, Fehler: Referenz nicht gefunden,Fehler: Referenz nicht gefunden and Fehler: Referenz nicht gefunden.
1.0	18.04.11	Qseven® Consortium	Updated SDIO example schematics Fehler: Referenz nicht gefunden. Added CAN section Fehler: Referenz nicht gefunden and SPI section 3.16 . Updated SDVO Trace Routing Guidelines Fehler: Referenz nicht gefunden. Added USB Client section 3.7.2.3 . Added note regarding GP I2C bus. Added indication regarding power protection. Updated level shifter in figure Fehler: Referenz nicht gefunden.
1.0 SGeT	2013-05-04	SGeT e.V.	Added SGeT Copyright page. Updated disclaimers and header/footer layout following SGeT Guidelines. Changed Links to www.sget.org . Updated copyright Notice and Trademarks
1.2 alpha	2013-09-09	SGeT e.V	Full rework – Updated everything to Rev 1.2 including Schematics to current 1.2 Reference Board
1.2	2014-02-09	SGeT e.V	Reworked graphics figures to reduce pdf size and enhance readability – no changes in text or graphics content
2.0 r.c.	2015-02-24	SGeT e.V	Introduced new Chapter structure Rework for 2.0: Changed contents and adapted Schematics to match the new 2.0 Reference Board. 2.7 mm height between Qseven Module and carrier board no longer specified with 2.0; only 5.0 mm is permitted. Added PCIe lane multiplexer. Replaced Express Card with UART as defined in Specification V. 2.0

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Revision	Date (dd.mm.yy)	Author	Revision History
			Added USB3.0 SuperSpeed Removed SVDO Graphics chapter. Added eDP Graphics chapter. Updated connector pinning following Errandum to Spcification. Updated connector signals to new TMDS/DP scheme. Updated Layout rules sections. Final cleanup: Request for Release
2.0	2015-03-05	SGET e.V.	Last cleanup and Release

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Preface Qseven Consortium

This document provides information for designing a custom system carrier board for Qseven® modules. This document includes reference schematics for the external circuitry required to implement the various Qseven® peripheral functions. It also explains how to extend the supported buses and how to add additional peripherals and expansion slots to a Qseven® based system.

This design guide is not a specification. It contains additional detail information but does not replace the Qseven® specification. It's strongly recommended to use the latest Qseven® specification and the module vendor's product manuals as reference material.

Disclaimer

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The typical application circuits described in this document may not be suitable for all applications. In particular, additional components may need to be added to these circuits in order to meet specific ESD, EMC or safety isolation requirements. Such regulatory requirements and the techniques for meeting them vary by industry and are beyond the scope of this document.

Intended Audience

This Qseven® Design Guide is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols may be used in this specification:



Warning

Warnings indicate conditions that, if not observed, can cause personal injury.



Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.



Note

Notes call attention to important information that should be observed.

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Lead-Free Designs (RoHS)

All Qseven® designs shall be created from lead-free components in order to be RoHS compliant.

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Electrostatic Sensitive Device



All electronic parts described in this design guide are electrostatic sensitive devices and are packaged accordingly. Do not open or handle a carrier board or module except at an electrostatic-free workstation. Additionally, do not ship or store electronic devices near strong electrostatic, electromagnetic, magnetic, or radioactive fields unless the device is contained within its original manufacturer's packaging.

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Key Words

- ***May*** - Indicates flexibility of choice with no implied recommendation or requirement.
- ***Shall*** - Indicates a mandatory requirement. Designers shall implement such mandatory requirements to ensure interchangeability and to claim conformance with the specification.
- ***Should*** - Indicates a strong recommendation but not a mandatory requirement. Designers should give strong consideration to such recommendations but there is still a choice in implementation.

Qseven® Concept

The Qseven® concept is an off-the-shelf, multi vendor, Single-Board-Computer (SBC) that integrates all the core components of a typical PC and is mounted onto an application specific carrier board. Qseven® modules have a standardized form factor of 70mm x 70mm (Qseven) or 70mmm x 40mm (µQseven) and have specified pinouts based on the high speed MXM 2 system connector which are standardized regardless of the vendor. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, audio, mass storage, network and multiple USB ports. A single ruggedized MXM 2 connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a densely packed solution, which results in a more reliable product while simplifying system integration. Most importantly, Qseven® applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another, no redesign is necessary.

Qseven® offers the newest I/O technologies on this minimum size form factors.

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Terminology

Term	Description
PCI Express (PCIe)	Peripheral Component Interface Express. Next-generation high speed serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4, x8, x16	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4, x8 and x16 link.
DDC	Display Data Channel is an I²C bus interface between a display and a graphics adapter.
DVI	Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG).
MXM	Mobile PCI Express Module a standard for mobile modular graphics cards avaiable in different revisions. Revision 2 is used for Qseven.
GBE	Gigabit Ethernet
USB	Universal Serial Bus
OTG	On The Go – USB extension for automated switching between USB host and client mode.
SATA	Serial AT Attachment: serial interface standard for hard disks.
HDA	High Definition Audio
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.
SDIO	Secure Digital Input Output
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface defined by Silicon Image that is used for DVI and HDMI.
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
SMB	System Management Bus
LVDS	Low-Voltage Differential Signaling
ACPI	Advanced Control Programmable Interface
RoHS	Restriction on Hazardous Substances: The Directive on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment 2002/95/EC.
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

Schematics Naming Conventions

Voltage Reference	Description
VCC12V	12 volt input power rail.
VCC5V	5 volt input power rail.
VCC3V3	3.3 volt input power rail.
VCC5V_A	5 volt input power rail during standby.
VCC3V3_A	3.3 volt input power rail during standby.
VCC3_RTC	+2.0V to +3.3V CMOS battery power

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1 Customer Feedback

The Qseven® Design Guide has been created to help customers design Qseven® compliant carrier boards. It should be used in conjunction with the Qseven® Specification as well as any other relevant information with regards to the implementation of the interfaces mentioned within this document.

The guidelines set forth in this document have been carefully thought out by engineers of the SGeT e.V. and are considered to be the most important factors when designing a Qseven® carrier board. The SGeT e.V. is committed to helping customers who are designing Qseven® compliant carrier boards by sharing our expertise and providing the best possible support and documentation. Therefore, we welcome any suggestions our valued customers may have with regards to additional information that should be included in this Qseven® Design Guide. Additionally, we encourage any feedback about the contents of this document with regards to clarity and understanding.

If you have any suggestions about additional content, or any questions about the existing content, please contact the SGeT e.V. via email at info@sget.org.

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2 Qseven® Specification Overview

2.1 Qseven® Feature Overview

The Qseven® V2.0 Specification defines mandatory and optional features for both supported platform architectures.
Table 2-1 shows the minimum and maximum required configuration of the feature set.

Table 2-1 Qseven® Supported Features

System I/O Interface	ARM/RISC Based Minimum Configuration	X86 Based Minimum Configuration	Maximum Configuration
PCI Express lanes	0	1 (x1 link)	4
Serial ATA channels	0	0	2
USB 2.0 ports	3	4	8
USB 3.0 ports	0	0	2
USB OTG	0	0	1
LVDS channels embedded DisplayPort	0 0	0 0	Dual Channel 24bit 2
DisplayPort, TMDS	0	0	1
High Definition Audio / AC'97 / I2S	0	0	1
Ethernet 10/100 Mbit/Gigabit	0	0	1 (Gigabit Ethernet)
UART	0	0	1
Low Pin Count bus	0	0	1
Secure Digital I/O 8-bit for SD/MMC cards	0	0	1
System Management Bus	0	1	1
I²C Bus	1	1	1
SPI Bus	0	0	1
CAN Bus	0	0	1
Watchdog Trigger	1	1	1
Power Button	1	1	1
Power Good	1	1	1
Reset Button	1	1	1
LID Button	0	0	1
Sleep Button	0	0	1
Suspend To RAM (S3 mode)	0	0	1
Wake	0	0	1
Battery low alarm	0	0	1
Thermal control	0	0	1
FAN control	0	0	1

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2.2 Qseven® Mechanical Characteristics

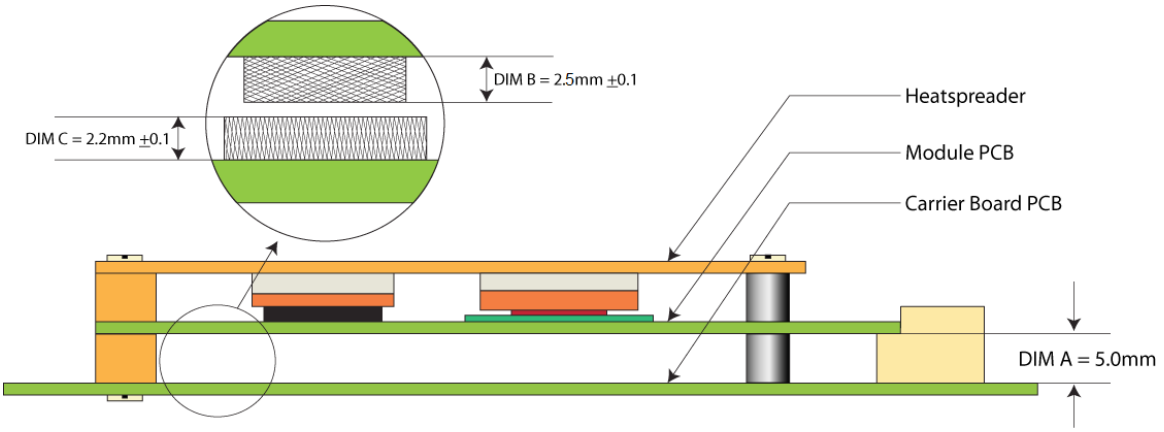
The Qseven® module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12mm thick.

Edge-fingers on the module are referenced to the PCB slot center with an overall PCB thickness of 1.2mm ±0.1mm measured across the fingers including the plating and/or metalization on both sides. A bevel is optional but the edge shall be free of burrs and shall not have sharp edges.

The components located on the top side of the module are up to 5.5mm high. Components mounted on the backside of the Qseven® module (in the space between the bottom surface of the module PCB and the top surface of the carrier board PCB) shall have a height of 2.5mm ±0.1 (dimension 'B' in Figure 2-1).

Carrier board component placement below the Qseven® module is only permitted when using a MXM 2 connector with a resulting height between carrier board and Qseven® module of 5.0mm (dimension 'A' in Figure 2-1) and no carrier board component shall exceed a height of 2.2mm ±0.1 (dimension 'C' in Figure 2-1). Using carrier board topside components up to 2.2mm allows a gap of 0.3mm between carrier board topside components and the Qseven® module bottom side components. This may not be sufficient in some situations. In carrier board applications in which vibration or board flex is a concern, then the carrier board component height should be restricted to a value less than 2.2mm that yields a clearance that is sufficient for the application. Refer to Table 2-2 regarding MXM 2 connector specifications.

Figure 2-1 Bottom Side Qseven® Module and Carrier Board Component Heights



All measurements are in millimeters

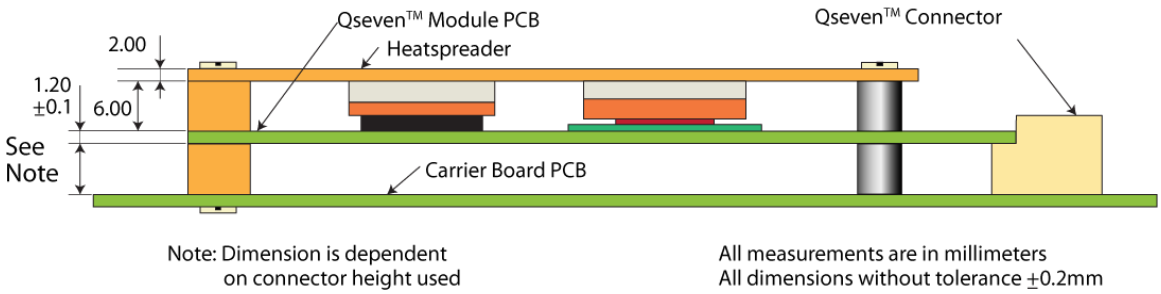
The heatspreader offered for Qseven® modules acts as a thermal coupling device and is not a heat sink. Heat dissipation devices such as a heat sink with fan or heat pipe may need to be connected to the heatspreader. The dissipation of heat will vary between different CPU boards. Refer to the Qseven® module's user's guide for heatspreader dimensions and specifications.

The standoffs for the heatspreader and carrier board must not exceed 5.6mm overall external diameter. This ensures that the standoff contact area does not exceed the defined mounting hole footprint on the Qseven® module. The screw that is to be used for mounting must be a metric thread M2.5 DIN7985 / ISO7045.

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Qseven® modules are defined to feature ultra low power CPU and chipset solutions with an ultra low “Thermal Design Power” (TDP). Furthermore, the modules power consumption should not exceed 12W.

Figure 2-2 Overall Height including Heatspreader of the Qseven® Module



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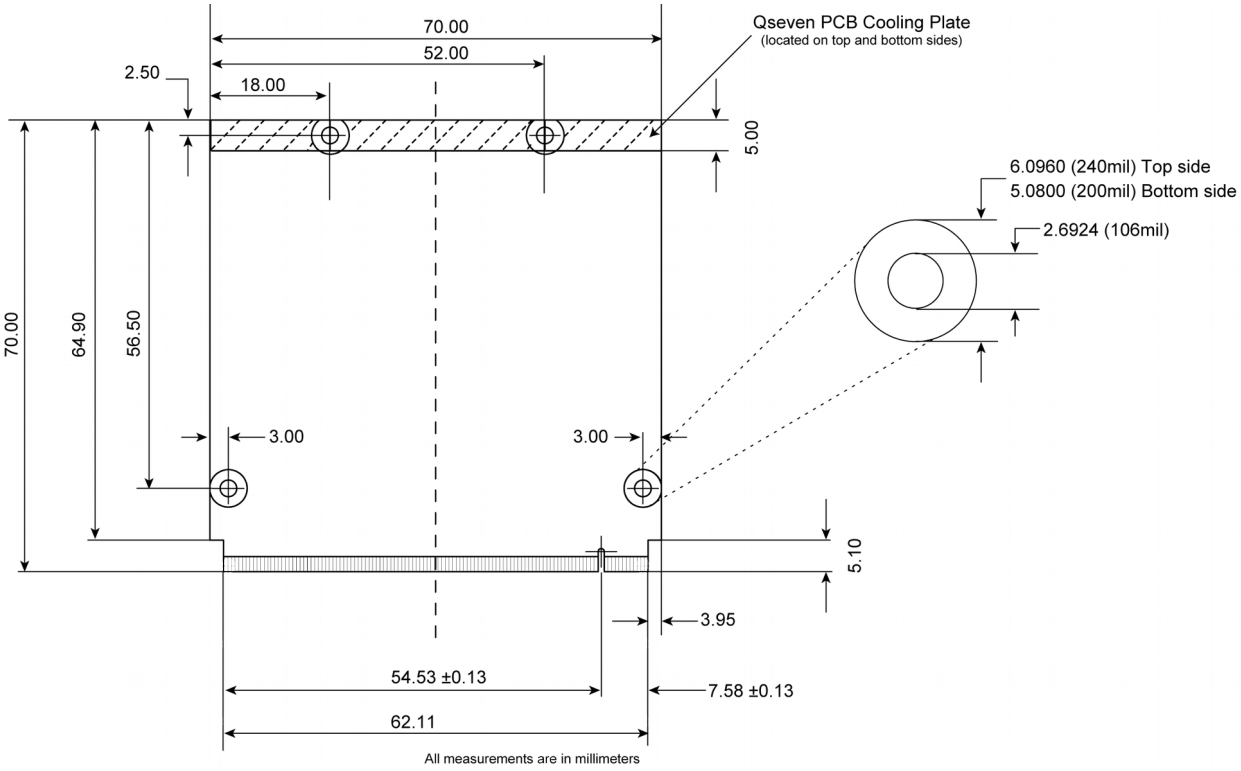
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2.3 Mechanical Dimensions

2.3.1 Module Outlines

2.3.1.1 Qseven® Module Outlines

Figure 2-3 Mechanical Dimensions of the Qseven® Module



Qseven Module Top Side

The Qseven® PCB cooling plate shown in Figure 2-3 is to be used as a cooling interface between the Qseven® module and the application specific cooling solution.

Note

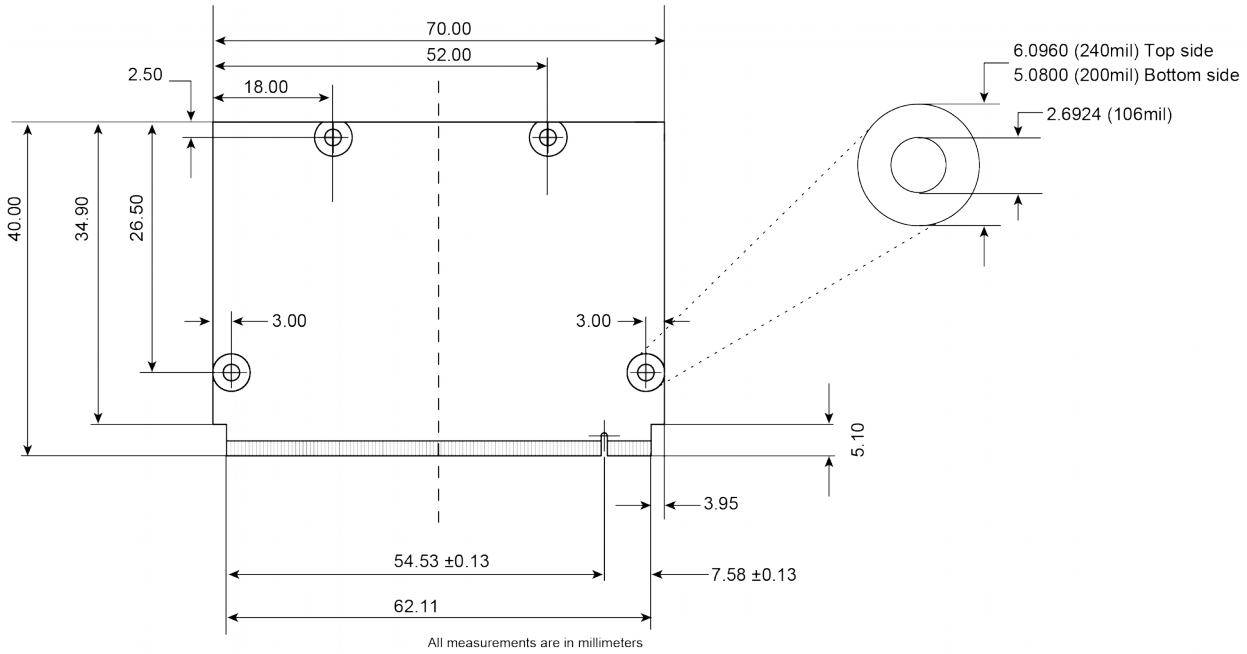
The Qseven® PCB cooling plate should be connected directly to the GND plane of the carrier board to ensure that the heat from the module can be properly dissipated.

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2.3.1.2 µQseven Module Outlines

Figure 2-4 Mechanical Dimensions of the µQseven Module



Qseven Module Top Side

Note

If one carrier board design is used for both µQseven and Qseven®, the standoffs of the smaller µQseven module will collide with the Qseven® module. To support both outlines, these standoffs of the µQseven module should be removed when full sized Qseven® modules are used.

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2.3.2 MXM Connector

The Qseven® carrier board utilizes a 230-pin card-edge connector to connect the Qseven® module. Originally, this card-edge connector was designed for MXM graphics modules that are used for PCI Express capable notebook graphics cards. The card-edge connector is following the MXM specification and therefore this connector type is also known as a MXM connector.

The MXM edge connector is the result of an extensive collaborative design effort with the industry's leading notebook manufacturers. This collaboration has produced a robust, low-cost edge connector that is capable of handling high-speed serialized signals.

The MXM connector accommodates various connector heights for different carrier board applications needs.

Table 2-2 MXM Connector

Manufacturer	Part Number	Specification	Resulting height between carrier board and Qseven® module	Overall height of the MXM Connector	Remarks
Foxconn	AS0B32x-S78N-xH	AS0B32x-S78N-xH	5.0mm	7.8mm	7.8mm oh
Aces	88882-2Dxx	88882-2Dxx	5.0mm	7.5mm	7.5mm oh
Nexus	5240HB75R	5240HB75R	5.0mm	7.5mm	7.5mm oh
Yamaichi	BEC05230S9xFREDC	BEC05230S9xFREDC	5.0mm	7.8mm	7.8mm oh

Note

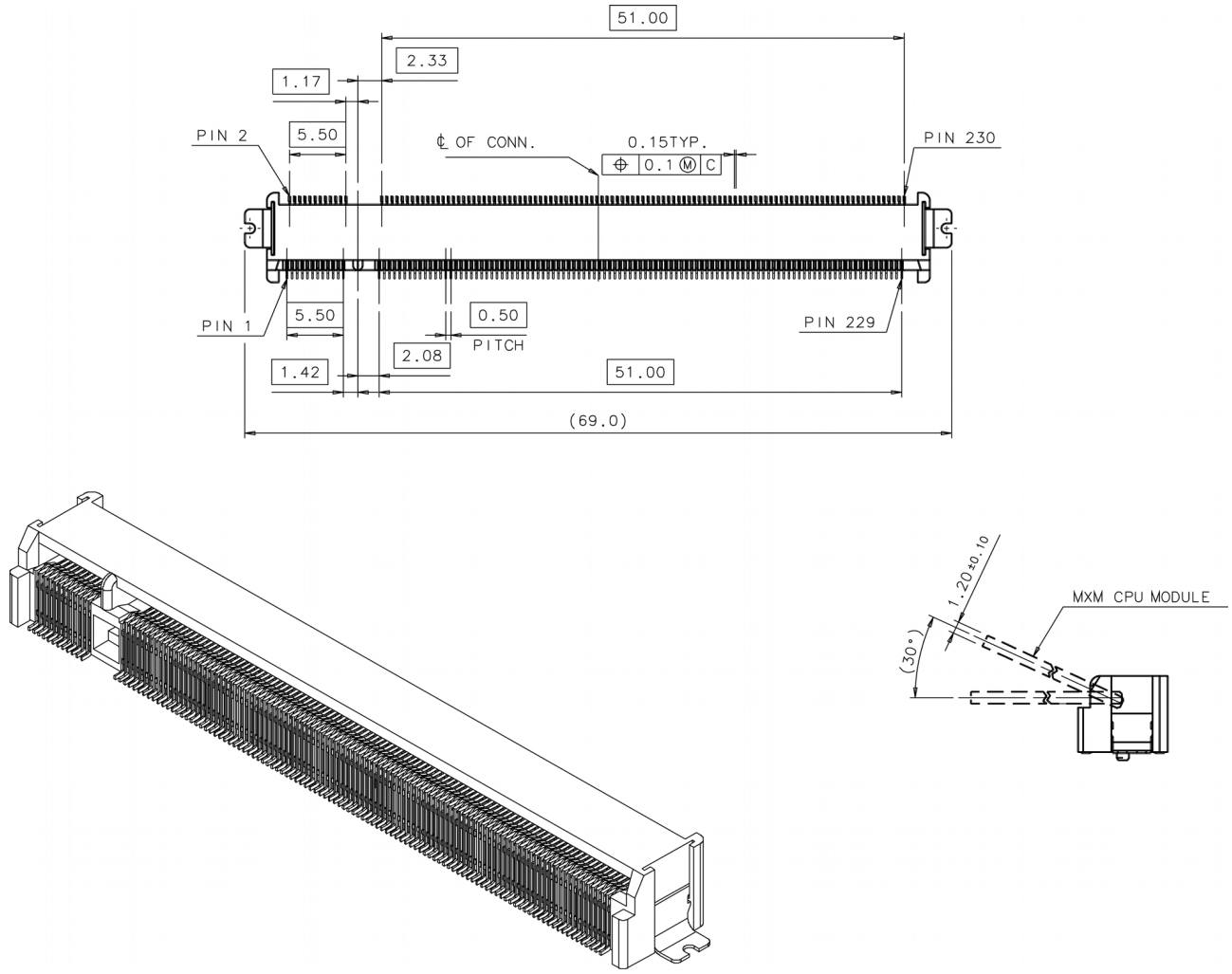
The connectors mentioned in Table 2-1 are only a partial list of what is offered by the manufacturers. For more information about additional variants contact the manufacturer and observe potential footprint changes.

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2.3.2.1 MXM 2 Connector Dimensions

Figure 2-5 MXM 2 Connector



All measurements are in millimeters.

Note:

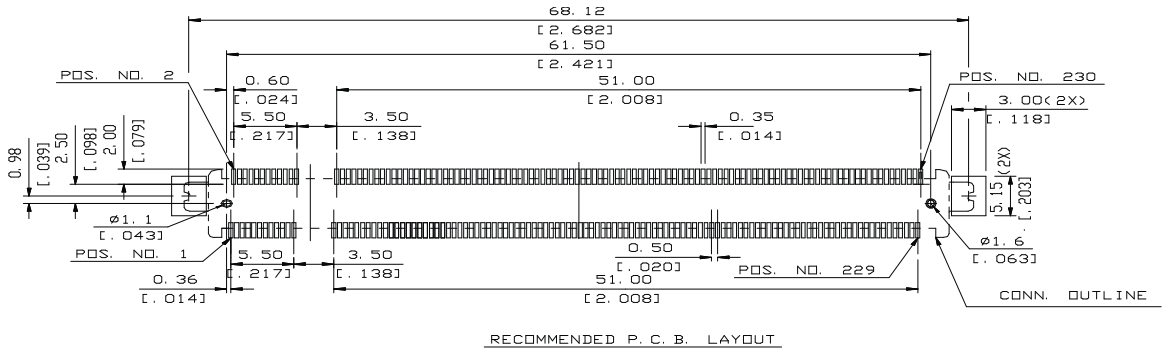
Dimensions will vary according to the vendors solutions.

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2.3.2.2 MXM 2 Connector Footprint

Figure 2-6 Carrier Board PCB Footprint for the MXM Connector



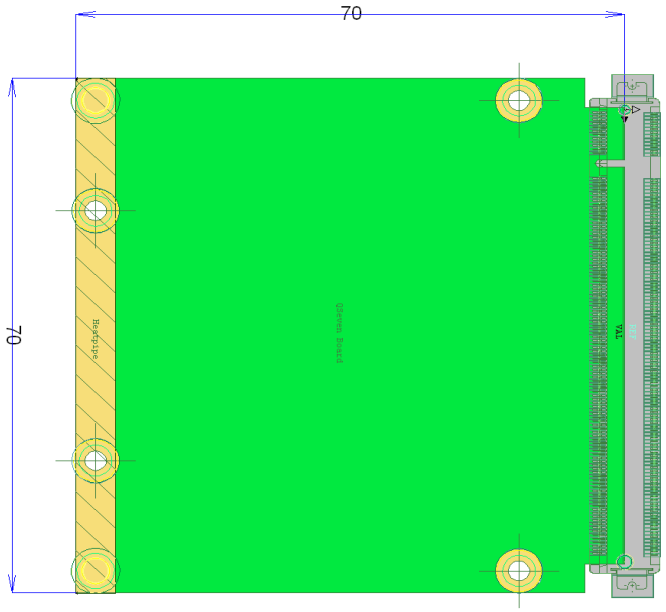
All measurements are in millimeters and mils (in brackets).

Note

Please verify the footprint of the selected connector.

2.3.2.3 Qseven® Module and MXM Connector PCB Footprint

Figure 2-7 PCB footprint for the Qseven® Module inserted in the MXM carrier board connector



All measurements are in millimeters

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3 Carrier Board Design compliant to Qseven Specification 2.0

With the introduction of USB 3.0 in Version 2.0 of the Qseven Standard there are a lot of different configurations possible. There may be up to two USB 3.0 ports present and/or alternatively up to 8 USB 2.0 ports, each of them either to be placed on module or carrier board. Also various graphics configurations and two different processor technology platforms are supported.

This design guide is not intended to handle all details of all possible configurations. It shows proven examples which have been implemented and tested with the Qseven V2.0 Reference Carrier Board designed and manufactured by SECO. This is one of many possible configurations supporting a variety of options for both technology platforms. Schematic examples in this Design Guide refer to the implementation of this Reference Carrier Board unless otherwise stated.

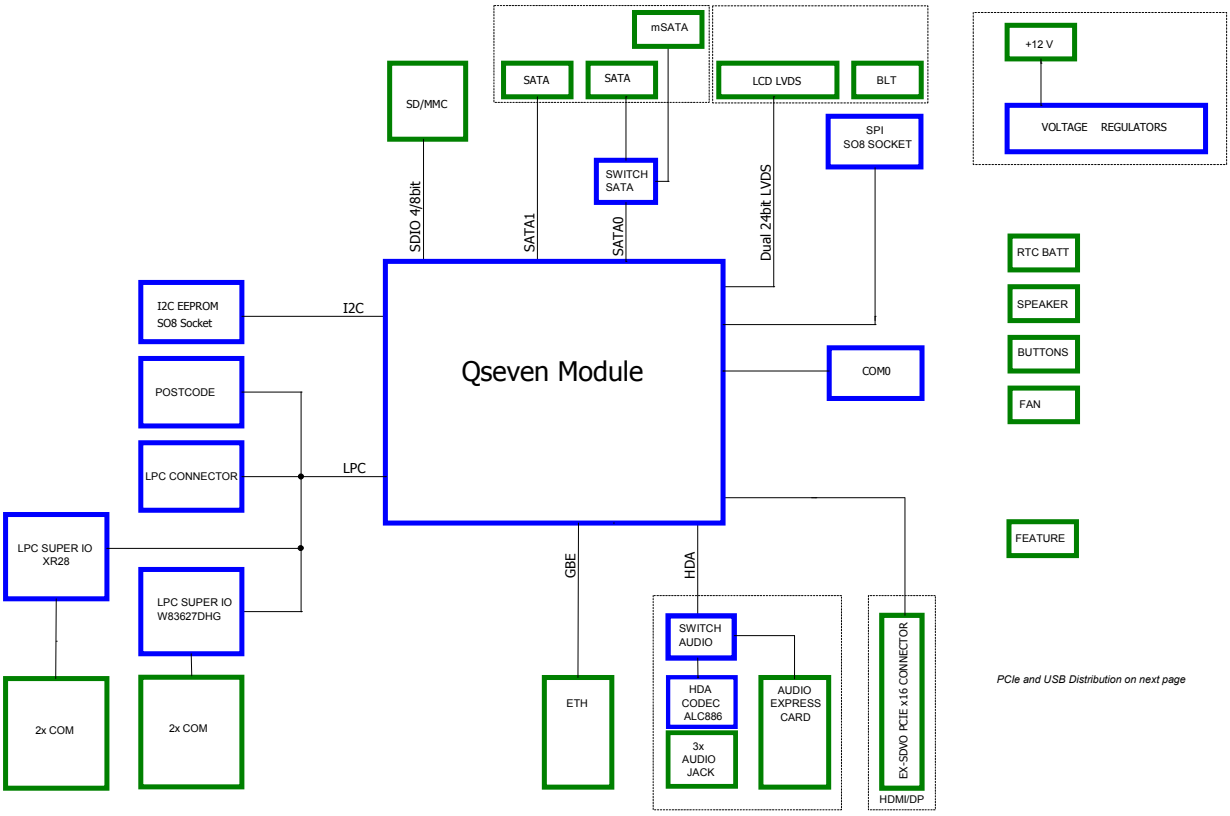
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3.1 Concept Overview

The concept of the Qseven V2.0 Reference Carrier Board is laid out in Figure 3-1, 'Figure 3-2 shows the details of the USB and PCI express signal distributions. .A mini PCI express card interface is supported as well as various USB2.0/3.0 configurations. Switches and multiplexers allow the configuration to adapt the Qseven V2.0 Reference Carrier Board to work with the provided interfaces on the respective modules.

Figure 3-1 Qseven V2.0 Reference Carrier Board overview

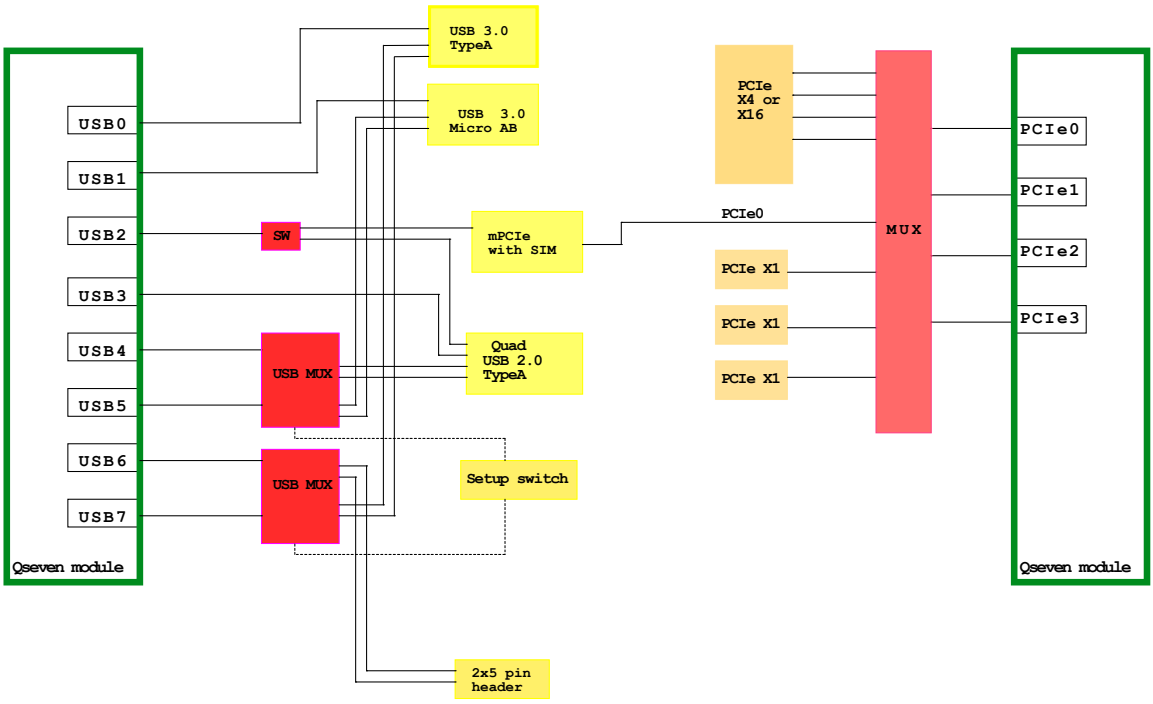


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Figure 3-2 USB and PCI express distributions

as implemented on the Qseven V2.0 Reference Carrier Board (with multiplexers).



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3.2 Connector Pin Assignments

There are 115 edge fingers on the top and bottom side of the Qseven® module that mate with the MXM connector. Table 3-1 lists the pin assignments for all 230 edge fingers.

Table 3-1 Connector Pinout Description

Pin	Signal	Modul Pin direction	Pin	Signal	Modul Pin direction
1	GND	Power	2	GND	Power
3	GBE_MDI3-	High-Speed I/O	4	GBE_MDI2-	High-Speed I/O
5	GBE_MDI3+	High-Speed I/O	6	GBE_MDI2+	High-Speed I/O
7	GBE_LINK100#	Output	8	GBE_LINK1000#	Output
9	GBE_MDI1-	High-Speed I/O	10	GBE_MDI0-	High-Speed I/O
11	GBE_MDI1+	High-Speed I/O	12	GBE_MDI0+	High-Speed I/O
13	GBE_LINK#	Output	14	GBE_ACT#	Output
15	GBE_CTREF	Output (Analog)	16	SUS_S5#	Output
17	WAKE#	Input	18	SUS_S3#	Output
19	SUS_STAT#	Output	20	PWRBTN#	Input
21	SLP_BTN#	Input	22	LID_BTN#	Input
23	GND	Power	24	GND	Power
	KEY			KEY	
25	GND	Power	26	PWGIN	Input (5V)
27	BATLOW#	Input	28	RSTBTN#	Input
29	SATA0_TX+	High-Speed Output	30	SATA1_TX+	High-Speed Output
31	SATA0_TX-	High-Speed Output	32	SATA1_TX-	High-Speed Output
33	SATA_ACT#	Open Drain	34	GND	Power
35	SATA0_RX+	High-Speed Input	36	SATA1_RX+	High-Speed Input
37	SATA0_RX-	High-Speed Input	38	SATA1_RX-	High-Speed Input
39	GND	Power	40	GND	Power
41	BIOS_DISABLE# / BOOT_ALT#	Input	42	SDIO_CLK#	Output
43	SDIO_CD#	Input/Output	44	SDIO_LED	Output
45	SDIO_CMD	Input/Output	46	SDIO_WP	Input
47	SDIO_PWR#	Output	48	SDIO_DAT1	Input/Output
49	SDIO_DAT0	Input/Output	50	SDIO_DAT3	Input/Output
51	SDIO_DAT2	Input/Output	52	SDIO_DAT5	Input/Output
53	SDIO_DAT4	Input/Output	54	SDIO_DAT7	Input/Output
55	SDIO_DAT6	Input/Output	56	USB_DRIVE_VBUS	Output
57	GND	Power	58	GND	Power
59	HDA_SYNC / AC97_SYNC / I2S_WS	Output	60	SMB_CLK / GP1_I2C_CLK	Open Drain Output
61	HDA_RST# / AC97_RST# / I2S_RST#	Output	62	SMB_DAT / GP1_I2C_DAT	Open Drain Input/Output

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Pin	Signal	Modul Pin direction	Pin	Signal	Modul Pin direction
63	HDA_BCLK / AC97_BCLK / I2S_CLK	Output	64	SMB_ALERT#	Input
65	HDA_SDI / AC97_SDI / I2S_SDI	Input	66	GP0_I2C_CLK	Open Drain Output
67	HDA_SDO / AC97_SDO / I2S_SDO	Output	68	GP0_I2C_DAT	Open Drain Input/Output
69	THRM#	Input	70	WDTRIG#	Input
71	THRMTRIP#	Output	72	WDOUT	Output
73	GND	Power	74	GND	Power
75	USB_P7- / USB_SSTX0-	High-Speed I/O	76	USB_P6- / USB_SSRX0-	High-Speed I/O
77	USB_P7+ / USB_SSTX0+	High-Speed I/O	78	USB_P6+ / USB_SSRX0+	High-Speed I/O
79	USB_6_7_OC#	Input	80	USB_4_5_OC#	Input
81	USB_P5- / USB_SSTX1-	High-Speed I/O	82	USB_P4- / USB_SSRX1-	High-Speed I/O
83	USB_P5+ / USB_SSTX1+	High-Speed I/O	84	USB_P4+ / USB_SSRX1+	High-Speed I/O
85	USB_2_3_OC#	Input	86	USB_0_1_OC#	Input
87	USB_P3-	High-Speed I/O	88	USB_P2-	High-Speed I/O
89	USB_P3+	High-Speed I/O	90	USB_P2+	High-Speed I/O
91	USB_VBUS	Input (5V)	92	USB_ID	Input
93	USB_P1-	High-Speed I/O	94	USB_P0-	High-Speed I/O
95	USB_P1+	High-Speed I/O	96	USB_P0+	High-Speed I/O
97	GND	Power	98	GND	Power
99	eDP0_TX0+ / LVDS_A0+	High-Speed Output	100	eDP1_TX0+ / LVDS_B0+	High-Speed Output
101	eDP0_TX0- / LVDS_A0-	High-Speed Output	102	eDP1_TX0- / LVDS_B0-	High-Speed Output
103	eDP0_TX1+ / LVDS_A1+	High-Speed Output	104	eDP1_TX1+ / LVDS_B1+	High-Speed Output
105	eDP0_TX1- / LVDS_A1-	High-Speed Output	106	eDP1_TX1- / LVDS_B1-	High-Speed Output
107	eDP0_TX2+ / LVDS_A2+	High-Speed Output	108	eDP1_TX2+ / LVDS_B2+	High-Speed Output
109	eDP0_TX2- / LVDS_A2-	High-Speed Output	110	eDP1_TX2- / LVDS_B2-	High-Speed Output
111	LVDS_PPEN	Output	112	LVDS_BLEN	Output
113	eDP0_TX3+ / LVDS_A3+	High-Speed Output	114	eDP1_TX3+ / LVDS_B3+	High-Speed Output
115	eDP0_TX3- / LVDS_A3-	High-Speed Output	116	eDP1_TX3- / LVDS_B3-	High-Speed Output
117	GND	Power	118	GND	Power
119	eDP0_AUX+ / LVDS_A_CLK+	High-Speed I/O	120	eDP1_AUX+ / LVDS_B_CLK+	High-Speed I/O
121	eDP0_AUX- / LVDS_A_CLK-	High-Speed I/O	122	eDP1_AUX- / LVDS_B_CLK-	High-Speed I/O

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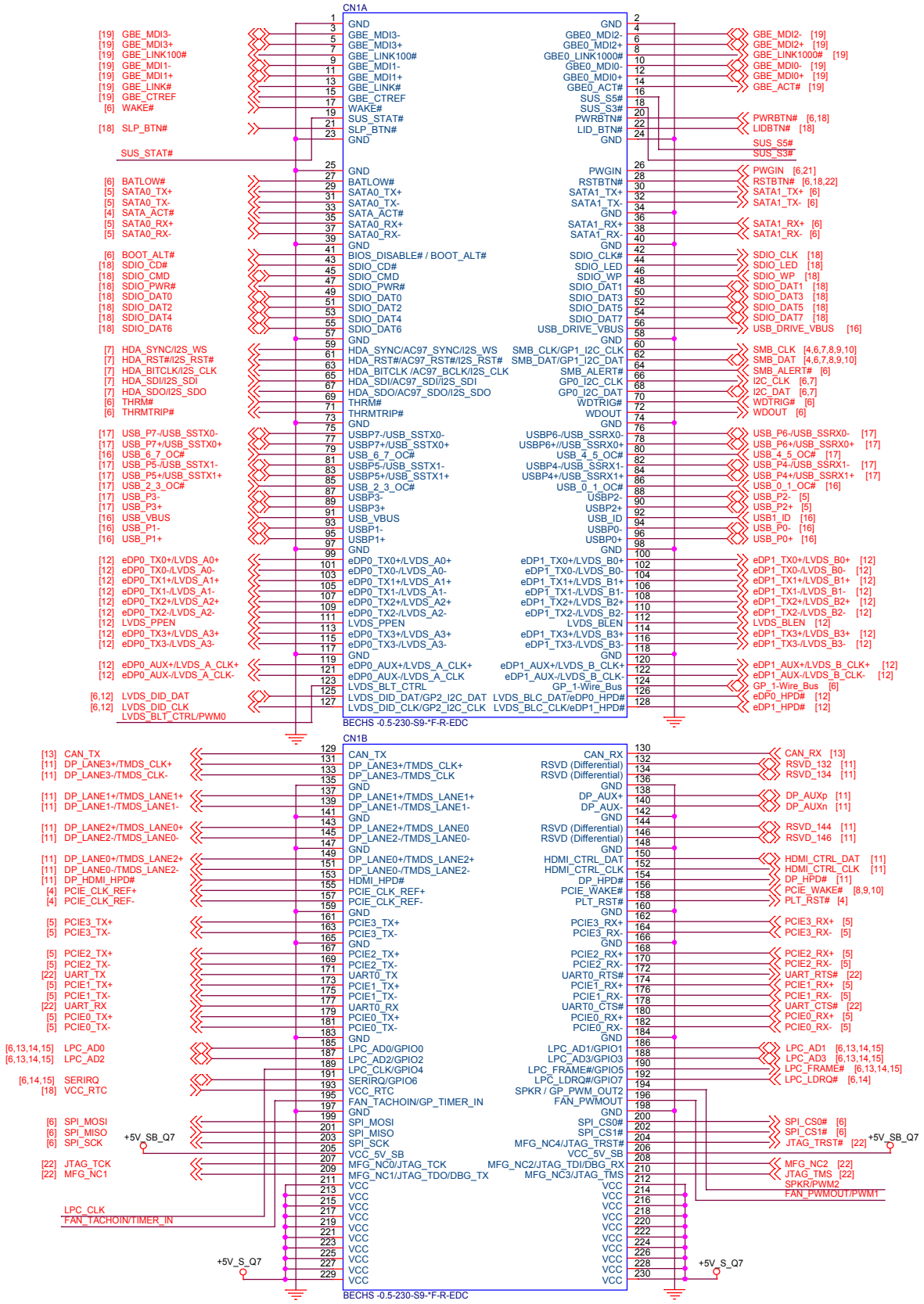
Pin	Signal	Modul Pin direction	Pin	Signal	Modul Pin direction
123	LVDS_BLT_CTRL /GP_PWM_OUT0	Output	124	GP_1-Wire_Bus	Input/Output
125	GP2_I2C_DAT / LVDS_DID_DAT	Open Drain Input/Output	126	eDP0_HPD# / LVDS_BLC_DAT	Open Drain Input/Output
127	GP2_I2C_CLK / LVDS_DID_CLK	Open Drain Output	128	eDP1_HPD# / LVDS_BLC_CLK	Open Drain Input/Output
129	CAN0_TX	Output	130	CAN0_RX	Input
131	DP_LANE3+ / TMDS_CLK+	High-Speed Output	132	RSVD (Differential Pair)	N.C.
133	DP_LANE3- / TMDS_CLK-	High-Speed Output	134	RSVD (Differential Pair)	N.C.
135	GND	Power	136	GND	Power
137	DP_LANE1+ / TMDS_LANE1+	High-Speed Output	138	DP_AUX+	High-Speed I/O
139	DP_LANE1- / TMDS_LANE1-	High-Speed Output	140	DP_AUX-	High-Speed I/O
141	GND	Power	142	GND	Power
143	DP_LANE2+ / TMDS_LANE0+	High-Speed Output	144	RSVD (Differential Pair)	N.C.
145	DP_LANE2- / TMDS_LANE0-	High-Speed Output	146	RSVD (Differential Pair)	N.C.
147	GND	Power	148	GND	Power
149	DP_LANE0+ / TMDS_LANE2+	High-Speed Output	150	HDMI_CTRL_DAT	Open Drain Input/Output
151	DP_LANE0- / TMDS_LANE2-	High-Speed Output	152	HDMI_CTRL_CLK	Open Drain Output
153	DP_HDMI_HPD#	Input	154	DP_HPD#	Input
155	PCIE_CLK_REF+	High-Speed Output	156	PCIE_WAKE#	Input
157	PCIE_CLK_REF-	High-Speed Output	158	PCIE_RST#	Output
159	GND	Power	160	GND	Power
161	PCIE3_TX+	High-Speed Output	162	PCIE3_RX+	High-Speed Input
163	PCIE3_TX-	High-Speed Output	164	PCIE3_RX-	High-Speed Input
165	GND	Power	166	GND	Power
167	PCIE2_TX+	High-Speed Output	168	PCIE2_RX+	High-Speed Input
169	PCIE2_TX-	High-Speed Output	170	PCIE2_RX-	High-Speed Input
171	UART0_TX	Output	172	UART0_RTS#	Output
173	PCIE1_TX+	High-Speed Output	174	PCIE1_RX+	High-Speed Input
175	PCIE1_TX-	High-Speed Output	176	PCIE1_RX-	High-Speed Input
177	UART0_RX	Input	178	UART0_CTS#	Input
179	PCIE0_TX+	High-Speed Output	180	PCIE0_RX+	High-Speed Input
181	PCIE0_TX-	High-Speed Output	182	PCIE0_RX-	High-Speed Input
183	GND	Power	184	GND	Power
185	LPC_AD0 / GPIO0	Input/Output	186	LPC_AD1 / GPIO1	Input/Output
187	LPC_AD2 / GPIO2	Input/Output	188	LPC_AD3 / GPIO3	Input/Output
189	LPC_CLK / GPIO4	Input/Output	190	LPC_FRAME# / GPIO5	Input/Output
191	SERIRQ / GPIO6	Input/Output	192	LPC_LDRQ# / GPIO7	Input/Output

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Pin	Signal	Modul Pin direction	Pin	Signal	Modul Pin direction
193	VCC_RTC	Power (3V)	194	SPKR / GP_PWM_OUT2	Output
195	FAN_TACHOIN /GP_TIMER_IN	Input	196	FAN_PWMOUT / GP_PWM_OUT1	Output
197	GND	Power	198	GND	Power
199	SPI_MOSI	Output	200	SPI_CS0#	Output
201	SPI_MISO	Input	202	SPI_CS1#	Output
203	SPI_SCK	Output	204	MFG_NC4	N.C.
205	VCC_5V_SB	Power (5V)	206	VCC_5V_SB	Power (5V)
207	MFG_NC0	N.C.	208	MFG_NC2	N.C.
209	MFG_NC1	N.C.	210	MFG_NC3	N.C.
211	VCC	Power (5V)	212	VCC	Power (5V)
213	VCC	Power (5V)	214	VCC	Power (5V)
215	VCC	Power (5V)	216	VCC	Power (5V)
217	VCC	Power (5V)	218	VCC	Power (5V)
219	VCC	Power (5V)	220	VCC	Power (5V)
221	VCC	Power (5V)	222	VCC	Power (5V)
223	VCC	Power (5V)	224	VCC	Power (5V)
225	VCC	Power (5V)	226	VCC	Power (5V)
227	VCC	Power (5V)	228	VCC	Power (5V)
229	VCC	Power (5V)	230	VCC	Power (5V)

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Figure 3-3 Qseven® Connector Schematics



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3.2.1 Signal Descriptions

The following section describes the signals on Qseven MXM connector that are provided over the edge-fingers of the Qseven® module. Refer to the Qseven Specification for more details.
The "#" symbol at the end of the signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level. Differential pairs are indicated by trailing '+' and '-' signs for the positive or negative signal.
All required pull-ups or pull-down resistors shall be implemented on the Qseven® module. This ensures that none of the signals that are not used will be left floating. Termination of all signals will be always on the module unless explicitly otherwise noted. Please note Figure 3-2 "PCI Express Termination default Configurations" in chapter 3.3.

The following terminology is used to describe the signals types in the I/O columns for the tables located below.

Table 3-2 Signal Tables Terminology Descriptions

Term	Description
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Module Input 3.3V tolerant
I 5V	Module Input 5V tolerant
I/O 3.3VSB	Bi-directional 3.3V tolerant active during suspend and running state.
I_{OL}	Module Output low current. The I_{OL} is the maximum output low current the module must be able to drive to an external circuitry.
I_{IL}	Module Input low current. The I_{IL} is the maximum input low current that must be provided to the Qseven® module via external circuitry in order to guarantee a proper logic low level of the signal.
O 3.3V	Module Output 3.3V signal level
O 5V	Module Output 5V signal level
OD	Module Open drain output
OC	Open collector
P	Power input/output
PP	Push Pull
PDS	Pull-down strap
REF	Module Reference voltage output. May be sourced from a module power plane.
DDC	Display Data Channel
PCIE	In compliance with PCI Express Base Specification, Revision 1.0a
USB	In compliance with the Universal Serial Bus Specification, Revision 2.0
GBE	In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet
SATA	In compliance with Serial ATA specification, Revision 1.0a
LVDS	Low-Voltage Differential Signaling differential pair signals. In compliance with the LVDS Owner's Manual 4.0.
TMDS	Transition Minimized Differential Signaling differential pair signals. In compliance with the Digital Visual Interface (DVI) Specification 1.0.
CMOS	Logic input or output.

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3.3 PCI Express

3.3.1 PCI Express Interface Signals

PCI Express provides a scalable, high-speed, serial I/O point-to-point bus connection. A PCI Express lane consists of dual simplex channels, each implemented as a low-voltage differentially driven transmit pair and receive pair. They are used for simultaneous transmission in each direction. The bandwidth of a PCI Express link can be scaled by adding signal pairs to form multiple lanes between two devices. The Qseven® modules can optionally provide configurations with x1 and x4 link widths. Each single lane has a raw data transfer rate of 2.5Gbps @ 1.25GHz.

The PCI Express interface of the Qseven® module consists of a minimum of 0 [ARM] resp. 1 [x86] and up to 4 lanes, each with a receive and transmit differential signal pair designated from PCIE0_RX (+ and -) to PCIE3_RX (+ and -) and correspondingly from PCIE0_TX (+ and -) to PCIE3_TX (+ and -). According to the PCI Express specification, these four lanes can be configured as several PCI Express x1 links or to a combined x4 link. These configuration possibilities are based on the Qseven® module's chipset capabilities. Refer to the vendor specific Qseven® module documentation for the module that you are using for additional information about this subject.

Table 3-3 Signal Definition PCI Express

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IIL}	I/O
PCIE0_RX+ PCIE0_RX-	180 182	PCI Express channel 0, Receive Input differential pair.	PCIE		I
PCIE0_TX+ PCIE0_TX-	179 181	PCI Express channel 0, Transmit Output differential pair.	PCIE		O
PCIE1_RX+ PCIE1_RX-	174 176	PCI Express channel 1, Receive Input differential pair.	PCIE		I
PCIE1_TX+ PCIE1_TX-	173 175	PCI Express channel 1, Transmit Output differential pair.	PCIE		O
PCIE2_RX+ PCIE2_RX-	168 170	PCI Express channel 2, Receive Input differential pair.	PCIE		I
PCIE2_TX+ PCIE2_TX-	167 169	PCI Express channel 2, Transmit Output differential pair.	PCIE		O
PCIE3_RX+ PCIE3_RX-	162 164	PCI Express channel 3, Receive Input differential pair.	PCIE		I
PCIE3_TX+ PCIE3_TX-	161 163	PCI Express channel 3, Transmit Output differential pair.	PCIE		O
PCIE_CLK_REF+ PCIE_CLK_REF-	155 157	PCI Express Reference Clock for Lanes 0 to 3.	PCIE		O
PCIE_WAKE#	156	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	CMOS 3.3V Suspend	≥ 5 mA	I
PCIE_RST#	158	Reset Signal for external devices.	CMOS 3.3V	max. 1 mA	O

Note

There are a maximum of 4 PCI Express TX and RX differential pairs supported on the Qseven® module standard. Depending on the features supported by the Qseven® module and the core logic chipset used, these lines may be used to form x1 or x4 PCI Express links. The documentation for the Qseven® module shall clearly identify, which PCI Express link configuration or configurations (in the case that these can be programmed in the core logic chipset) are supported.

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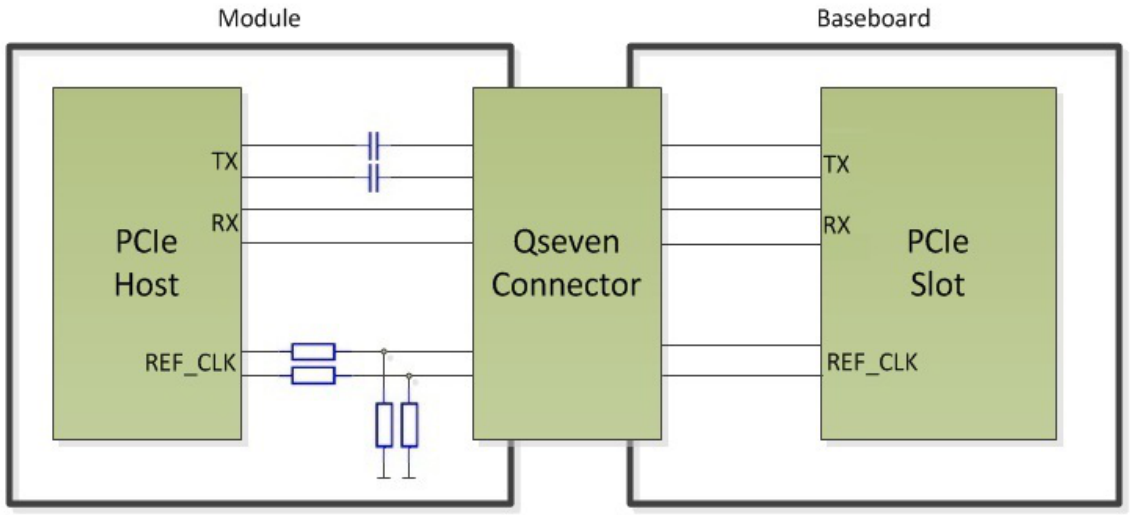
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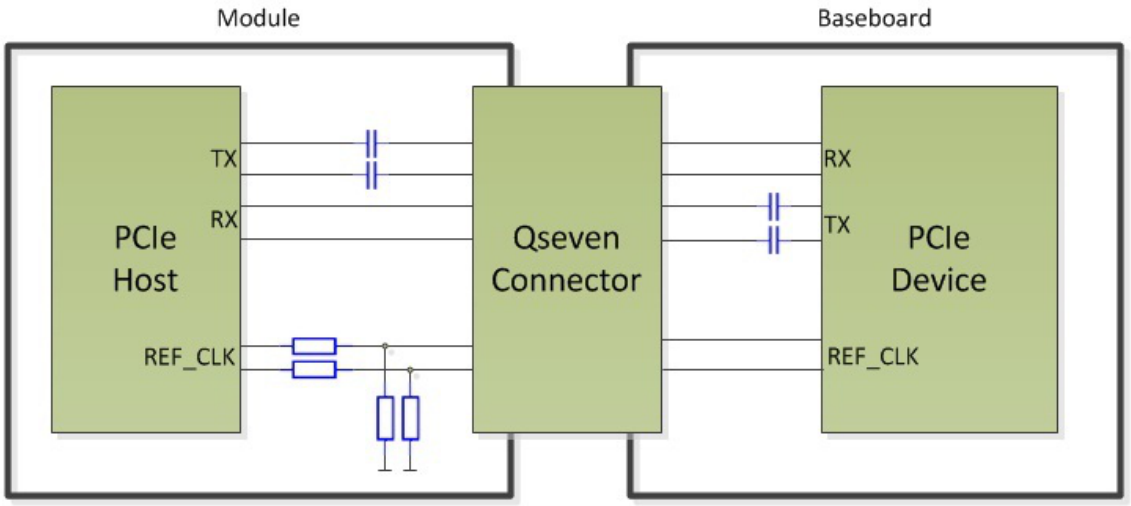
3.3.2 PCI Express Implementation Guidelines

All required pull-ups or pull-down resistors shall be implemented on the Qseven® module. This ensures that none of the signals that are not used will be left floating. Figure 3-4 shows the two standard configurations: “Slot” and “Device Down”.

Figure 3-4 PCI Express Termination Default Configurations

a) Slot Configuration





3.3.2.1 PCI Express Reference Clock

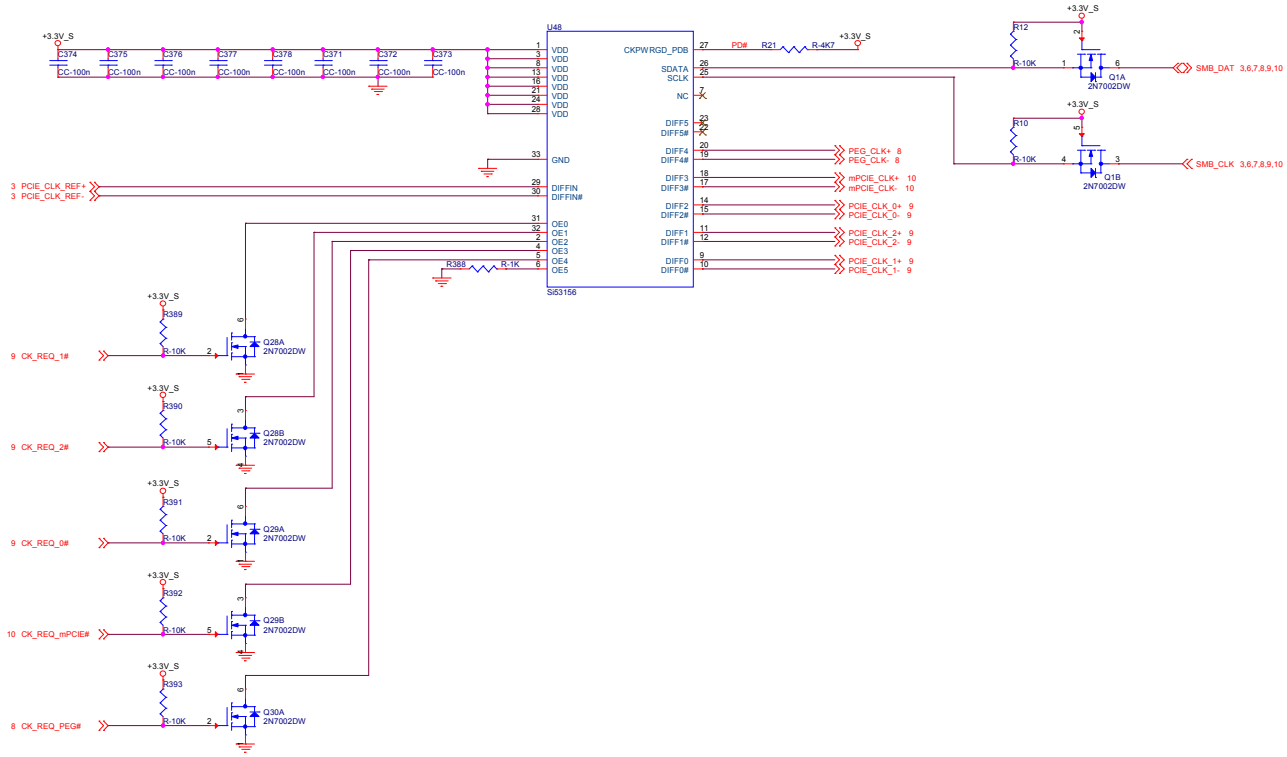
PCI Express does not specify the external clock source for PCI Express devices. It only provides a 100MHz differential Serial Reference Clock (SRC), which can be used by the internal PLL of the PCI Express device to generate the required 1.25GHz clock. The corresponding Serial Reference Clock signals *'PCI_CLK_REF+'* and *'PCI_CLK_REF-'* can be found on the Qseven® module connector on pins 155 and 157. In an application where more than one PCI Express slot or device is needed, the differential Serial Reference Clock signal must be replicated by using a buffer. Figure 3-3 shows an example implementing the ICS9DB833 PCI Express from Integrated Circuit Systems (ICS) (http://www.idt.com).

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This PCIe compliant clock buffer provides eight Serial Reference Clock outputs including clock request functionality. This circuit is also used on the Qseven® 2.0 evaluation carrier board.

The PCI Express architecture has specified the clock signal to be embedded in the serial data stream for synchronization of the two devices. For carrier board designs that implement PCI Express connectors for external add-in card devices, the SRC is required on the connector interface. External add-in cards may utilize this SRC differential signal pair to reduce jitter for maintaining maximum data transfer rate. For detailed information about this subject refer to chapter 2.1 of the 'PCI Express™ Card Electromechanical Specification Revision 1.1'.

Figure 3-5 PCI Express Clock Buffer Example



Note

Termination of all signals will be always on the module unless explicitly otherwise noted. Please note Figure 3-4 “PCI Express Termination default Configurations”.

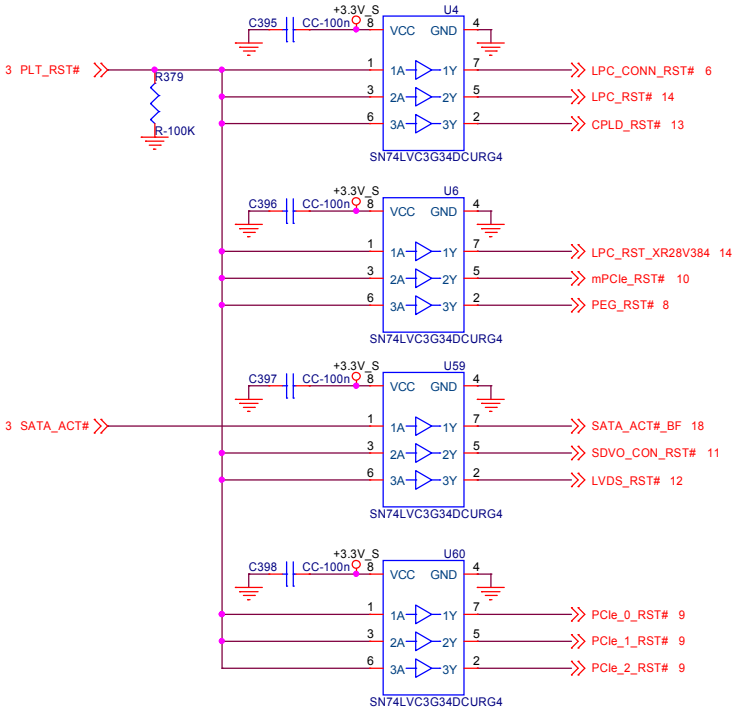
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3.3.2.2 PCI Express Reset

The Qseven® module provides one PCI Express Reset signal on pin 158 of the Qseven® connector(referenced as PLT_RST#) in the example schematics. It is recommended to use a buffer to replicate the Reset signal on the carrier board when more than one PCI Express slot or device is needed. Figure 3-6 shows a possible implementation example.

Figure 3-6 PCI Express Reset Buffer Example



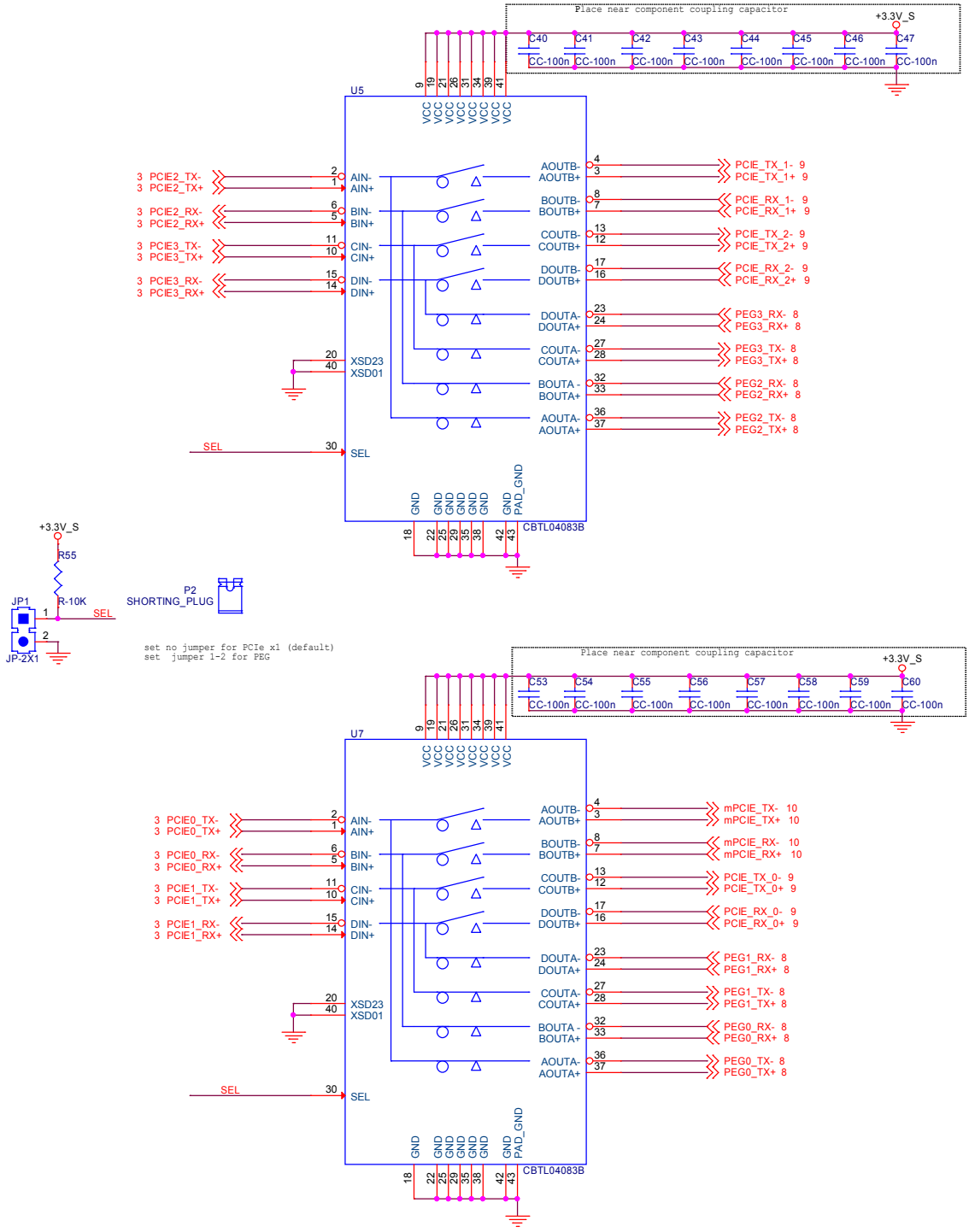
3.3.2.3 PCI Express Lane Configurations And Multiplexing

The lane configuration possibilities of the PCI Express interface of a Qseven® module is dependent on the module's chipset. If an application requires an x4 PCI Express link, it may be necessary to implement a hardware strap onto the carrier board in order to tell the module's chipset to switch the PCI Express lanes 0-3 from quad x1 to single x4 mode. The configuration possibilities and implementation requirements may differ depending on the module's chipset. Refer to the Qseven module's user's guide for additional information about this subject.

To provide maximum configuration flexibility the Qseven® V2.0 Reference Carrier Board is using a multiplexer for management and configuration of the four PCI Express lanes from the module.

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Figure 3-7 PCI Express Lanes Multiplexer



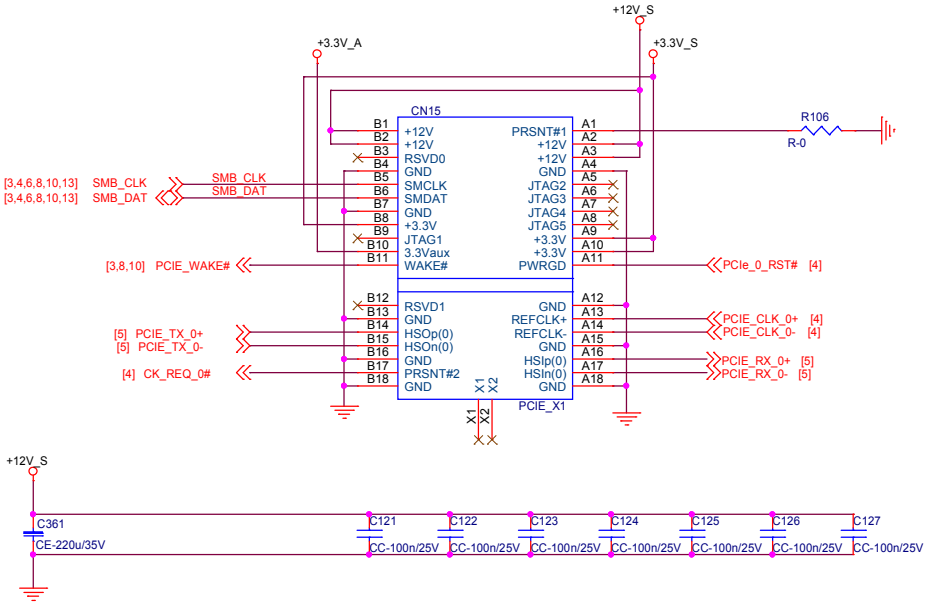
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3.3.2.4 PCI Express x1, x4 and x16 Connectors

Figure 3-8 illustrates the pinout definition for the standard x1 PCI Express connector as it has been implemented on the Qseven V2.0 Reference Carrier Board. It utilizes PCI Express lane 0.

Figure 3-8 PCI Express x1 Connector



Note

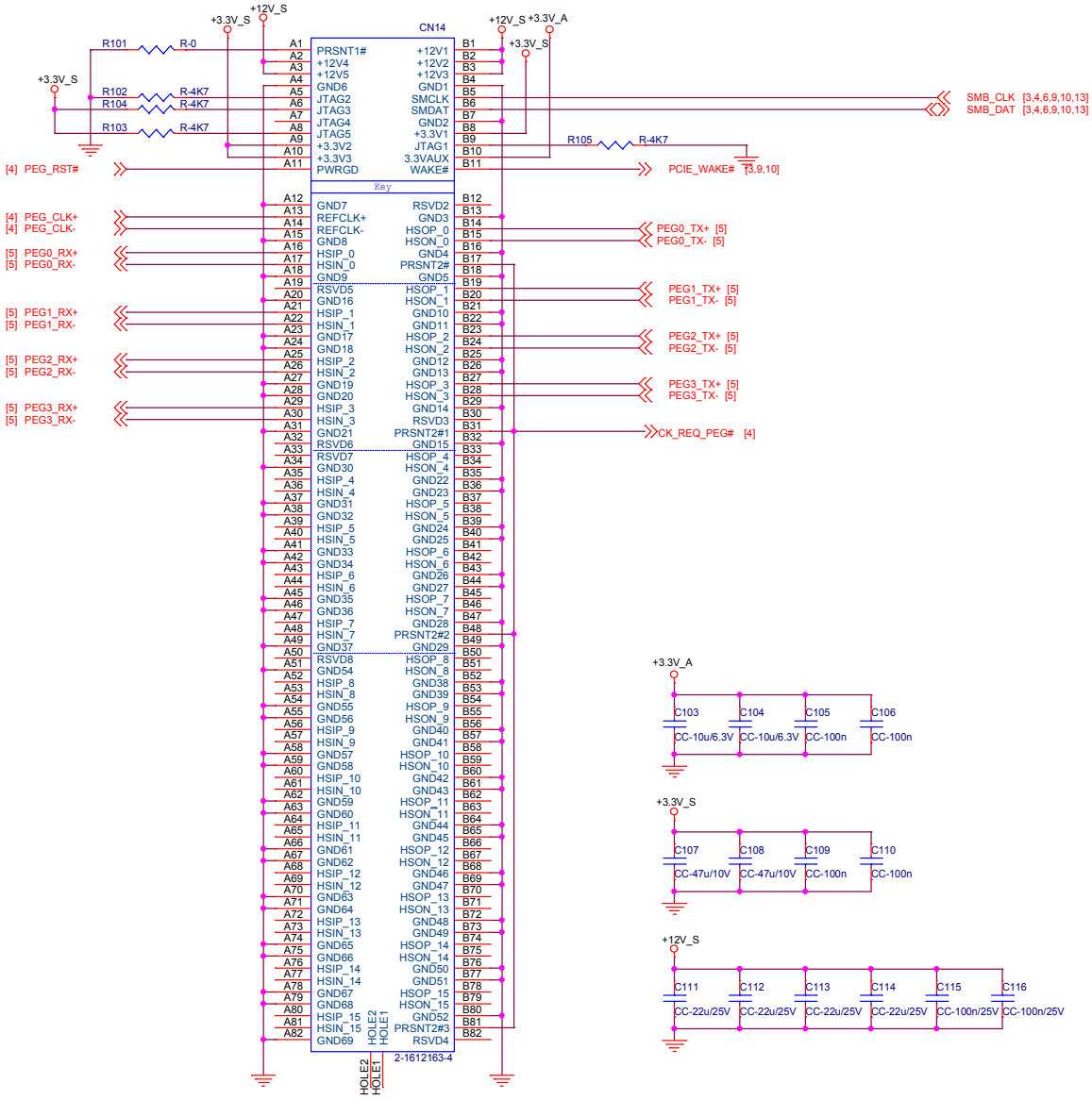
No crossing of TX and RX to socket.
Crossing of TX and RX only when PCIe Device is soldered down on the board

Figure 3-9 illustrates the pinout definition for the standard x16 PCI Express connector as it has has been implemented on the Qseven® V2.0 evaluation carrier board. It utilizes PCI Express lanes 0 to 3.

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Figure 3-9 PCI Express x16 Connector



PCIeX x16

Note

No crossing of TX and RX to socket.
Crossing of TX and RX only when PCIe Device is soldered down on the board

Signal fields in Table 3-4 that do not have any light grey shading describe the pinout for the PCI Express x1 slot (1 PCI Express Lane) and the signal fields marked with light grey indicate the additional signals needed on a PCI Express x4 connector (4 PCI Express Lanes), the fields marked with bold face characters indicate the additional signals required on a PCI Express x16 connector.

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Table 3-4 PCI Express x1, x4 and x16 Connector Pinout and Signal Description

Pin	Signal	Description	Pin	Signal	Description
1B	+12V	12V power	1A	PRSNT1#*	Hot-Plug presence detected
2B	+12V	12V power	2A	+12V	12V power
3B	+12V	12V power	3A	+12V	12V power
4B	GND	Ground	4A	GND	Ground
5B	SMB_CLK*	SMBus Clock	5A	JTAG2*	TCK - Boundary Scan Test Clock
6B	SMB_DAT*	SMBus Data	6A	JTAG3*	TDI – Boundary Scan Test Data Input
7B	GND	Ground	7A	JTAG4*	TDO - Boundary Scan Test Data Output
8B	+3.3V	3.3V power	8A	JTAG5*	TMS - Boundary Scan Test Mode Select
9B	JTAG1*	TRST# - Boundary Scan Test Reset	9A	+3.3V	3.3V power
10B	+3.3Vaux*	3.3V auxiliary power	10A	+3.3V	3.3V power
11B	PCIE_WAKE#*	Link Reactivation	11A	PCIE_RST#*	Reset
Mechanical Key					
12B	RSVD	Reserved	12A	GND	Ground
13B	GND	Ground	13A	PCIE_CLK_REF+*	Reference Clock differential pair positive signal
14B	PCIE0_TX+	Transmitter differential pair positive signal, Lane 0	14A	PCIE_CLK_REF-*	Reference Clock differential pair negative signal
15B	PCIE0_TX-	Transmitter differential pair negative signal, Lane 0	15A	GND	Ground
16B	GND	Ground	16A	PCIE0_RX+	Receiver differential pair positive signal, Lane 0
17B	PRSNT2#*	Hot-Plug presence detected	17A	PCIE0_RX-	Receiver differential pair negative signal, Lane 0
18B	GND	Ground	18A	GND	Ground
19B	**PCIE1_TX+**	**Transmitter differential pair positive signal, Lane 1**	**19A**	**RSVD**	**Reserved**
20B	**PCIE1_TX-**	**Transmitter differential pair negative signal, Lane 1**	**20A**	**GND**	**Ground**
21B	**GND**	**Ground**	**21A**	**PCIE1_RX+**	**Receiver differential pair positive signal, Lane 1**
22B	**GND**	**Ground**	**22A**	**PCIE1_RX-**	**Receiver differential pair negative signal, Lane 1**
23B	**PCIE2_TX+**	**Transmitter differential pair positive signal, Lane 2**	**23A**	**GND**	**Ground**
24B	**PCIE2_TX-**	**Transmitter differential pair negative signal, Lane 2**	**24A**	**GND**	**Ground**
25B	**GND**	**Ground**	**25A**	**PCIE2_RX+**	**Receiver differential pair positive signal, Lane 2**
26B	**GND**	**Ground**	**26A**	**PCIE2_RX-**	**Receiver differential pair negative signal, Lane 2**
27B	**PCIE3_TX+**	**Transmitter differential pair positive signal, Lane 3**	**27A**	**GND**	**Ground**

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Pin	Signal	Description	Pin	Signal	Description
28B	PCIE3_TX-	Transmitter differential pair negative signal, Lane 3	28A	GND	Ground
29B	GND	Ground	29A	PCIE3_RX+	Receiver differential pair positive signal, Lane 3
30B	RSVD	Reserved	30A	PCIE3_RX-	Receiver differential pair negative signal, Lane 3
31B	PRSTN2#1*	Hot-Plug presence detected	31A	GND	Ground
32B	GND	Ground	32A	RSVD	Reserved
33B	n/c	Not Connected	33A	RSVD	Reserved
34B	n/c	Not Connected	34A	GND	Ground
35B	GND	Ground	35A	n/c	Not Connected
36B	GND	Ground	36A	n/c	Not Connected
37B	n/c	Not Connected	37A	GND	Ground
38B	n/c	Not Connected	38A	GND	Ground
39B	GND	Ground	39A	n/c	Not Connected
40B	GND	Ground	40A	n/c	Not Connected
41B	n/c	Not Connected	41A	GND	Ground
42B	n/c	Not Connected	42A	GND	Ground
43B	GND	Ground	43A	n/c	Not Connected
44B	GND	Ground	44A	n/c	Not Connected
45B	n/c	Not Connected	45A	GND	Ground
46B	n/c	Not Connected	46A	GND	Ground
47B	GND	Ground	47A	n/c	Not Connected
48B	PRSTN2#2*	Hot-Plug presence detected	48A	n/c	Not Connected
49B	GND	Ground	49A	GND	Ground
50B	n/c	Not Connected	50A	RSVD	Reserved
51B	n/c	Not Connected	51A	GND	Ground
52B	GND	Ground	52A	n/c	Not Connected
53B	GND	Ground	53A	n/c	Not Connected
54B	n/c	Not Connected	54A	GND	Ground
55B	n/c	Not Connected	55A	GND	Ground
56B	GND	Ground	56A	n/c	Not Connected
57B	GND	Ground	57A	n/c	Not Connected
58B	n/c	Not Connected	58A	GND	Ground
59B	n/c	Not Connected	59A	GND	Ground
60B	GND	Ground	60A	n/c	Not Connected
61B	GND	Ground	61A	n/c	Not Connected
62B	n/c	Not Connected	62A	GND	Ground
63B	n/c	Not Connected	63A	GND	Ground
64B	GND	Ground	64A	n/c	Not Connected
65B	GND	Ground	65A	n/c	Not Connected
66B	n/c	Not Connected	66A	GND	Ground

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Pin	Signal	Description	Pin	Signal	Description
67B	n/c	Not Connected	67A	GND	Ground
68B	GND	Ground	68A	n/c	Not Connected
69B	GND	Ground	69A	n/c	Not Connected
70B	n/c	Not Connected	70A	GND	Ground
71B	n/c	Not Connected	71A	GND	Ground
72B	GND	Ground	72A	n/c	Not Connected
73B	GND	Ground	73A	n/c	Not Connected
74B	n/c	Not Connected	74A	GND	Ground
75B	n/c	Not Connected	75A	GND	Ground
76B	GND	Ground	76A	n/c	Not Connected
77B	GND	Ground	77A	n/c	Not Connected
78B	n/c	Not Connected	78A	GND	Ground
79B	n/c	Not Connected	79A	GND	Ground
80B	GND	Ground	80A	n/c	Not Connected
81B	PRSTN2#3*	Hot-Plug presence detected	81A	n/c	Not Connected
82B	RSVD	Reserved	82A	GND	Ground

Note

** Auxiliary signals. These signals are not required by the PCI Express Architecture.*

3.3.2.5 PCI Express Power Requirements

To utilize the full functionality of PCI Express devices on the Qseven® carrier board, some additional supply voltages may be necessary beside the standard supply voltages (see table 3-5).

When an external PCI Express Mini Card device will be implemented on the carrier board, an additional 1.5V supply voltage is required by the appropriate card sockets. The voltage regulator must be designed to meet the power requirements of the connected devices.

Note

Refer to the reference schematics of the Qseven® evaluation carrier board for an example of how to implement a 1.5V voltage regulator.

The PCI Express specification defines maximum power requirements for the different PCI Express connectors and/or devices. The power supply for the carrier board must be designed to meet these maximum power requirements. Table 3-5 shows the maximum current consumption defined for the different types of PCI Express connectors.

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Table 3-5 PCI Express Connector Power Requirements

Power Rail	PCIe x1, x4 or x8 Connector	PCIe x16 Connector	PCIe Mini Card 2.0 Connector
12V	2.1A @ 1000uF bulk	5.5A @ 2000uF bulk	
3.3V	3.0A @ 1000uF bulk	3.0A @ 1000uF bulk	
3.3V Standby Aux	375mA @ 150uF bulk	375mA @ 150uF bulk	1.1A / 2.75A (peak)
1.5V			500mA

Implementing PCI Express connectors on the carrier board requires distinctive decoupling of the connector supply voltages to reduce possible voltage drops and to provide an AC return path in a manner consistent with high-speed signaling techniques. Decoupling capacitors should be placed as close as possible to the power pins of the connectors. Table 3-6 shows the minimum requirements for power decoupling of the different power pin types of each PCI Express connector type.

Table 3-6 PCIe Power Decoupling Requirements

Power Pin Type	PCIe x1, x4 or x8 Connector	PCIe x16 Connector	PCIe Mini Card 2.0 Connector
12V	1x 22µF, 2x 100nF	4x 22uF, 2x 100nF	
3.3V	1x 22uF, 2x 100nF	1x 100uF, 2x 100nF	
3.3V Standby Aux	1x 22uF, 1x 100nF	1x 22uF, 1x 100nF	
1.5V			3x 100nF

3.3.2.6 PCI Express Mini Card 2.0

The PCI Express Mini Card 2.0 add-in card is a small size unique form factor optimized for mobile computing platforms equipped with communication applications such as Wireless LAN. A small footprint connector can be implemented on the carrier board providing the ability to insert different removable PCI Express Mini Cards. Using this approach gives the flexibility to mount an upgradeable, standardized PCI Express Mini Card 2.0 device to the carrier board without the additional expenditure of a redesign.

In addition to a PCI Express x1 link and a USB 2.0 link, the PCI Express Mini Card 2.0 interface utilizes the following control and reset signals, which are provided by the Qseven® module.

Table 3-7 PCI Express Mini Card 2.0 Control Signal Descriptions

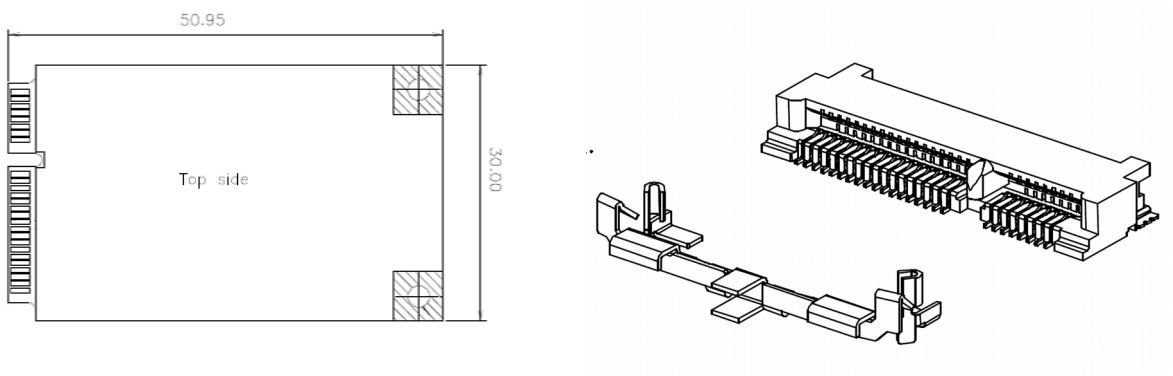
Signal	Pin	Description	I/O	Comment
SMB_CLK / GP1_I2C_CLK	60	System Management Bus Clock Signal	I/O 3.3V OD CMOS	PU resistors shall be located on the CPU Module
SMB_DAT / GP1_I2C_DAT	62	System Management Bus Data Signal	I/O 3.3V OD CMOS	PU resistors shall be located on the CPU Module

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The reference circuit for PCI Express Mini Card 2.0 adaptation displayed in Figure 3-11 uses the following signals that are generated on the Qseven® evaluation carrier board.

Signal	Description	I/O	
PCIE_RST#_5	PCI Express Bus Reset	I 3.3V Standby CMOS	This signal originates from the PCI Express reset buffer shown in Figure 3-6 'PCI Express Reset Buffer Circuitry'
PCIECLK_OE5#	Request for PCI Express Serial Reference Clock. For more details see section 'PCI Express Reference Clock' for details.	I 3.3V CMOS	This signal originates from the clock buffer shown in Figure 3-5 'PCI Express Clock Buffer Circuitry'.

Figure 3-10 PCI Express Mini Card 2.0 and Socket



Note

Compatible half-sized cards are available from a variety of vendors

A potential source for this PCI Express Mini Card 2.0 carrier board connector is: AMP/Tyco HARD TRAY ASSY MINI PCI EXPRESS CONNECTOR 52 POS Article No. 1717831-1.

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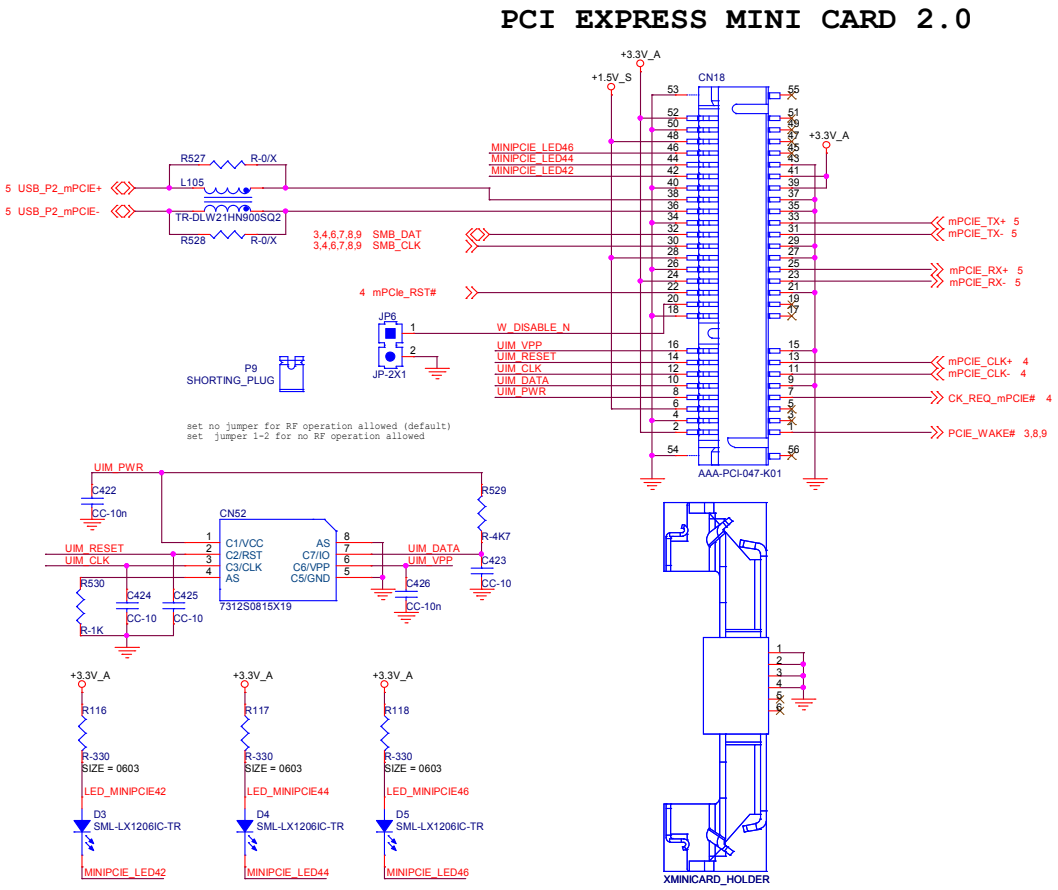
Table 3-8 PCI Express Mini Card 2.0 Connector Pinout

Pin	Signal	Description	Pin	Signal	Description
1	WAKE#	Request that the host interface return to full operation and respond to PCIe.	2	+3.3V	Primary voltage source, 3.3V.
3	RSVD	Reserved	4	GND	Ground
5	RSVD	Reserved	6	+1.5V	Secondary voltage source, 1.5V.
7	CLKREQ#	Reference clock request signal.	8	UIM_PWR	Power source for User Identity Modules (UIM).
9	GND	Ground	10	UIM_DATA	Data signal for UIM.
11	REFCLK-	Reference Clock differential pair negative signal.	12	UIM_CLK	Clock signal for UIM.
13	REFCLK+	Reference Clock differential pair positive signal.	14	UIM_RESET	Reset signal for UIM.
15	GND	Ground	16	UIM_VPP	Variable supply voltage for UIM.
Mechanical Key					
17	RSVD	Reserved for future second User Identity Modules interface (UIM_C8).	18	GND	Ground
19	RSVD	Reserved for future second User Identity Module interface (UIM_C4).	20	W_DISABLE	Used by the system to disable radio operation on add-in cards that implement radio frequency application.
21	GND	Ground	22	PERST#	PCI Express Reset
23	PCIEx_RX-	Receiver differential pair negative signal, Lane x.	24	3.3Vaux	Auxiliary voltage source, 3.3V.
25	PCIEx_RX+	Receiver differential pair positive signal, Lane x.	26	GND	Ground
27	GND	Ground	28	+1.5V	Secondary voltage source, 1.5V.
29	GND	Ground	30	SMB_CLK	System Management Bus Clock.
31	PCIEx_TX-	Transmitter differential pair negative signal, Lane x.	32	SMB_DATA	System Management Bus Data.
33	PCIEx_TX+	Transmitter differential pair positive Signal, Lane x.	34	GND	Ground
35	GND	Ground	36	USB_D-	USB Serial Data Interface differential pair, negative signal.
37	GND	Ground	38	USB_D+	USB Serial Data Interface differential pair, positive signal.
39	3.3Vaux	Auxiliary voltage source, 3.3V.	40	GND	Ground
41	3.3Vaux	Auxiliary voltage source, 3.3V.	42	LED_WWAN#	LED status indicator signals provided by the system.
43	GND	Ground	44	LED_WLAN#	LED status indicator signals provided by the system.
45	RSVD	Reserved for future second PCIe lane.	46	LED_WPAN#	LED status indicator signals provided by the system.
47	RSVD	Reserved for future second PCIe lane.	48	+1.5V	Secondary voltage source, 1.5V.
49	RSVD	Reserved for future second PCIe lane.	50	GND	Ground
51	RSVD	Reserved for future second PCIe lane.	52	+3.3V	Primary voltage source, 3.3V.

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Figure 3-11 displays an example of how a PCI Express Mini Card 2.0 socket can be connected to a Qseven® carrier board. The same solution has been implemented on the Qseven® V2.0 evaluation carrier board. It utilizes USB Port 2 and PCI Express lane 0 (via the PCIe Multiplexer shown in Figure 3-7).

Figure 3-11 PCI Express Mini Card Reference Circuitry



3.3.2.7 PCI Express Switch

In applications where additional PCI Express lanes other than those provided by the Qseven® module are needed, a PCI Express Switch on the Qseven® carrier board can be used to expand the number of available PCI Express lanes.

Note:

The current Qseven® V2.0 evaluation carrier board is using a multiplexer (shown in Figure 3-7) and not a switch for lane expansion.

*If you are looking for an example of a PCI Express Switch please refer to the Qseven V1.2 Design Guide, chapter 3.3.7 .The example shown there is the implementation on the Qseven® V1.2 evaluation carrier board using a 5 Lane 5 Port PCI Express Switch PEX8505AA25BIG from PLX Technology (*http://www.plxtech.com*).*

3.3.3 Routing Considerations for PCI Express

See section 4 of this document for trace routing guidelines and the Qseven® specification for more information about this subject.

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3.4 UART

3.4.1 UART Interface Signals

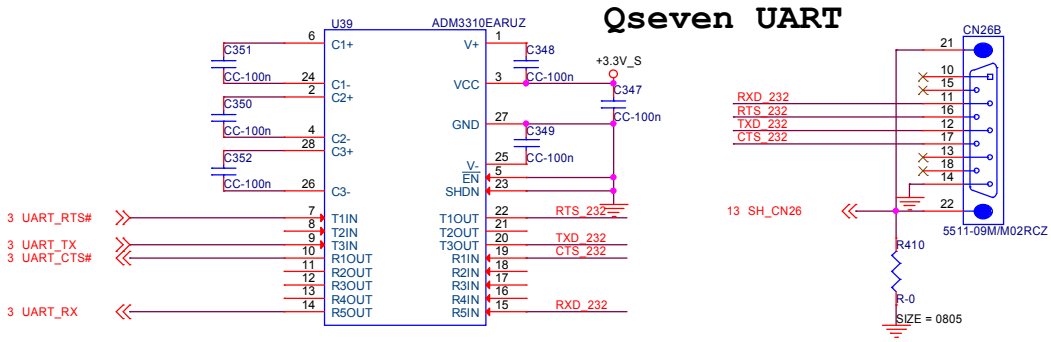
Table 3-9 Signal Definition of UART

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
UART0_TX	Serial Data Transmitter	CMOS 3.3V	max 1 mA	O
UART0_RX	Serial Data Receiver	CMOS 3.3V	≥ 5 mA	I
UART0_CTS#	Handshake signal, ready to send data	CMOS 3.3V	≥ 5 mA	I
UART0_RTS#	Handshake signal, ready to receive data	CMOS 3.3V	max. 1 mA	O

3.4.2 UART Implementation example

Figure 3-12 shows a reference circuitry for a serial COM0 Interface as implemented on the Qseven V2.0 reference carrier board.

Figure 3-12 UART Reference Circuitry



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3.5 Gigabit Ethernet LAN

Qseven® modules provide at least one 10/100/1000BaseT Gigabit Ethernet LAN port compliant with the IEEE 802.3ab specification.

3.5.1 Gigabit Ethernet Signals

The LAN interface of the Qseven® module consists of 4 pairs of low voltage differential pair signals designated from *'GBE_MDI0'* (+ and -) to *'GBE_MDI3'* (+ and -) plus additional control signals for link activity indicators. These signals can be used to connect a 10/100/1000BaseT RJ45 connector with integrated or external isolation magnetics to the carrier board.

Table 3-10 Signal Definition Ethernet Signals

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
GBE_MDI0+ GBE_MDI0-	12 10	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	GB_LAN		I/O
GBE_MDI1+ GBE_MDI1-	11 9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	GB_LAN		I/O
GBE_MDI2+ GBE_MDI2-	6 4	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	GB_LAN		I/O
GBE_MDI3+ GBE_MDI3-	5 3	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	GB_LAN		I/O
GBE_CTREF	15	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output should be current limited on the module. In a situation in which the reference is shorted to ground, the current must be limited to 250mA or less.	REF		O
GBE_LINK#	13	Ethernet controller link indicator, active low.	CMOS 3.3V PP	max 10 mA	O
GBE_LINK100#	7	Ethernet controller 100Mbit/sec link indicator, active low.	CMOS 3.3V PP	max 10 mA	O
GBE_LINK1000#	8	Ethernet controller 1000Mbit/sec link indicator, active low.	CMOS 3.3V PP	max 10 mA	O
GBE_ACT#	14	Ethernet controller activity indicator, active low.	CMOS 3.3V PP	max 10 mA	O

3.5.2 LAN Implementation Guidelines

The most critical component in the LAN interface is the isolation magnetics connected directly to the MDI differential pair signals of the Qseven® module. It should be carefully qualified for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection and Crosstalk Isolation to pass the IEEE conformance tests and EMI tests.

Even if a Qseven® module complies with the basic specifications set forth for IEEE certification, it's still possible that the overall system could fail IEEE testing because of a poor quality or unsuitable external isolation magnetics module and/or improper PCB layout of the carrier board.

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3.5.2.1 LAN Magnetics Modules

1000Base-T Ethernet magnetics modules are similar to those designed solely for 10/100 BaseTx Ethernet, except that there are four MDI differential signal pairs instead of two. 1000Base-T magnetics modules have a center tap pin that is connected to the reference voltage output *'GBE_CTREF'* of the Qseven® module, which biases the controller's output buffers. Magnetics with four center tap pins may have better characteristics than those with one or two center tap pins. Depending on the PHY manufacturer some PHYs may require, that each differential pair center tap pin is connected separately via a capacitor to ground. In this case the PHY center tap pins are not connected together.The isolation magnetics can be integrated in a RJ45 jack, which also provides activity and speed LED indicators. Alternatively, they can be designed as discrete magnetics modules, which will be connected to a pure RJ45 jack. Table 3-11 lists recommended magnetics modules and RJ45 jacks for usage on a carrier board design.

Table 3-11 Recommended LAN Magnetic Modules

Manufacturers	Part Number	Technology	Comments
Pulse Engineering	H5007	10/100/1000BaseT	Discrete magnetics module
Pulse Engineering	JK0-0036	10/100/1000BaseT	RJ45 jack with integrated magnetics and activity LEDs
Bel Fuse	S558-5999–P3	10/100/1000BaseT	Discrete magnetics module
Pulse	JW0A1P01R-E	10/100/1000BaseT	RJ45 jack with integrated magnetics and USB jacks
Foxconn	UB11123-J51	10/100/1000BaseT	RJ45 jack with integrated magnetics and USB jacks

For optimum performance consult module manufacturers for magnetics recommendations and schematics

3.5.2.2 LAN Component Placement

When using RJ45 connectors without integrated magnetics, the discrete magnetics module has to be placed as close as possible to the RJ45 connector. The distance between the magnetics module and RJ45 connector must be less than 1 inch. This distance requirement must be observed during the carrier board layout when implementing LAN. Due to the insertion loss budget of Qseven®, the overall trace length of the MDI signal pairs on the carrier board should be less than 4 inches. Signal attenuation could cause data transfer problems for traces longer than 4 inches.

3.5.2.3 LAN Ground Plane Separation

Isolated separation between the analog ground plane and digital ground plane is recommended. If this is not implemented properly then bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to ground bounce noise.

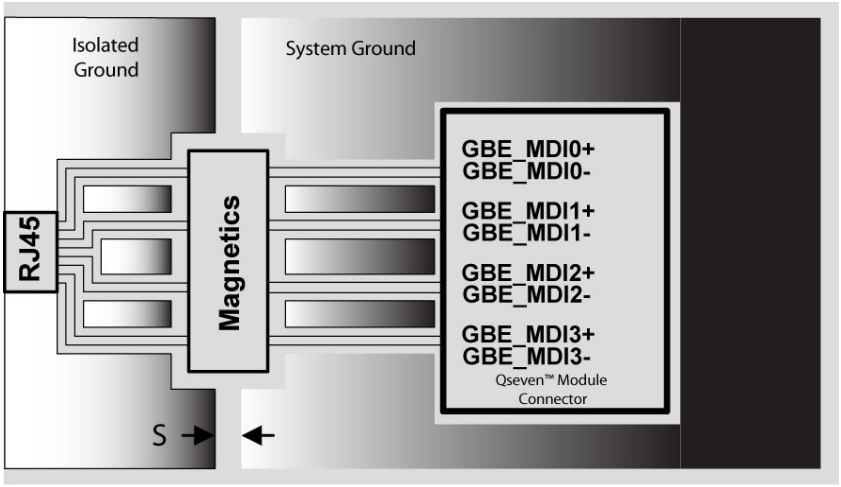
The plane area underneath the magnetic module should be left empty. This free area is to keep transformer induced noise away from the power and system ground planes.

The isolated ground, also called chassis ground, connects directly to the fully shielded RJ45 connector. For better isolation it is also important to maintain a gap between chassis ground and system ground that is wider than 60mils. For ESD protection, a 3kV high voltage capability capacitor is recommended to connect to this chassis ground.

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Figure 3-13 LAN Ground Plane Separation



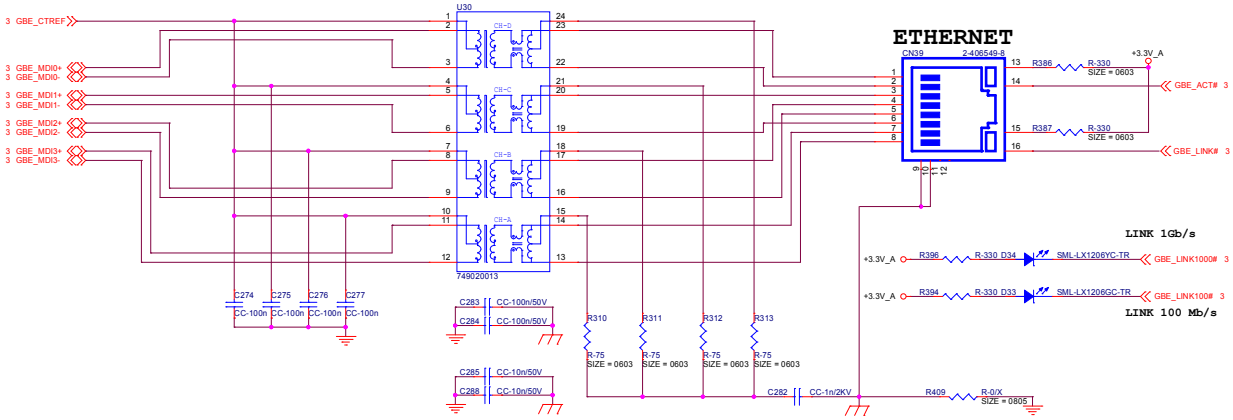
S= Ground Plane Separation

3.5.2.4 LAN Link Activity and Speed LED

The Qseven® module has four 3.3V push/pull outputs to directly drive activity, speed indication and link status LEDs. The 3.3V standby voltage should be used as LED supply voltage so that the link activity can be viewed during system standby state. Since LEDs are likely to be integrated into a RJ45 connector with integrated magnetics module, the LED traces need to be routed away from potential sources of EMI noise. Consider adding a filtering capacitor per LED for extremely noisy situations. The suggested value for this capacitor is 470pF.

3.5.2.5 LAN Reference Schematics

Figure 3-14 GbE Schematic Example



Note:

Depending on the PHY manufacturer some PHYs may require that each differential pair center tap pin is connected separately via a capacitor to ground. In this case the PHY center tap pins are not connected together.

3.5.3 Routing Considerations for LAN

See section 4 of this document for trace routing guidelines and the Qseven® specification for more information about this subject.

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3.6 Serial ATA Interface

Serial ATA (SATA) is a serial interface for connecting storage devices (mainly hard disks) and was defined to replace the old parallel ATA interface. Serial ATA uses a point-to-point serial connection between the system and the storage device. The first generation of standard Serial ATA provides a maximum effective data transfer rate of 150MB/s per port. With the second generation SATA II, an effective transfer rate of up to 300MB/s per port is possible. Serial ATA is completely software transparent to the IDE interface while providing a lower pin count and higher performance.

3.6.1 Serial ATA Interface Signals

Qseven® modules can provide up to 2 Serial ATA channels, each with a receive and transmit differential signal pair designated from *'SATA0_RX'* (+ and -) to *'SATA1_RX'* (+ and -) and correspondingly from *'SATA0_TX'* (+ and -) to *'SATA1_TX'* (+ and -). The appropriate signals can be found on the Qseven® module connector.

Table 3-12 Signal Definition SATA

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
SATA0_RX+ SATA0_RX-	35 37	Serial ATA channel 0, Receive Input differential pair.	SATA		I
SATA0_TX+ SATA0_TX-	29 31	Serial ATA channel 0, Transmit Output differential pair.	SATA		O
SATA1_RX+ SATA1_RX-	36 38	Serial ATA channel 1, Receive Input differential pair.	SATA		I
SATA1_TX+ SATA1_TX-	30 32	Serial ATA channel 1, Transmit Output differential pair.	SATA		O
SATA_ACT#	33	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC 3.3V	max. 10mA	O

3.6.2 Serial ATA Implementation Example

Figure 3-15 shows an example implementation of Serial ATA hard drive Interfaces on the Qseven® V2.0 carrier board. In this example Serial ATA channel 1 of the Qseven® module is used directly and channel 0 uses a SATA switch to switch alternatively to an mSATA connector. The Serial ATA hard drive can be powered directly or by a Serial ATA power connector implemented on the carrier board.

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Figure 3-15 Example Serial ATA Implementation (Data and Power)

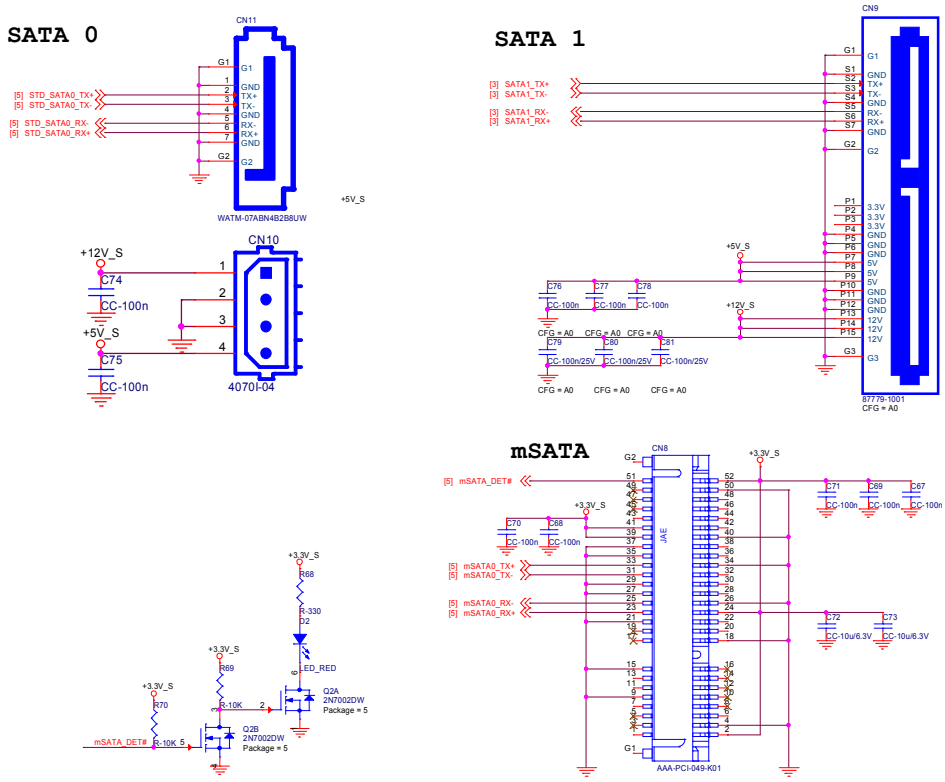
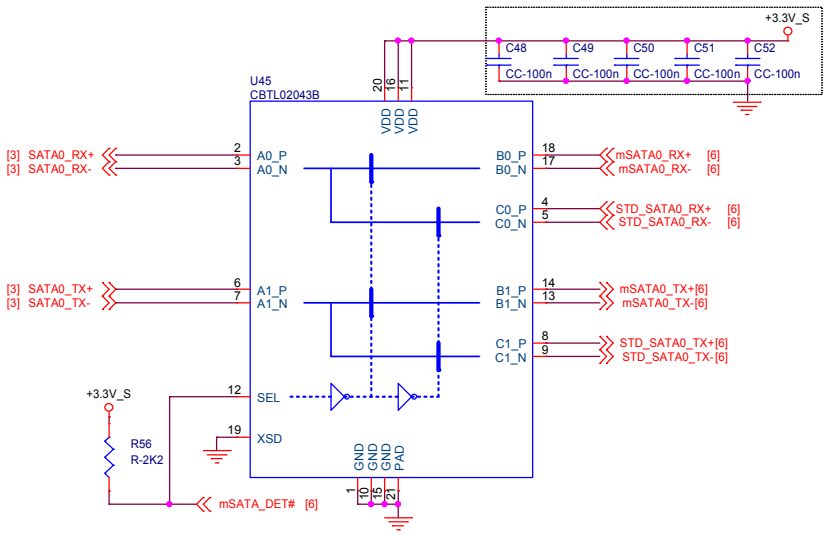


Figure 3-16 Example for a Serial ATA / mSATA Switch implementation



-

Table 3-13 Serial ATA Data Connector Pinout and Signal Description

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	5	RX-	Receiver differential pair negative signal
2	TX+	Transmitter differential pair positive signal	6	RX+	Receiver differential pair positive signal
3	TX-	Transmitter differential pair negative signal	7	GND	Ground
4	GND	Ground			

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Table 3-14 Serial ATA Power Connector Pinout and Signal Description

Pins	Signal	Description	Pins	Signal	Description
1 2 3	+3.3V	3.3V power supply	10 11 12	GND	Ground
4 5 6	GND	Ground	13 14 15	+12V	12V power supply
7 8 9	+5V	5V power supply			

Table 3-15 mSATA Connector Pinout and Signal Description

Pin	Signal	Description	Pin	Signal	Description
1	RSVD	Reserved	2	+3.3V	3.3V.power supply
3	RSVD	Reserved	4	GND	Ground
5	RSVD	Reserved	6	n/c	1.5V secondary voltage source*
7	RSVD	Reserved	8	RSVD	Reserved
9	GND	Ground	10	RSVD	Reserved
11	RSVD	Reserved	12	RSVD	Reserved
13	RSVD	Reserved	14	RSVD	Reserved
15	GND	Ground	16	RSVD	Reserved
Mechanical Key					
17	RSVD	Reserved	18	GND	Ground
19	RSVD	Reserved	20	RSVD	Reserved
21	GND	Ground	22	RSVD	Reserved
23	RX+	Receiver differential pair positive signal	24	3.3Vaux	3.3V.power supply
25	RX-	Receiver differential pair negative signal	26	GND	Ground
27	GND	Ground	28	n/c	1.5V secondary voltage source*
29	GND	Ground	30	n/c	System Management Bus Clock.
31	TX-	Transmitter differential pair negative signal	32	n/c	System Management Bus Data.
33	TX+	Transmitter differential pair positive Signal	34	GND	Ground
35	GND	Ground	36	RSVD	Reserved
37	GND	Ground	38	RSVD	Reserved
39	+3.3V	3.3V.power supply	40	GND	Ground
41	+3.3V	3.3V.power supply	42	RSVD	Reserved
43	RSVD	Reserved	44	RSVD	Reserved
45	RSVD	Reserved	46	RSVD	Reserved
47	RSVD	Reserved	48	n/c	1.5V secondary voltage source*
49	RSVD	Reserved	50	GND	Ground
51	DET	mSATA device presence detection	52	+3.3V	Primary voltage source, 3.3V

* There is no 1.5V power rail used in the Qseven V2.0 reference carrier board

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Note

mSATA (Mini Serial ATA, not to be confused with micro Serial ATA) is using a standard PCI express mini card connector, however the pinout is different.

3.6.3 Routing Considerations for Serial ATA

See section 4 of this document for trace routing guidelines and the Qseven® specification for more information about this subject.

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3.7 USB Interface

The Universal Serial Bus interface of the Qseven® module is compliant to USB 1.1 as well as USB 2.0 and USB 3.0 specification. Qseven® specifies a minimum configuration of 3 USB 2.0 host ports for ARM architectures respectively 4 USB 2.0 ports for Intel architectures up to a maximum of 8 ports on both platforms.
The number of USB 3.0 ports may vary from 0 to 2 ports on both platforms.

Note

Depending on the Qseven® module' used, some USB ports may not support USB 1.1 , USB 2.0 or USB 3.0.

3.7.1 USB Interface Signals

USB Port1 can be optionally configured as a USB client port

Table 3-16 Signal Definition USB

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
USB_P0+	96	Universal Serial Bus Port 0 differential pair +	USB		I/O
USB_P0-	94	Universal Serial Bus Port 0 differential pair -	USB		I/O
USB_P1+	95	Universal Serial Bus Port 1 differential pair + This port may be optionally used as USB client port (+)	USB		I/O
USB_P1-	93	Universal Serial Bus Port 1 differential pair - This port may be optionally used as USB client port (-)	USB		I/O
USB_P2+	90	Universal Serial Bus Port 2 differential pair +	USB		I/O
USB_P2-	88	Universal Serial Bus Port 2 differential pair -	USB		I/O
USB_P3+	89	Universal Serial Bus Port 3 differential pair +	USB		I/O
USB_P3-	87	Universal Serial Bus Port 3 differential pair -	USB		I/O
USB_P4+ / USB_SSRX1+	84	Universal Serial Bus Port 4 differential pair + / USB SuperSpeed Channel 1 receive data +	USB / USB SuperSpeed		I/O I
USB_P4- / USB_SSRX1-	82	Universal Serial Bus Port 4 differential pair - / USB SuperSpeed Channel 1 receive data -	USB / USB SuperSpeed		I/O I
USB_P5+ / USB_SS_TX1+	83	Universal Serial Bus Port 5 differential pair + / USB SuperSpeed Channel 1 transmit data -	USB / USB SuperSpeed		I/O O
USB_P5- / USB_SS_TX1-	81	Universal Serial Bus Port 5 differential pair - / USB SuperSpeed Channel 1 transmit data -	USB / USB SuperSpeed		I/O O
USB_P6+ / USB_SS_TX0+	78	Universal Serial Bus Port 6 differential pair + / USB SuperSpeed Channel 0 receive data +	USB / USB SuperSpeed		I/O
USB_P6- / USB_SS_RX0-	76	Universal Serial Bus Port 6 differential pair - / USB SuperSpeed Channel 0 receive data -	USB / USB SuperSpeed		I/O I
USB_P7+ / USB_SS_TX0+	77	Universal Serial Bus Port 7 differential pair + / USB SuperSpeed Channel 0 transmit data +	USB / USB SuperSpeed		I/O O
USB_P7- / USB_SS_TX0-	75	Universal Serial Bus Port 7 differential pair - / USB SuperSpeed Channel 0 transmit data -	USB / USB SuperSpeed		I/O O
USB_0_1_OC#	86	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_2_3_OC#	85	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_4_5_OC#	80	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	CMOS 3.3V Suspend	≥ 5 mA	I

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Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
USB_6_7_OC#	79	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_VBUS	91	USB VBUS pin. • 5V tolerant • VBUS resistance has to be placed on the module • VBUS capacitance has to be placed on the carrier board	CMOS 5.0V	<=2.5mA (B-device)	I
USB_ID	92	USB ID pin. Configures the mode of the USB Port 1. The resistance of this pin measured to ground is used to determine whether USB Port 1 is going to be used as USB Client to enable/ disable USB Client support. Please check the USB-OTG Reference of your chip manufacturer for further details.	Analogue		O
USB_OTG_PEN	56	USB Power enable pin for USB Port 1 Enables the Power for the USB-OTG port on the carrier board.	CMOS 3.3V		I

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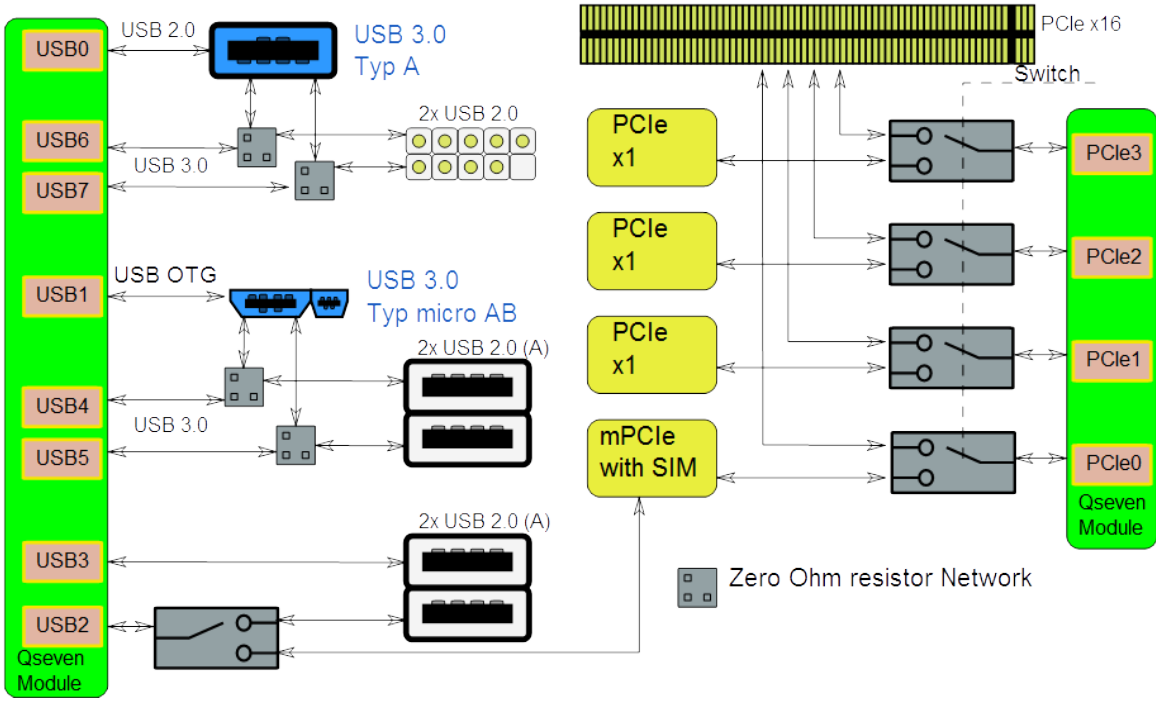
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3.7.2 USB Implementation Guidelines

3.7.2.1 Mixed USB2.0/3.0 Distribution

The Qseven V2.0 standard enables a variety of possible implementations for USB 2.0 and/or USB 3.0 implementations. It's also ready for USB on-the-go (USB-OTG) implementations. In addition to the switches used in the Qseven V2.0 Reference Carrier Board another method to keep maximum configuration flexibility for evaluation carrier boards is to use zero ohm resistors to switch between 2.0 and 3.0 usage of the USB signals coming from the module. For signal integrity reasons fixed solutions or zero ohm resistors are preferred for custom production boards, especially when utilizing USB 3.0.

Figure 3-17 Example for USB 2.0 / 3.0 distribution



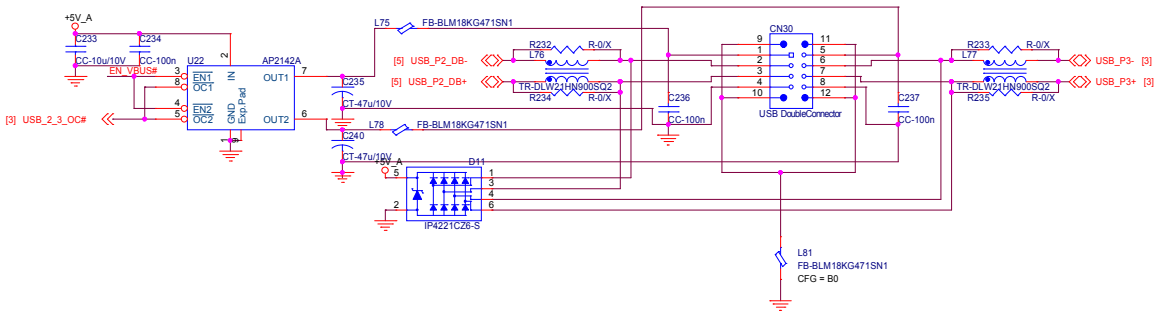
Please refer also to Figure 3-2 USB and PCI express distributions of the final Qseven V2.0 Reference Board.

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3.7.2.2 USB 2.0 Reference Schematics

Figure 3-18 USB 2.0 Reference Circuit



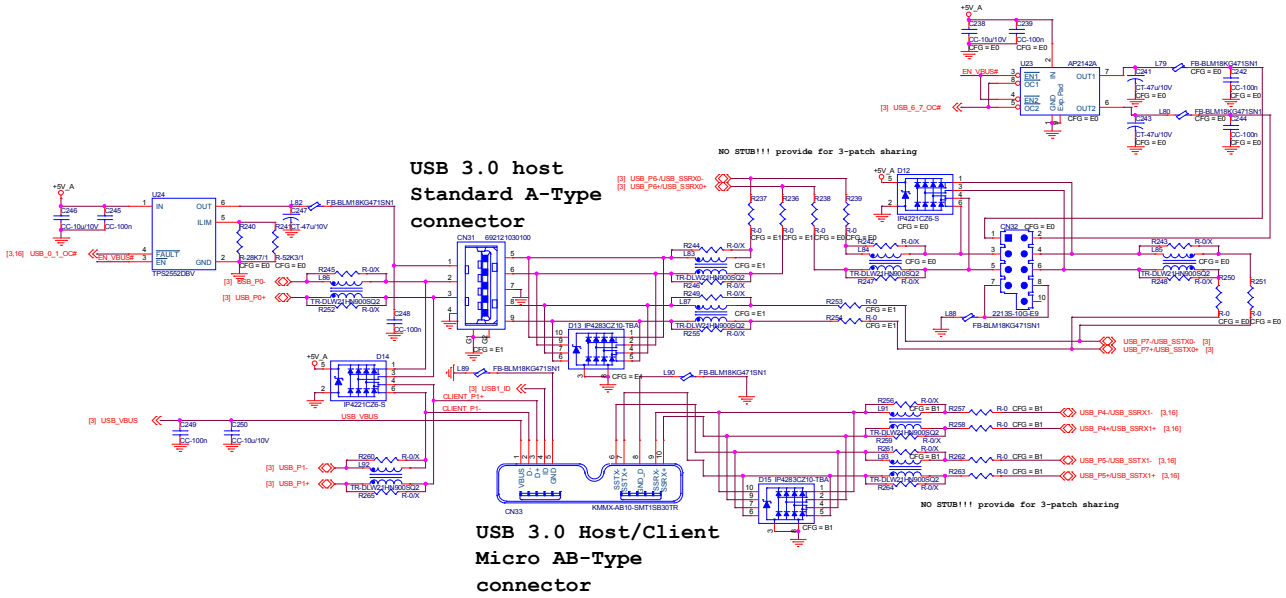
This example shows an USB2.0 implementation without USB switches/multiplexers as shown in Figure 3-17. It uses dual USB 2.0 connectors for the USB ports 2, 3, and 4, 5.

Table 3-17 USB 2.0 Host Dual Type-A Connector Pinout

Signal	Pin	Description	I/O	Comment
VCC	1	+5V Power Supply	P 5V	
D-	2	Universal Serial Bus Data, negative differential signal.	I/O USB	
D+	3	Universal Serial Bus Data, positive differential signal.	I/O USB	
GND	4	Ground	P	

3.7.2.3 USB 3.0 Reference Schematics

Figure 3-19 USB 3.0 Reference Circuit



This example shows a USB 3.0 implementation with zero ohm resistors instead of switches/multiplexers for configuration. It uses a USB 3.0 Type A Host connector for the the channel 0 USB 3.0 host and a USB 3.0 microAB connector for the second host channel 1 and alternatively the USB 2.0 Client Port 1.

Table 3-18 USB 3.0 Type A Connector Pinout

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Signal	Pin	Description	I/O	Comment
VBUS	1	+5V Power Supply	Power 5V	
D-	2	Universal Serial Bus Data, negative differential signal.	I/O USB	
D+	3	Universal Serial Bus Data, positive differential signal.	I/O USB	
GND	4	Ground	GND	
StdA_SSRX-	5	High Speed Input -	I	
StdA_SSRX+	6	High Speed Input +	I	
GND Drain	7	Reference Ground	GND	
StdA_SSTX-	8	High Speed Output -	O	
StdA_SSTX+	9	High Speed Output -	O	
Shield	G1	Connector Shell	GND	
Shield	G2	Connector Shell	GND	

Table 3-19 USB 3.0 microAB Host/Client Connector Pinout

Signal	Pin	Description	I/O	Comment
VBUS	1	+5V Power Supply	Power 5V	
D-	2	Universal Serial Bus Data, negative differential signal.	I/O USB	
D+	3	Universal Serial Bus Data, positive differential signal.	I/O USB	
OTG ID	4	OTG ID for identifying lines		USB_ID signal from module
GND	5	Ground	GND	
StdA_SSRX-	6	High Speed Input -	I	
StdA_SSRX+	7	High Speed Input +	I	
GND Drain	8	Reference Ground	GND	
StdA_SSTX-	9	High Speed Output -	O	
StdA_SSTX+	10	High Speed Output -	O	

Note:

Depending on the module used there are two methods for switching between host and client mode for USB Port 1:

1. *OTG (on-the-go) and*
2. *manual selection.*

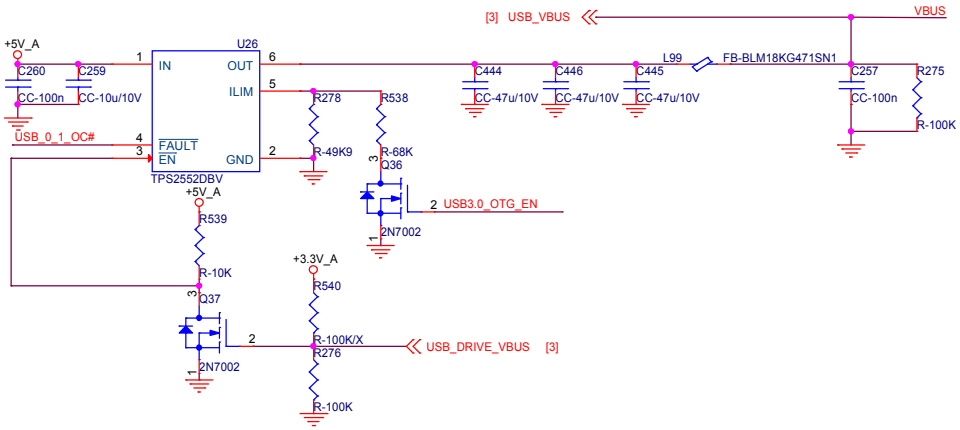
OTG switches automatically in a runtime environment, manual selection can be realized using Bios setup

3.7.2.4 USB Overcurrent Protection

Figure 3-20 Current Limiter Circuitry

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The USB Specification describes power distribution over the USB port, which supplies power for USB devices that are directly connected to the carrier board. Therefore, the host must implement over-current protection on the ports for safety reasons. Should the aggregate current drawn by the downstream ports exceed a permitted value, the overcurrent protection circuit removes power from all affected downstream ports. The overcurrent limiting mechanism must be resettable without user mechanical intervention. For more detailed information about this subject refer to the 'Universal Serial Bus Specifications Revision 2.0', which can be found at http://www.usb.org.

Over-current protection for USB ports can be implemented by using power distribution switches on the carrier board that monitor the USB port power lines. Power distribution switches usually have a soft-start circuitry that minimizes inrush current in applications where highly capacitive loads are employed. Transient faults are internally filtered. Additionally, they offer a fault status output that is asserted during over-current and thermal shutdown conditions. These outputs should be connected to the corresponding Qseven® module's USB over-current sense signals.

Simple resettable PolySwitch devices are capable of fulfilling the requirements of USB over-current protection and therefore can be used as a replacement for power distribution switches.

3.7.2.5 EMI/ESD Protection

To improve the EMI behavior of the USB interface, a design should include common mode chokes, which have to be placed as close as possible to the USB connector signal pins. Common mode chokes can provide required noise attenuation but they also distort the signal quality of full-speed and high-speed signaling. Therefore, common mode chokes should be chosen carefully to meet the requirements of the EMI noise filtering while retaining the integrity of the USB signals on the carrier board design.

To protect the USB host interface of the module from over-voltage caused by electrostatic discharge (ESD) and electrical fast transients (EFT), it is highly recommended to use low capacitance steering diodes and transient voltage suppression diodes that must be implemented on the carrier board (for example SR05 RailClamp®' surge rated diode arrays from Semtech, http://semtech.com).

3.7.2.6 USB Client Considerations

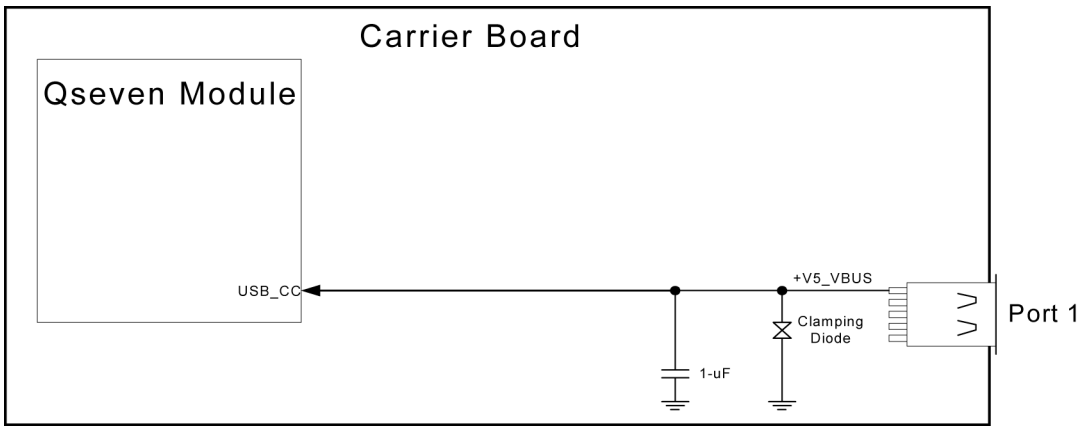
Precautions at the carrier board level must be taken to protect against voltage spikes

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and ESD to ensure robust operation of the host detection circuitry after multiple connect/disconnect events. A clamping diode may be used to minimize ESD, and a bulk capacitor should be placed on +5V USB client rail to avoid excessive voltage spikes.

Level Shifter removed for Qseven Specification 2.0 – please check for compatibility with old 1.2 designs

Figure 3-21 USB Client Connect Protection



NOTE:

In the errata sheet 1 for the Qseven Specification Rev 2.0 the USB_CC signal is redefined to be the USB_VBUS signal. So there is no level shifter circuit needed on the USB_CC signal. The module's USB_VBUS input is directly connected to the +5V Vbus Signal on the connector on the carrier board.

3.7.3 Routing Considerations for USB

See section 4 of this document for trace routing guidelines and the Qseven® specification for more information about this subject.

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3.8 SDIO Interface

SDIO (Secure Digital I/O) provides an easy to implement solution for high-speed data I/O combined with low power consumption. SDIO cards are fully compatible with SD memory cards. This includes mechanical, electrical, power, signaling and software compatibility. SDIO hosts are able to drive SD cards and MMC (MultiMediaCards) as well as SDIO cards that provide functions such as Ethernet or WLAN, GPS receivers, Bluetooth, modems etc.

The Qseven® specification defines one optional 8-bit SDIO interface on the module.

3.8.1 SDIO Interface Signals Definition

Table 3-20 Signal Definition SDIO

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
SDIO_CD#	43	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	CMOS 3.3V		I/O
SDIO_CLK	42	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.	CMOS 3.3V		O
SDIO_CMD	45	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	CMOS 3.3V OD/PP		I/O
SDIO_LED	44	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.	CMOS 3.3V	max 1 mA	O
SDIO_WP	46	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	CMOS 3.3V		I/O
SDIO_PWR#	47	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	CMOS 3.3V		O
SDIO_DAT0-7	48 to 55	SDIO Data lines. These signals operate in push-pull mode.	CMOS 3.3V PP		I/O

Note

If the SDIO presence LED is located on the carrier board a pulldown resistor is required on the carrier board

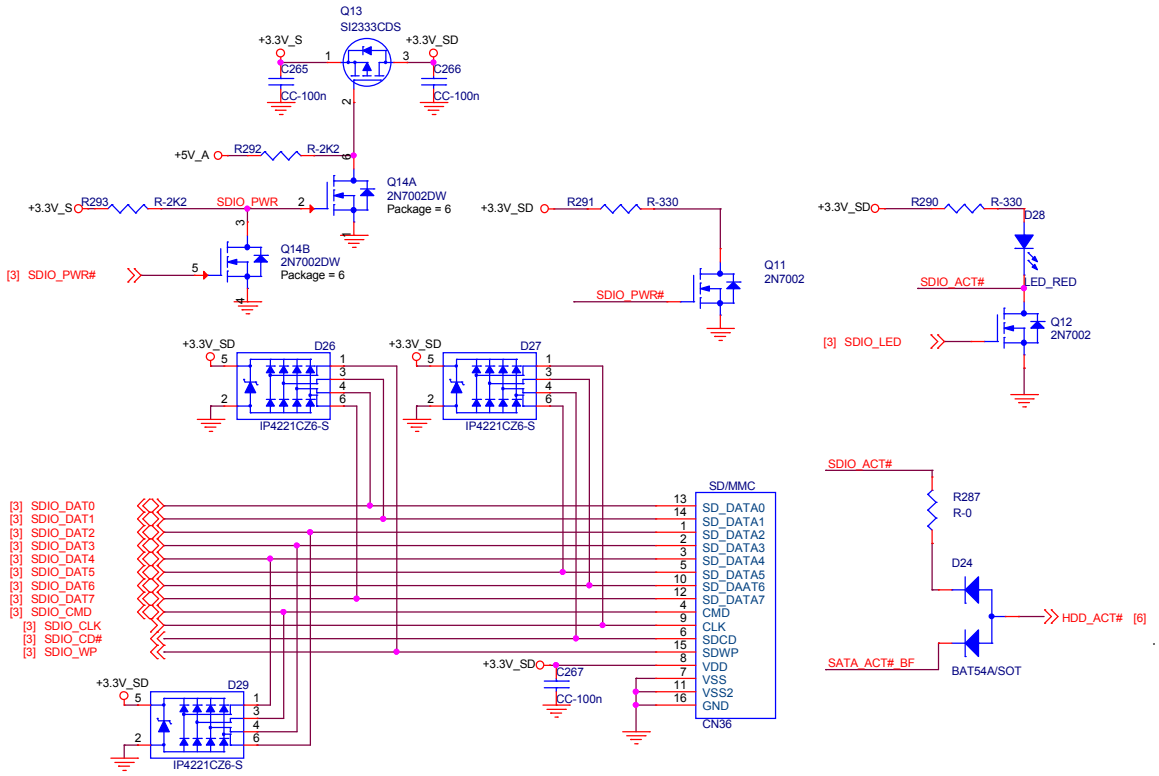
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3.8.2 SDIO Card Implementation Example

The example below shows an SDIO interface as implemented in the Qseven V2.0 reference carrier board.

Figure 3-22 Example for SDIO Card Implementation



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3.9 High Definition Audio / AC97 / I²S Audio Signals

Since Version 2.0Qseven® modules support either High Definition Audio (HDA), AC'97 or I²S for implementing audio functionality.

3.9.1 High Definition Audio / AC97 / I²S Audio Signals Definitions

Table 3-21 Signal Definition HDA

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
HDA_RST#	61	HD Audio/AC'97/I²S Codec Reset.	CMOS 3.3V		O
HDA_SYNC	59	Serial Bus Synchronization.	CMOS 3.3V		O
HDA_BITCLK	63	HD Audio/AC'97/I²S 24 MHz Serial Bit Clock from Codec.	CMOS 3.3V		O
HDA_SDO	67	HD Audio/AC'97/I²S Serial Data Output to Codec.	CMOS 3.3V		O
HDA_SDI	65	HD Audio/AC'97/I²S Serial Data Input from Codec.	CMOS 3.3V		I/O

Note

I/O Orientation:
Input denotes a signal flow to the module and output denotes a signal flow from the module.

The High Definition Audio interface found on the Qseven® module complies with Intel® High Definition Audio Specification 1.0.

HD Audio is primarily intended for use with x86 products. ARM based products normally do not provide any HDA.
Please see Section 3.9.2.2 for I²S Implementation and Section 3.9.2.3 for AC97 implementation examples.

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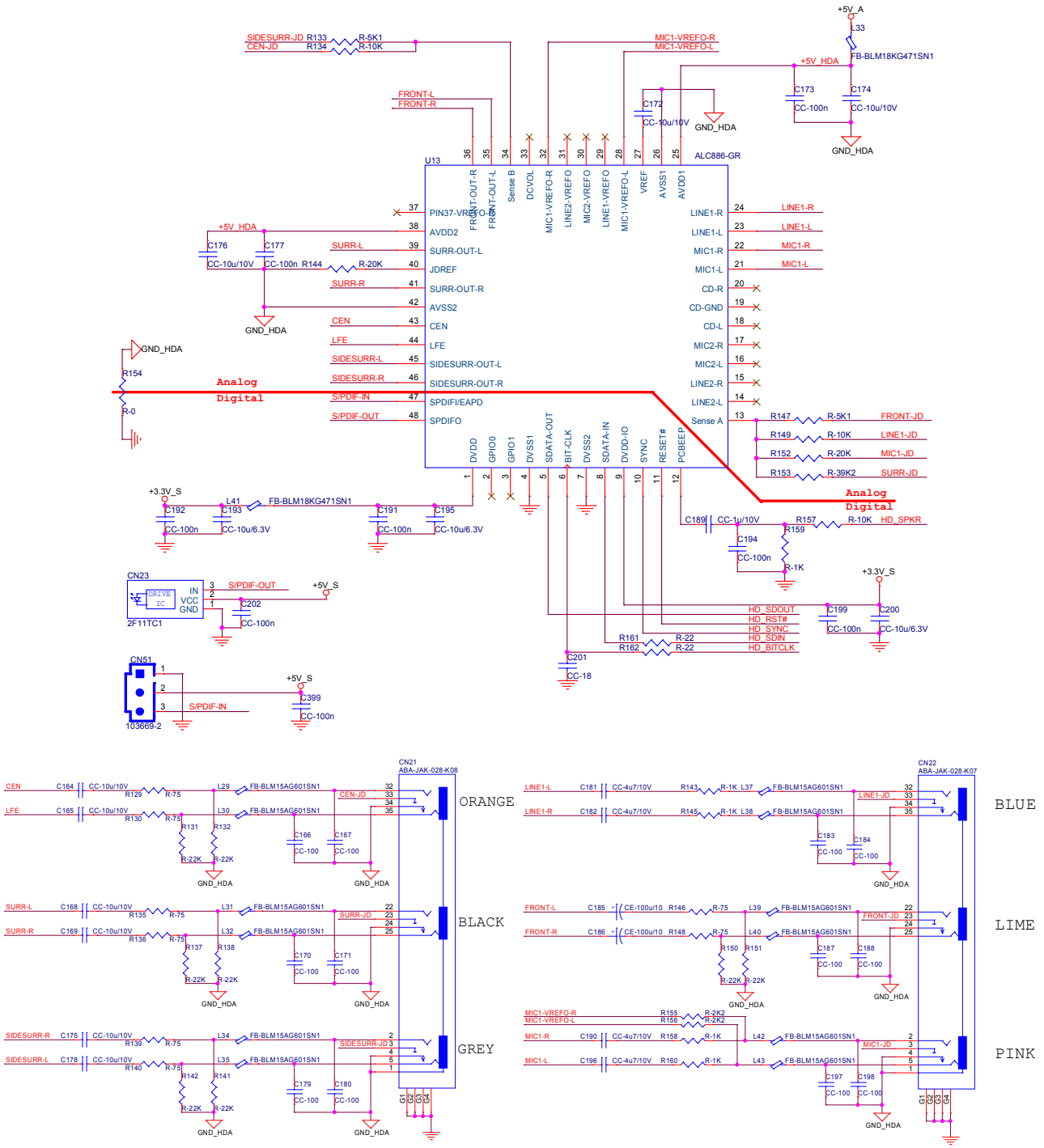
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3.9.2 High Definition Audio / AC97 / I²S Guidelines / Examples

3.9.2.1 HDA Implementation Example

The example in Figure 3-23 shows the implementation of the Realtek ALC 886 HDA Codec (http://www.realtek.com.tw). This HDA Codec is used on the Qseven® V2.0 evaluation carrier board.

Figure 3-23 HDA Codec Reference Schematics



3.9.2.2 I²S Implementation Example

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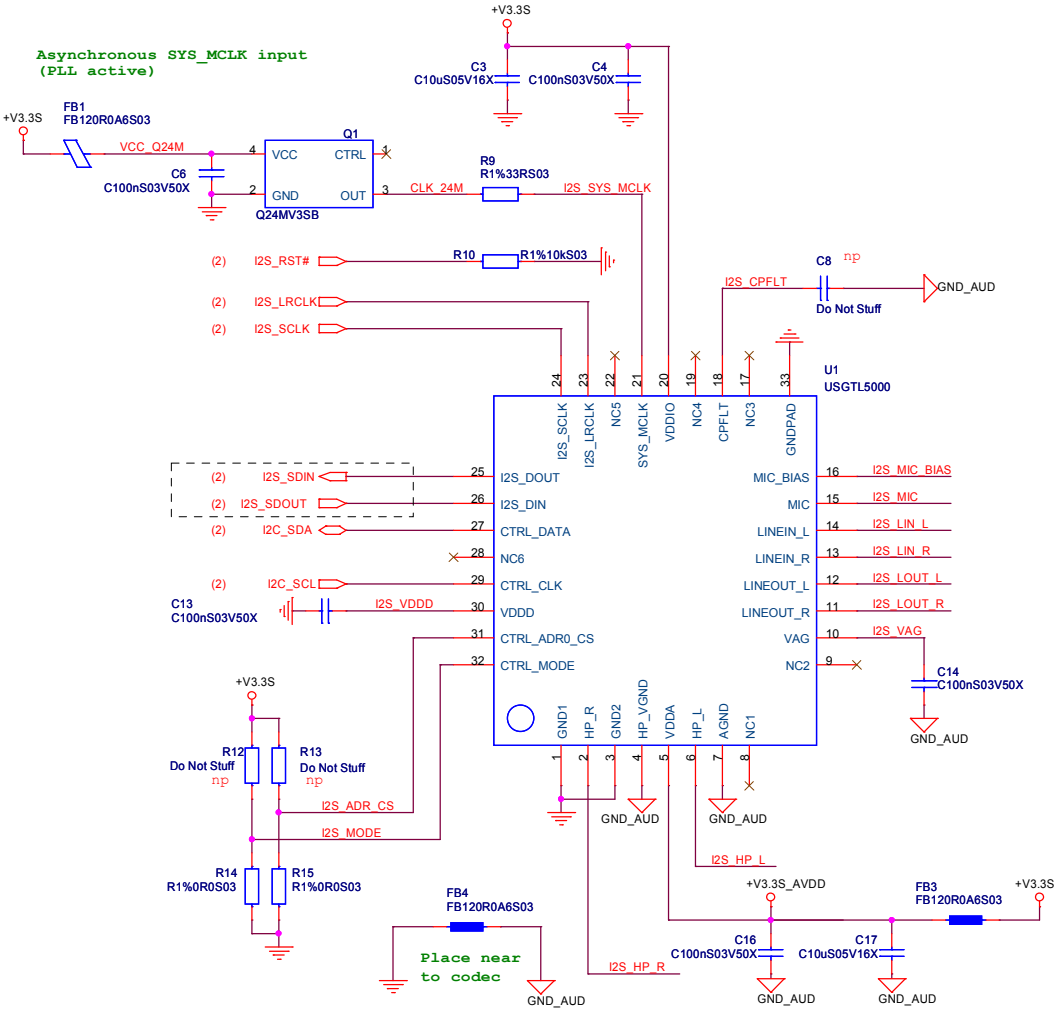
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Note

The Qseven® V2.0 evaluation carrier board supports an onboard HDA solution and an Audio card interface only. The following I2S Codec Reference schematic has been verified with an external I2S Audio card, available as an option with the reference platform.

The example in Figure 3-24 shows the implementation with a Freescale SGTL5000 I2S Codec (http://www.freescale.com). This HDA Codec has been verified with the Qseven® V2.0 evaluation carrier board.

Figure 3-24 I²S Codec Reference Schematics



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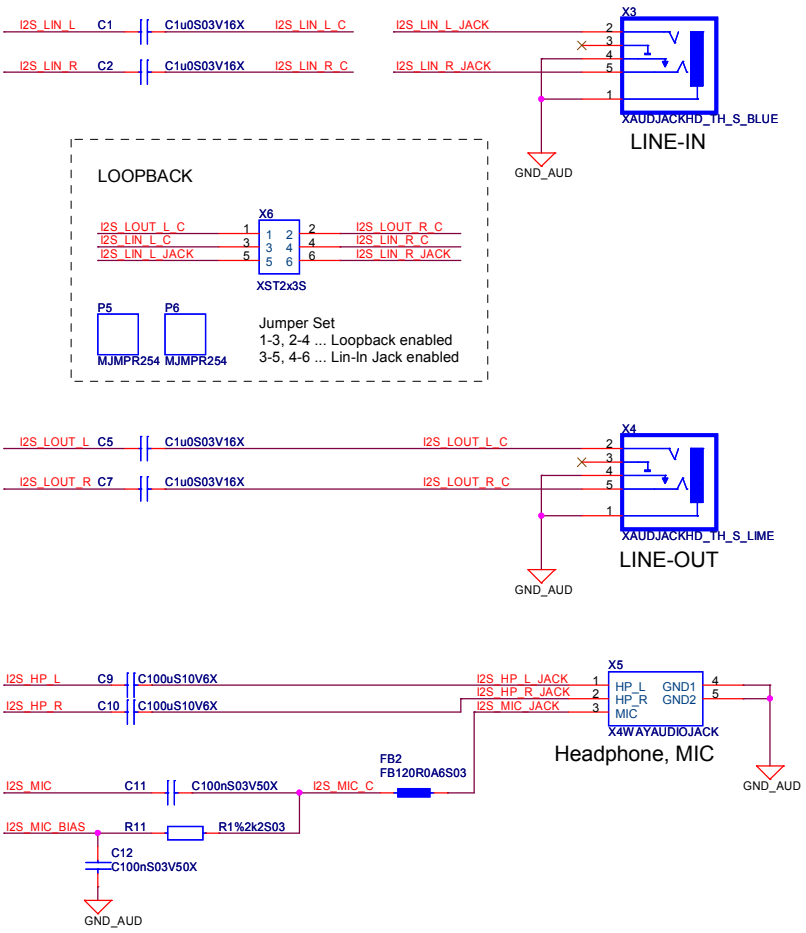
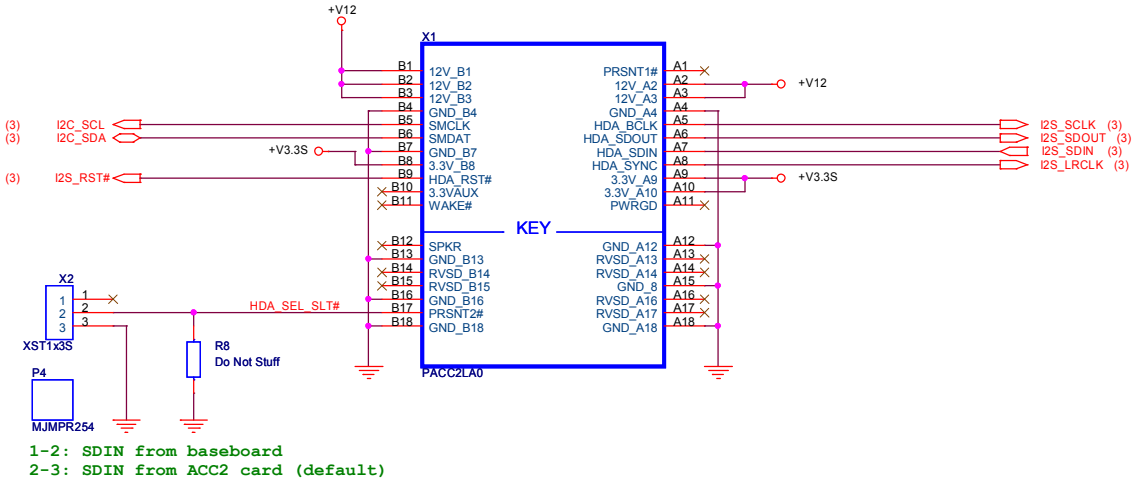


Figure 3-25 External I²S Audio Card Connectors Reference Schematics



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3.9.2.3 AC97 Implementation Example

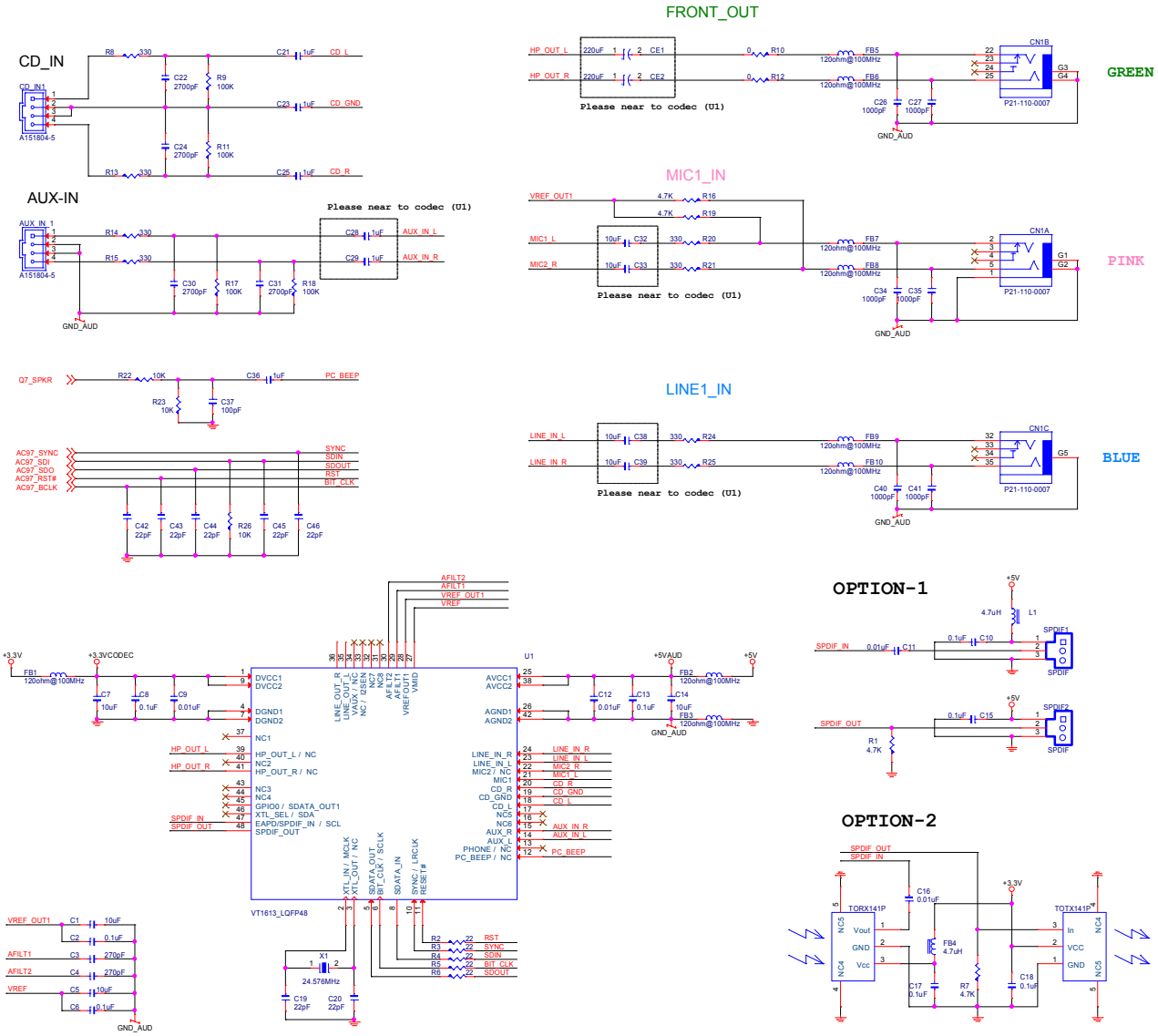
Note

The Qseven® V2.0 evaluation carrier board supports an onboard HDA solution and an Audio card interface only. The following AC97 Codec Reference schematic has not been verified with this board.

The example in Figure 3-26 shows the implementation of the VIA technologies VT 1613 AC97 Codec Chip (http://www.via.com.tw) as used on the Qseven® V1.2 evaluation carrier board.

There are two options for digital input/output:
Option 1 supports coaxial S/PDIF input/output.
Option 2 supports optical S/PDIF (Toslink) input/output.

Figure 3-26 AC97 Codec Reference Schematics



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3.9.3 HDA / AC97 / I2S Placement and Routing Guidelines

The implementation of proper component placement and routing techniques will help to ensure that the maximum performance available from the codec is achieved. Routing techniques that should be observed include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes from the rest of the carrier board. This includes split planes and the proper routing of signals not associated with the audio section.

The following is a list of basic recommendations:

- Traces must be routed with a target impedance of 55Ω with an allowed tolerance of ± 15%.
- Ground return paths for the analog signals must be given special consideration.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Locate the analog and digital signals as far as possible from each other.
- Partition the carrier board with all analog components grouped together in one area and all digital components in another.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Provide separate analog and digital ground planes with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Route analog power and signal traces over the analog ground plane.
- Route digital power and signal traces over the digital ground plane.
- Position the bypassing and decoupling capacitors close to the IC pins, or position the capacitors for the shortest connections to pins, with wide traces to reduce impedance.
- Do not completely isolate the analog/audio ground plane from the rest of the carrier board ground plane. Provide a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main carrier board ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.

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3.10 LVDS Flat Panel Signals

The Qseven® 2.0 specification defines a LVDS flat panel interface that optionally supports up to two 24-bit LVDS channels. It permits dual pixel, two channel data transmission between the host and flat panel display. Each LVDS channel consists of up to five LVDS signal pairs transmitting a serial bit stream directly to a LVDS flat panel or to an external LVDS receiver. Additional control signals, as well as a dedicated I²C bus interface, are specified to control flat panel attributes. This dedicated I²C bus can be used to connect an external I²C EEPROM containing the specific timing data of the flat panel display.

Note

1. *Some LVDS Signal Pins share signals with eDP since Version 2.0*
2. *eDP is a new standard for internal display interfaces.*

3.10.1 LVDS Flat Panel Interface Signals

Table 3-22 LVDS Signals

Signal	Shared with	Pin #	Description	I/O Type (Signal)	I_{OL}/I_{IL}	I/O
LVDS_PPEN		111	Controls panel power enable.	CMOS 3.3V	max 1mA	O
LVDS_BLEN		112	Controls panel backlight enable.	CMOS 3.3V	max 1mA	O
LVDS_BLT_CTRL	GP_PWM_OUT0	123	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this purpose it can be used as General Purpose PWM Output.	CMOS 3.3V		O
LVDS_A0+ LVDS_A0-	eDP0_TX0+ eDP0_TX0-	99 101	LVDS primary channel differential pair 0.	LVDS		O
LVDS_A1+ LVDS_A1-	eDP0_TX1+ eDP0_TX1-	103 105	LVDS primary channel differential pair 1.	LVDS		O
LVDS_A2+ LVDS_A2-	eDP0_TX2+ eDP0_TX2-	107 109	LVDS primary channel differential pair 2.	LVDS		O
LVDS_A3+ LVDS_A3-	eDP0_TX3+ eDP0_TX3-	113 115	LVDS primary channel differential pair 3.	LVDS		O
LVDS_A_CLK+ LVDS_A_CLK-	eDP0_AUX+ eDP0_AUX-	119 121	LVDS primary channel differential pair clock lines.	LVDS		O
LVDS_B0+ LVDS_B0-	eDP1_TX0+ eDP1_TX0-	100 102	LVDS secondary channel differential pair 0.	LVDS		O
LVDS_B1+ LVDS_B1-	eDP1_TX1+ eDP1_TX1-	104 106	LVDS secondary channel differential pair 1.	LVDS		O
LVDS_B2+ LVDS_B2-	eDP1_TX2+ eDP1_TX2-	108 110	LVDS secondary channel differential pair 2.	LVDS		O
LVDS_B3+ LVDS_B3-	eDP1_TX3+ eDP1_TX3-	114 116	LVDS secondary channel differential pair 3.	LVDS		O
LVDS_B_CLK+ LVDS_B_CLK-	eDP1_AUX+ eDP1_AUX-	120 122	LVDS secondary channel differential pair clock lines.	LVDS		O
LVDS_DID_CLK	GP_I2C_CLK	127	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If primary functionality is not used it can be used as General Purpose I²C bus clock line.	CMOS 3.3V OD		O

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Signal	Shared with	Pin #	Description	I/O Type (Signal)	I_{OL}/I_{IL}	I/O
LVDS_DID_DAT	GP_I2C_DAT	125	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If primary functionality is not used it can be used as General Purpose I²C bus data line.	CMOS 3.3V OD		I/O
LVDS_BLC_CLK	eDP1_HPD#	128	Control clock signal for external SSC clock chip.	CMOS 3.3V OD		I/O
LVDS_BLC_DAT	eDP0_HPD#	126	Control data signal for external SSC clock chip.	CMOS 3.3V OD		I/O

Note

1. ALL pull ups/downs are to be on the module.

2. The LVDS flat panel configuration within the BIOS of the Qseven® module shall be implemented in accordance to the DisplayID specification from the Video Electronics Standards Association (VESA). For more information about the LVDS flat panel configuration with DisplayID refer to the specification 'Display Identification Data (DisplayID) Structure Version 1.0' that is available on the web page of the Video Electronics Standards Association (VESA).

3.10.2 LVDS Implementation Guidelines

Many carrier board designs do not need the full range of LVDS performance offered by Qseven® modules. It depends on the flat panel configuration of the Qseven® module, as well as the carrier board design, as to how many LVDS signal pairs are supported. While the dual channel 24-bit LVDS configuration needs all 10 LVDS signal pairs, a single channel 18-bit LVDS configuration only requires 4 LVDS signal pairs. In this case all unused LVDS signal pairs should be left open on the carrier board.

If the LVDS display interface of the Qseven® module is not implemented, all signals associated with this interface should be left open.

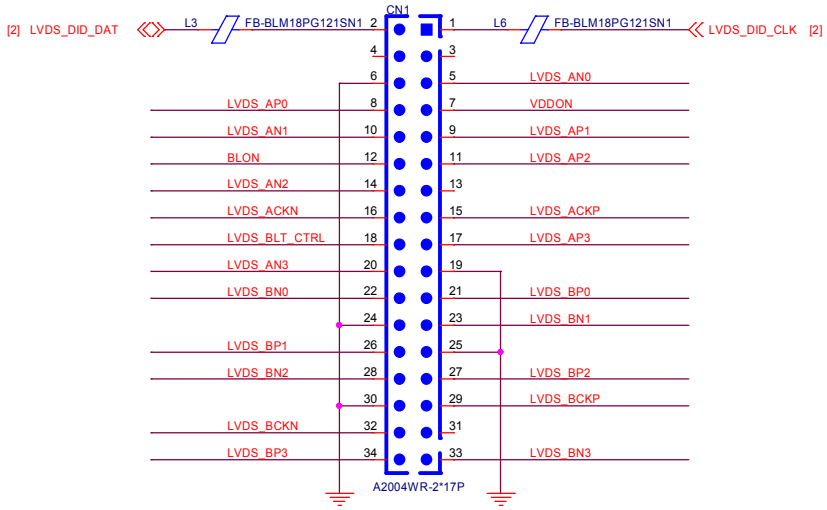
3.10.2.1 Connector and Cable Considerations

The SGeT e.V. doesn't define the connector layout for interfacing LVDS on the Qseven® carrier board design. It is up to the system designer and the system requirements as to which connectors and which pinout will be used for the application. The following example in Figure 3-27 is taken from the Qseven® V2.0 Reference Carrier Board and should only be considered as an example of how to implement the LVDS interface on the carrier board.

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Figure 3-27 LVDS Connector



When implementing LVDS signal pairs on a single-ended carrier board connector, the signals of a pair should be arranged so that the positive and negative signal are side by side. The trace lengths of the LVDS signal pairs between the Qseven® module and the connector on the carrier board should be the same when possible. Additionally, one or more ground traces/pins must be placed between the LVDS pairs.

Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode noise, which is rejected by the receiver.

Twisted pair cables provide a low-cost solution with good balance and flexibility. They are capable of medium to long runs depending upon the application skew budget. A variety of shielding options are available.

Ribbon cables are a cost effective and easy solution. Even though they are not well suited for high-speed differential signaling they do work fine for very short runs. Most cables will work effectively for cable distances of <0.5m.

The cables and connectors that are to be utilized should have a differential impedance of 100Ω ±15%. They should not introduce major impedance discontinuities that cause signal reflections.

For more information about this subject refer to the 'LVDS Owners Manual Chapter 6' available from Texas Instruments (http://www.ti.com).

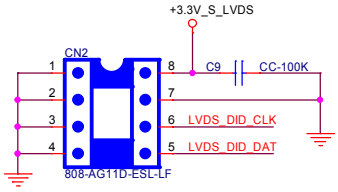
3.10.2.2 Display Timing Configuration

Usually the timing parameters for the flat panel display are stored in an external EEPROM that is implemented on the Qseven V2.0 Reference Carrier Board. It is accessible through the dedicated LVDS I²C bus via the signals *'LVDS_DID_CLK'* and *'LVDS_DID_DAT',* which can be found on the module's connector (pin 125 resp. pin 127). During POST the module's BIOS reads out the display timing data from the EEPROM and configures the module's graphics controller for proper flat panel operation. In order to be able to do this, the device address of the LVDS I²C EEPROM must be strapped to 0xA0.

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For more information about the LVDS flat panel configuration with DisplayID refer to the specification 'Display Identification Data (DisplayID) Structure Version 1.0' that is available on the webpage of the Video Electronics Standards Association (VESA) (http://www.vesa.org).

Figure 3-28 LVDS I²C EEPROM



Note

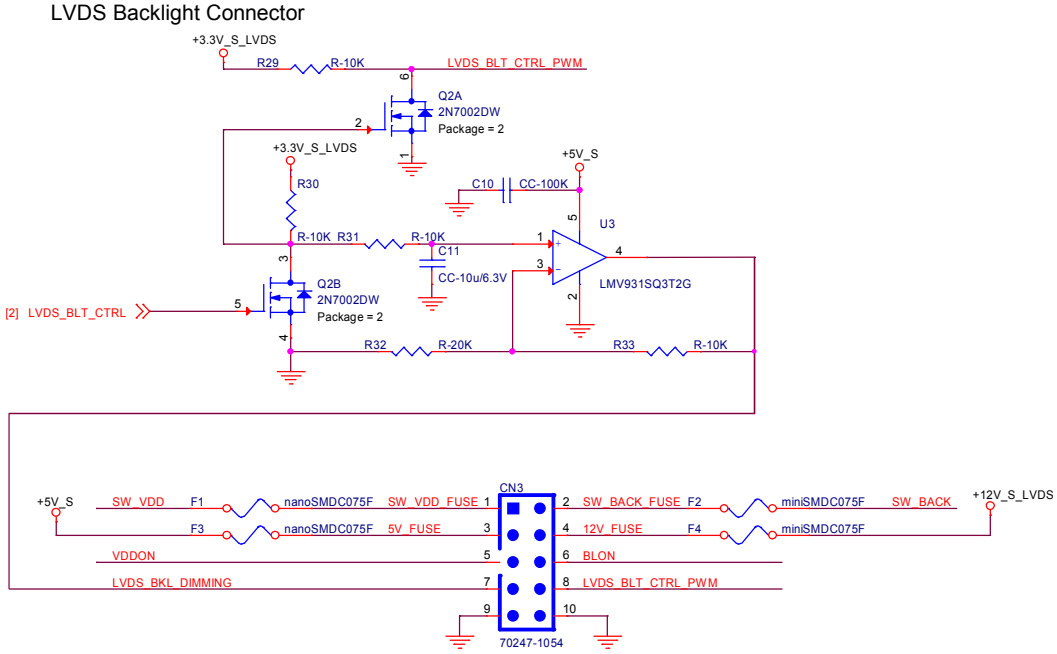
Required pull ups/downs are integrated on the module.

3.10.2.3 Backlight Control

The following LVDS reference circuitry shows a backlight control solution . The signal level of the signals coming from the module must be adapted to the specified level of the used devices. In the example used on the Qseven V2.0 Reference Carrier Board the signals LVDS_BLT_CTRL , LVDS_DID_DAT and LVDS_DID_CLK can level shifted by using the Backlight Logic Voltage Selection shown in Figure 3-29. The backlight supply voltage selection shown in the same figure allows adaption of the backlight supply voltage VDD to 5V or 12V

Backlight control is part of the EAPI (Embedded Application Programmer Interface) API and can be accessed by using the 32bit API functions. For more details about EAPI refer to the Qseven specification and the module vendor's EAPI Programmers Guide.

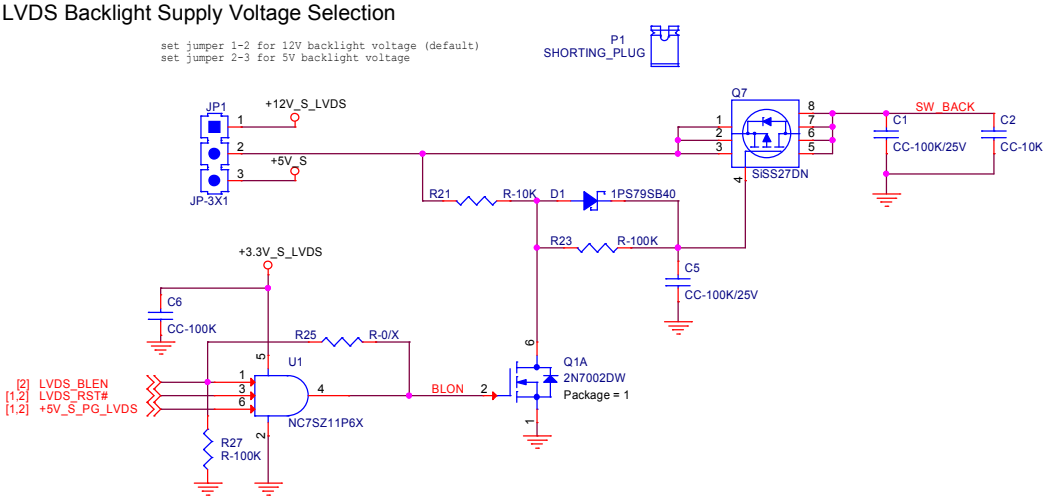
Figure 3-29 LVDS Backlight and Panel Supply Voltage Control Circuitry



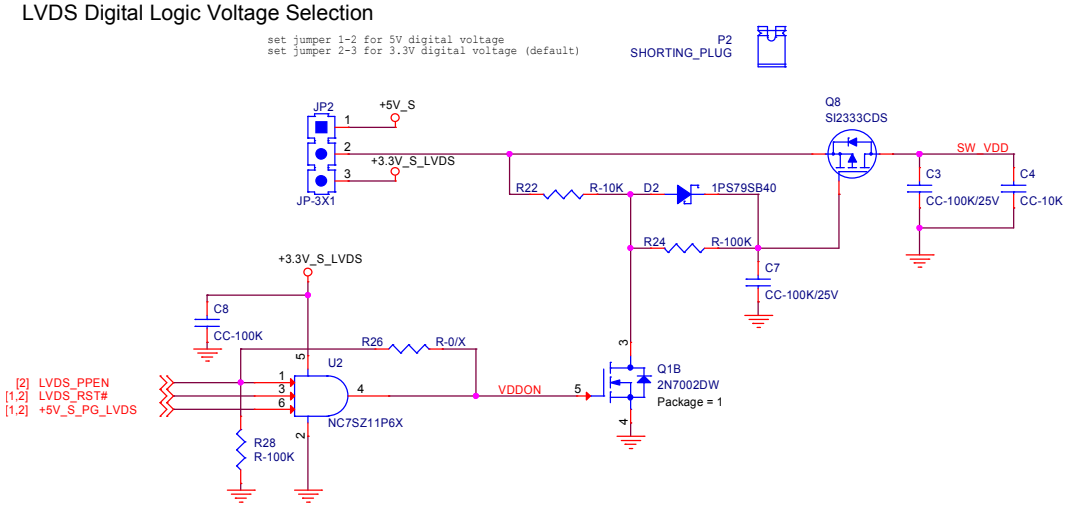
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LVDS Backlight Supply Voltage Selection



LVDS Digital Logic Voltage Selection



Note

Displays with LED backlight may use PWM for brightness control.

3.10.3 Routing Considerations for LVDS

See section 4 of this document for trace routing guidelines and the Qseven specification and the 'LVDS Owners Manual Chapter 3' from Texas Instruments (http://www.ti.com) for more information about this subject.

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3.11 Embedded DisplayPort (eDP)

Qseven® Rev 2.0 modules optionally support up to two Embedded DisplayPort (eDP) Version 1.2 interfaces. These interfaces are shared with LVDS signals.

eDP is an open, industry standard digital display interface that is under development within the Video Electronics Standards Association (VESA). The eDP specification defines a scalable digital display interface. It defines a license-free, royalty-free, state-of-the-art digital video interconnect intended to be used primarily between a computer and its internal display(s). The eDP interface supports 1, 2, or 4 data pairs that carry the video signal and embeds the clock in the data signal. The eDP interface is designed to replace LVDS as an internal Graphics interface in the coming years. Benefits are embedded clock, higher data rates and less data lines than with LVDS. EDP support is offered by ARM and x86 processor based platforms, depending on the selected processor. AC coupling is provided on the module. If the eDP display interface of the Qseven® module is not implemented, all signals associated with this interface should be left open.

3.11.1 eDP Interface Signals

Table 3-23 Embedded DisplayPort Signals

Signal	Shared with	Pin#	Description	I/O Type (Signal)	I_{OL}/I_{IL}	I/O
eDP0_TX0+ eDP0_TX0-	LVDS_A0+ LVDS_A0-	99 101	eDP primary channel differential pair Lane 0.	PCIe		O
eDP0_TX1+ eDP0_TX1-	LVDS_A1+ LVDS_A1-	103 105	eDP primary channel differential pair Lane 1.	PCIe		O
eDP0_TX2+ eDP0_TX2-	LVDS_A2+ LVDS_A2-	107 109	eDP primary channel differential pair Lane 2.	PCIe		O
eDP0_TX3+ eDP0_TX3-	LVDS_A3+ LVDS_A3-	113 115	eDP primary channel differential pair Lane 3.	PCIe		O
eDP0_AUX+ eDP0_AUX-	LVDS_A_CLK+ LVDS_A_CLK-	119 121	eDP primary channel differential pair Auxiliary Channel used for link management and device control.	PCIe		I/O
eDP0_HPD#	LVDS_BLC_DAT	126	eDP primary channel Hot Plug Detect.	CMOS 3.3V OD		I
eDP1_TX0+ eDP1_TX0-	LVDS_B0+ LVDS_B0-	100 102	eDP secondary channel differential pair Lane 0.	PCIe		O
eDP1_TX1+ eDP1_TX1-	LVDS_B1+ LVDS_B1-	104 106	eDP secondary channel differential pair Lane 1.	PCIe		O
eDP1_TX2+ eDP1_TX2-	LVDS_B2+ LVDS_B2-	108 110	eDP secondary channel differential pair Lane 2.	PCIe		O
eDP1_TX3+ eDP1_TX3-	LVDS_B3+ LVDS_B3-	114 116	eDP secondary channel differential pair Lane 3.	PCIe		O
eDP1_AUX+ eDP1_AUX-	LVDS_B_CLK+ LVDS_B_CLK-	120 122	eDP secondary channel differential pair Auxiliary Channel used for link management and device control.	PCIe		I/O
eDP1_HPD#	LVDS_BLC_CLK	128	eDP secondary channel Hot Plug Detect.	CMOS 3.3V OD		I

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3.11.2 eDP Implementation Guidelines

Many carrier board designs do not need the full range of eDP performance offered by Qseven® modules. It depends on the flat panel configuration of the Qseven® module, as well as the carrier board design, as to how many eDP lanes are supported. In this case all unused eDP signal lanes should be left open on the carrier board. If the eDP display interface of the Qseven® module is not implemented at all, non-shared signals associated with this interface should be left open.

3.11.2.1 Connector and Cable Considerations

The SGeT e.V. doesn't define the connector layout for interfacing eDP on the Qseven carrier board design. It is up to the system designer and the system requirements as to which connectors and which pinout will be used for the application. The following examples in Table 3-24 and Table 3-25 are taken from the Qseven® V2.0 Reference Carrier Board and should only be considered as an example of how to implement the eDP interface on the carrier board. However it is recommended to follow the VESA guidelines for eDP connectors. The examples below implement up to 2 lanes (30 pin) and up to 4 lanes (40 pin).

Table 3-24 Pinout Embedded DisplayPort Connector (eDP) 30 Pin on Baseboard

Pin#	Signal	Description	Pin#	Signal	Description
1	n/c	Rsvd. for LCD Manufacturer's Use	2	BACK	Backlight Power (5V or 12V)
3	BACK	Backlight Power (5V or 12V)	4	BACK	Backlight Power (5V or 12V)
5	BACK	Backlight Power (5V or 12V)	6	n/c	Rsvd. for LCD Manufacturer's Use
7	n/c	Rsvd. for LCD Manufacturer's Use	8	eDP_BLT_CTRL	Backlight PWM Dimming Control*
9	BLON_eDP	Backlight enable (on/off)*	10	GND	Backlight Ground
11	GND	Backlight Ground	12	GND	Backlight Ground
13	GND	Backlight Ground	14	eDP_HPD#	Hot Plug Detect
15	GND	Logic Ground	16	GND	Logic Ground
17	n/c	LCD Self Test Enable*	18	VDD_eDP	Logic Power (3.3V or 5V)
19	VDD_eDP	Logic Power (3.3V or 5V)	20	GND	Signal Ground
21	DP_AUX-	Auxiliary Channel (negative)	22	DP_AUX+	Auxiliary Channel (positive)
23	GND	Signal Ground	24	eDP_TX0+	eDP Lane 0 (positive)
25	eDP_TX0-	eDP Lane 0 (negative)	26	GND	Signal Ground
27	eDP_TX1+	eDP Lane 1 (positive)	28	eDP_TX1-	EDP Lane 1 (negative)
29	GND	Signal Ground	30	n/c	Rsvd. for LCD Manufacturer's Use

* denotes optional signals

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Table 3-25 Pinout Embedded DisplayPort Connector (eDP) 40 Pin on Baseboard

Pin#	Signal	Description	Pin#	Signal	Description
1	n/c	Rsvd. for LCD Manufacturer's Use	2	BACK	Backlight Power (5V or 12V)
3	BACK	Backlight Power (5V or 12V)	4	BACK	Backlight Power (5V or 12V)
5	BACK	Backlight Power (5V or 12V)	6	n/c	Rsvd. for LCD Manufacturer's Use
7	n/c	Rsvd. for LCD Manufacturer's Use	8	eDP_BLT_CTRL	Backlight PWM Dimming Control*
9	BLON_eDP	Backlight enable (on/off)*	10	GND	Backlight Ground
11	GND	Backlight Ground	12	GND	Backlight Ground
13	GND	Backlight Ground	14	eDP_HPD#	Hot Plug Detect
15	GND	Logic Ground	16	GND	Logic Ground
17	GND	Logic Ground	18	GND	Logic Ground
19	n/c	LCD Self Test Enable*	20	VDD_eDP	Logic Power (3.3V or 5V)
21	VDD_eDP	Logic Power (3.3V or 5V)	22	VDD_eDP	Logic Power (3.3V or 5V)
23	VDD_eDP	Logic Power (3.3V or 5V)	24	GND	Signal Ground
25	DP_AUX-	Auxiliary Channel (negative)	26	DP_AUX+	Auxiliary Channel (positive)
27	GND	Signal Ground	28	eDP_TX0+	eDP Lane 0 (positive)
29	eDP_TX0-	eDP Lane 0 (negative)	30	GND	Signal Ground
31	eDP_TX1+	eDP Lane 1 (positive)	32	eDP_TX1-	eDP Lane 1 (negative)
33	GND	Signal Ground	34	eDP_TX2+	eDP Lane 2 (positive)
35	eDP_TX2-	EDP Lane 2 (negative)	36	GND	Signal Ground
37	eDP_TX3+	eDP Lane 3 (positive)	38	eDP_TX3-	EDP Lane 3 (negative)
39	GND	Signal Ground	40	n/c	Rsvd. for LCD Manufacturer's Use

* denotes optional signals

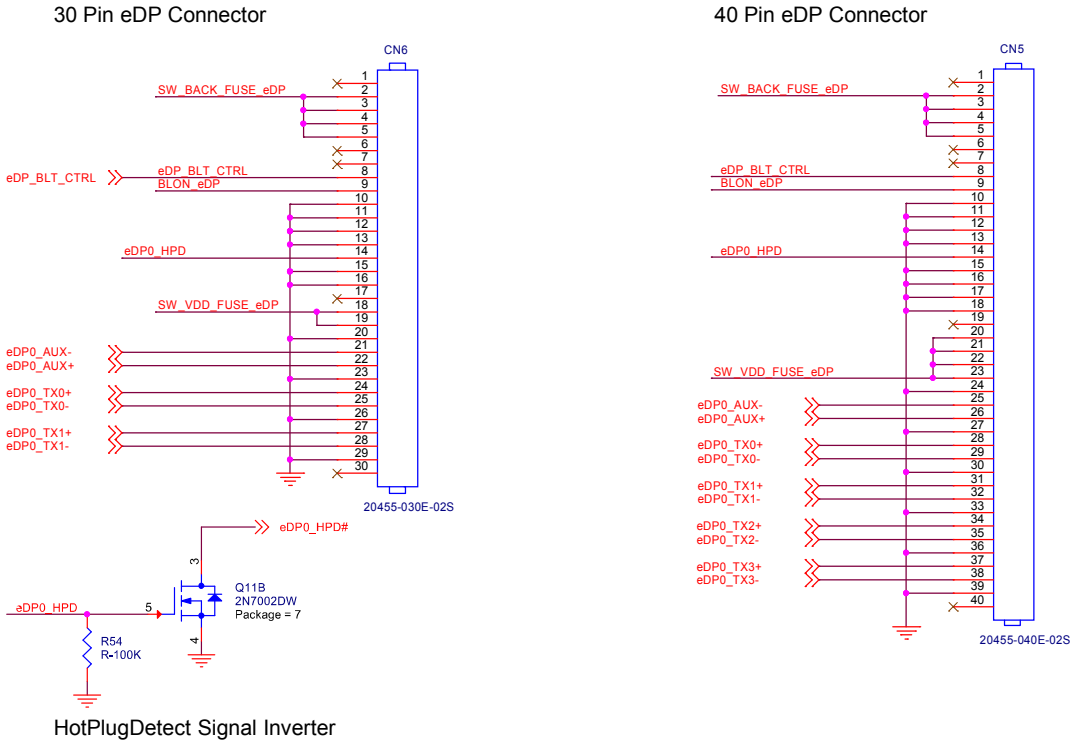
Note

1. *As the VESA Guidelines for the pin out of the eDP Connector refers to the panel connector the signal numbering of the connector on the baseboard appears in reverse order.*
2. *Depending on the Type of FlatPanel Display used an Inverter for the HotPlugDetect signal may be required.*
3. *eDP switches may be used to link both types of connectors (30 pin and 40 pin) to the same eDP channel (primary or secondary).*

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Figure 3-30 eDP Connector and HPD Signal Inverter Schematics



When implementing eDP signal pairs on a single-ended carrier board connector, the signals of a pair should be arranged so that the positive and negative signal are side by side. The trace lengths of the eDP signal pairs must be length matched. Additionally, one or more ground traces/pins must be placed between the eDP pairs.

Balanced cables (twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode noise, which is rejected by the receiver.

Twisted pair cables provide a low-cost solution with good balance and flexibility. They are capable of medium to long runs depending upon the application skew budget. A variety of shielding options are available.

Micro coaxial cables are the first choice to connect eDP devices.

The cables and connectors that are to be utilized should have a differential impedance of 100Ω ±15%. They should not introduce major impedance discontinuities that cause signal reflections.

3.11.2.2 Display Timing

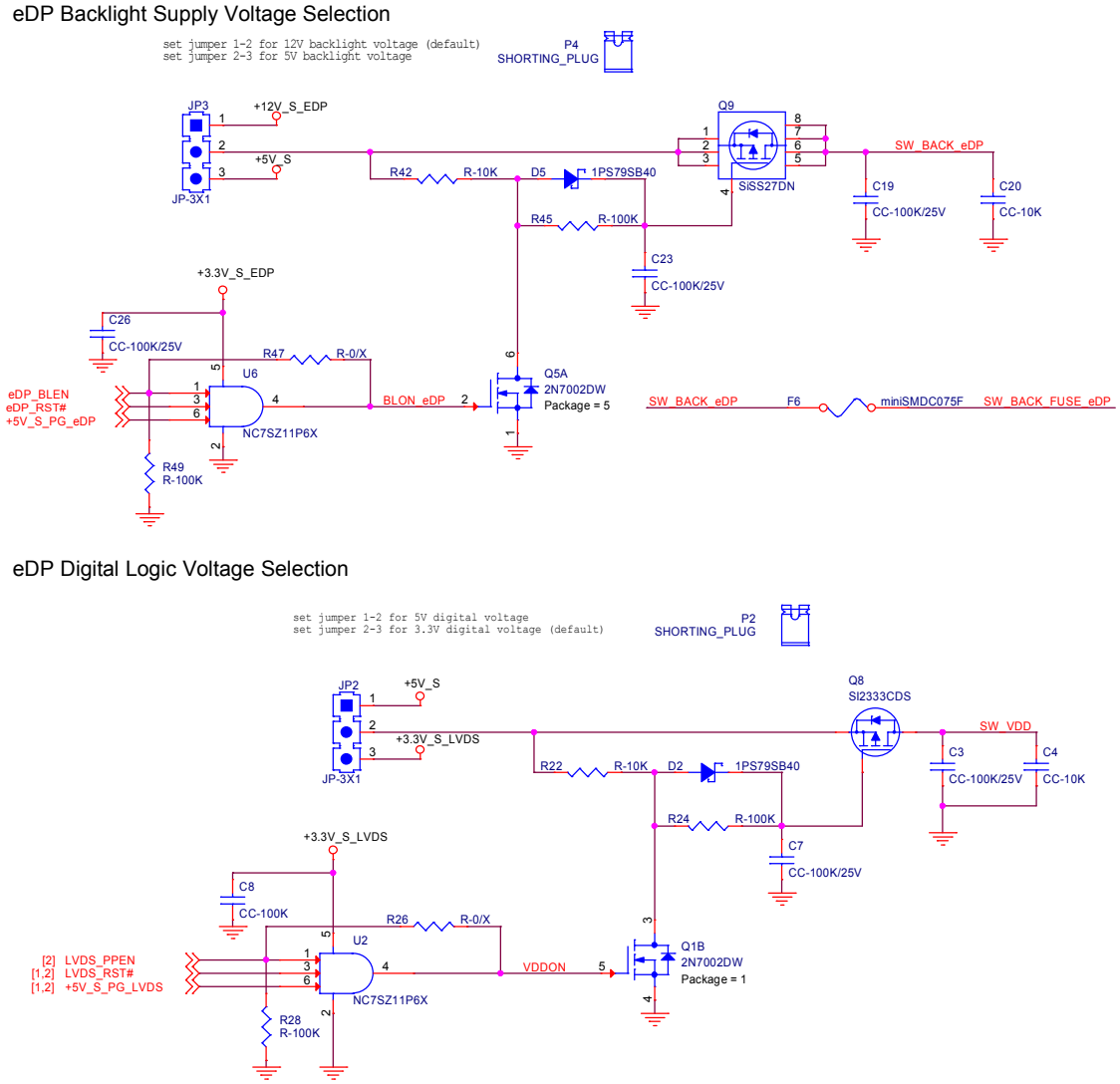
All display timing information (i.e. pixel clock,Hsync, Vsync) and video information (bits-per-pixel, color space, etc.). video data error correction and optional audio data are carried in the eDP main link. EDID information (display format information), link training protocol, display control (from eDP1.2), power management and error checking of main link data (CRC protocol) are carried in the eDP AUX channel.

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3.11.2.3 eDP Backlight and Panel Voltage Control

The following eDP reference circuitry shows a panel Voltage control solution. The signal level of the signals coming from the module must be adapted to the specified signals/voltage level of the used devices on the panel display. In the example shown in Figure 3-31, which is used on the Qseven V2.0 Reference Carrier Board, the supply voltage for the display can be set to 12V or 5V via jumper JP3, and the supply voltage for the digital electronics circuitry can be set to 3.3V or 5V via jumper JP4.

Figure 3-31 eDP Backlight and Panel Voltage Control



3.11.3 Routing Considerations for eDP

Embedded Display Port is based on PCI Express signal technology.

Please see instructions for PCI Express technology in section 4 of this document for trace routing guidelines and the Qseven® specification for more information about this subject.

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3.12 DisplayPort Interface

3.12.1 DisplayPort Interface Signals (from Module)

Qseven® Rev 2.0 modules optionally support one DisplayPort Version 1.2 interface. This interface is shared with TMDS signals.

DisplayPort is an open, industry standard digital display interface that is under development within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect intended to be used primarily between a computer and its display monitor.

The DisplayPort interface supports 1, 2, or 4 data pairs that carry the video signal, clock and optional audio signals. The video signal of the DisplayPort interface is not compatible with DVI or HDMI but a DisplayPort connector can pass these signals through. While DVI and HDMI require separate clock signals, DisplayPort embeds the clock in the data signal. Unlike the separate DVI/HDMI and LVDS standards, DisplayPort supports both external (monitor) or internal (LCD panel) display connections.

Display Port++ (also known as dual-mode DisplayPort) output signals can easily provide the lower voltages required for Display Port using a passive adapter. This enables cost-efficient direct support for single-link HDMI and DVI signals. Dual-mode chipsets are able to detect when a DVI or HDMI passive adapter is connected and then switch to DVI/HDMI mode using the 4-lane main DisplayPort link and the AUX channel link to transmit 3 TMDS signals, clock and display data channel Data and Clock. Dual-mode compatible devices are recognizable by the DP++ logo.

Note

AC coupling is provided on the module for the main link, auxiliary channel needs AC coupling on the carrier board.

DP/DP++ use the same (shared) pins as TMDS to transmit the DP/DP++ graphics signals (see below).

Table 3-26 Signal Definition DisplayPort

Signal	Shared With	Pin#	Description	I/O Type	I_{OL}/I_{IL}	Module I/O
DP_LANE3- DP_LANE3+	TMDS_CLK- TMDS_CLK+	133 131	DisplayPort differential pair lines lane 3.	PCIe		O
DP_LANE2- DP_LANE2+	TMDS_LANE0- TMDS_LANE0+	145 143	DisplayPort differential pair lines lane 2.	PCIe		O
DP_LANE1- DP_LANE1+	TMDS_LANE1- TMDS_LANE1+	139 137	DisplayPort differential pair lines lane 1.	PCIe		O
DP_LANE0- DP_LANE0+	TMDS_LANE2- TMDS_LANE2+	151 149	DisplayPort differential pair lines lane 0.	PCIe		O
DP_AUX- DP_AUX+		140 138	Auxiliary channel used for link management and device control. Differential pair lines.	PCIe		I/O
DP_HPD#		154	Hot plug detection signal that serves as an interrupt request.	CMOS 3.3V		I

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Note

Support of the DisplayPort interface is chipset dependent and therefore may not be available on all Qseven® modules. It is available with most X86 processor technology based modules and some ARM processor technology based modules.

DisplayPort interface signals are shared with the signals for the TMDS interface (SDVO is no longer supported with Qseven V2.0).

DisplayPort

V1.2 introduces a new, HBR2 mode with a higher data rate of 5.4 Gb/s for increased resolutions and refresh rates as well as multiple independent video streams (daisy-chain connection with multiple monitors).

3.12.1.1 DisplayPort Connector Signals

Figure 3-32 DisplayPort Connector

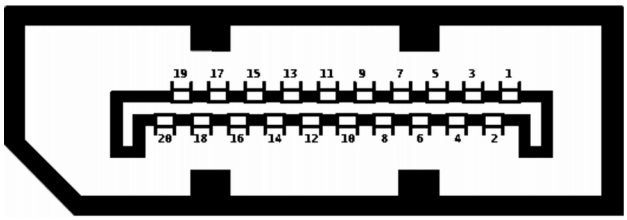


Table 3-27 Pinout DisplayPort Connector

Pin#	Signal	Description	Pin#	Signal	Description
1	DP_LANE0+	DisplayPort Lane 0 (positive)	2	GND	Ground
3	DP_LANE0-	DisplayPort Lane 0 (negative)	4	DP_LANE1+	DisplayPort Lane 1 (positive)
5	GND	Ground	6	DP_LANE1-	DisplayPort Lane 1 (negative)
7	DP_LANE2+	DisplayPort Lane 2 (positive)	8	GND	Ground
9	DP_LANE2-	DisplayPort Lane 2 (negative)	10	DP_LANE3+	DisplayPort Lane 3 (positive)
11	GND	Ground	12	DP_LANE3-	DisplayPort Lane 3 (negative)
13	CONFIG1	Configuration Pin 1 (connected to Ground via 1M resistor)	14	CONFIG2	Configuration Pin 2 (connected to Ground)
15	DP_AUX+	Auxiliary Channel (positive)	16	GND	Ground
17	DP_AUX-	Auxiliary Channel (negative)	18	DP_HPD#	Hot Plug Detect
19	RETURN	Return For Power	20	DP_PWR	Power For Connector

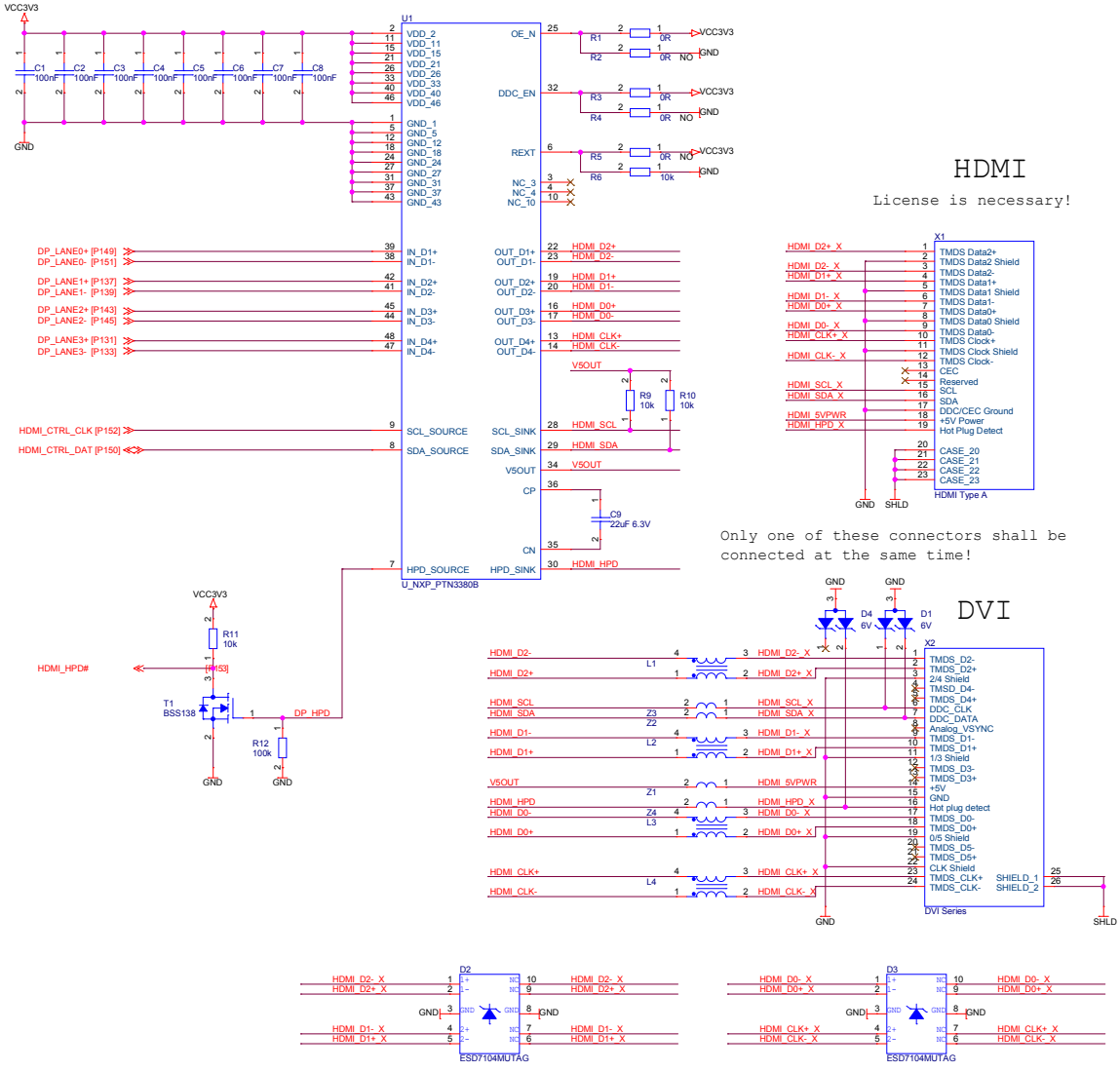
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3.12.2 DP++ to DVI or HDMI Transmitter Reference Circuitry

The following circuitry shows an example of how to connect a NXP PTN3380B active level shifter (http://www.nxp.com) directly to the Qseven® module.
The Qseven V2.0 refernce carrier board is implemented differently. It uses an external graphics adapter does not include an onboard level shifter for external graphics output. For details please see the Qseven V2.0 reference carrier board manual.

Figure 3-33 DP++ to DVI/HDMI Transmitter Reference Circuitry using an active level shifter



Note

1. *Only one of the connectors shown shall be connected at the same time!*
2. *DP++ capabilities are required on the module*
3. *In this example the carrier board supports HDMI and DVI only*

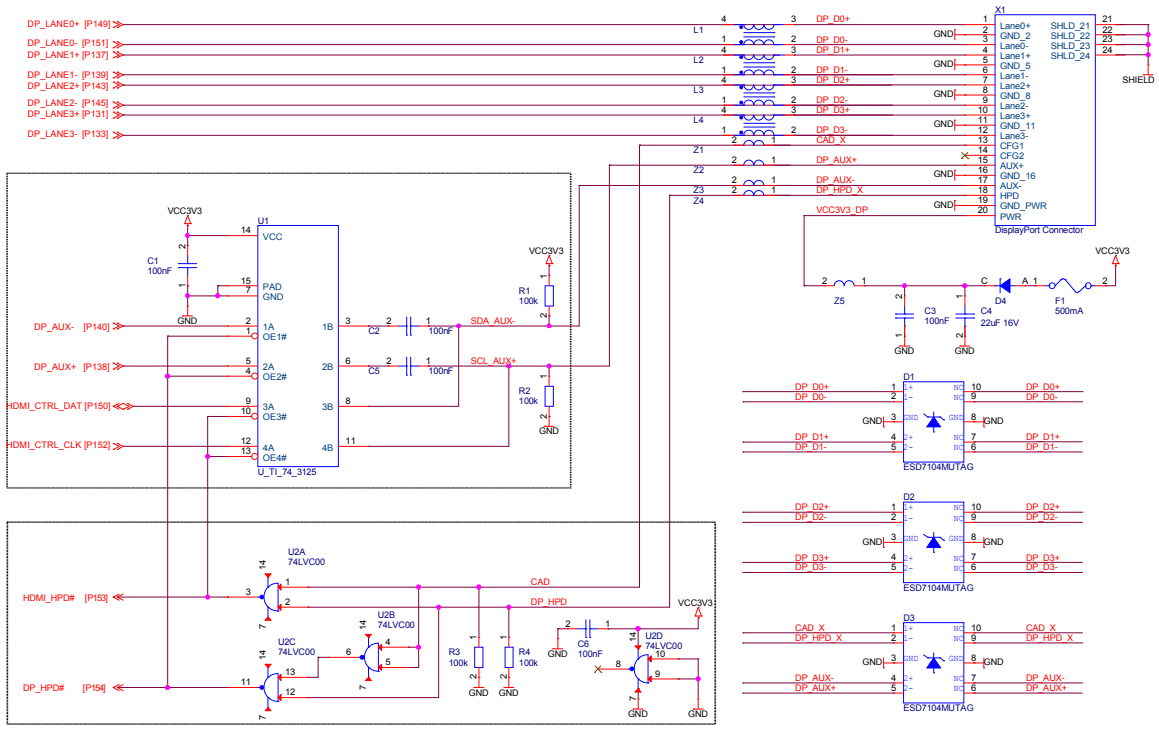
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3.12.2.1 DP++ Transmitter Reference Circuitry

The following circuitry shows an example for a DP/DP++ transmitter circuitry with a direct DisplayPort output. In this implementation the carrier board supports common DP Displays directly, HDMI and DVI via an external cable adapter connected to the DP++ connector. The external cable adapter corresponds to the level shifter in the schematics of Figure 3-33.

Figure 3-34 DP++ to DP Transmitter Reference Circuitry



Note

DP++ capabilities are required on the module.

The Qseven V2.0 reference carrier board is implemented differently. It uses an external graphics adapter and does not include an onboard level shifter for external graphics output. For details please see the Qseven V2.0 reference carrier board manual.

Figure 3-35 Pictures of a DP++ to DVI Level shifter





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3.13 HDMI Interface Signals (from Module)

High-Definition Multimedia Interface (HDMI) is a licenseable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data into TMDS for digital transmission and is fully backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video. Additionally, HDMI adds the ability to send up to 8 separate channels of uncompressed digital audio and auxiliary control data during the horizontal and vertical blanking intervals of the TMDS video stream.

The Qseven® specification defines a single-link HDMI interface with a pixel clock rate of up to 165 MHz. The appropriate TMDS receive and transmit differential signal pair, as well as additional control signals, can be found on the Qseven® module edge connector. This interface is shared with the DisplayPort signals.

Table 3-28 Signal Definition HDMI

Signal	Shared With	Pin#	Description	I/O Type	I_{OL}/I_{IL}	Module I/O (Signal)
TMDS_CLK- TMDS_CLK+	DP_LANE3- DP_LANE3+	133 131	TMDS differential pair clock lines.	TMDS		O
TMDS_LANE0- TMDS_LANE0+	DP_LANE2- DP_LANE2+	145 143	TMDS differential pair lines lane 0.	TMDS		O
TMDS_LANE1- TMDS_LANE1+	DP_LANE1- DP_LANE1+	139 137	TMDS differential pair lines lane 1.	TMDS		O
TMDS_LANE2- TMDS_LANE2+	DP_LANE0- DP_LANE0+	151 149	TMDS differential pair lines lane 2.	TMDS		O
HDMI_CTRL_CLK		152	DDC based control signal (clock) for HDMI device.	CMOS 3.3V OD		I/O
HDMI_CTRL_DAT		150	DDC based control signal (data) for HDMI device.	CMOS 3.3V OD		I/O
HDMI_HPD#		153	Hot plug detection signal that serves as an interrupt request.	CMOS 3.3V		I

Note

Level Shifters and pull-ups to 5V for HDMI_CTRL_CLK and HDMI_CTRL_DAT shall be on the carrier board as shown in the schematics.

Support of the TMDS interface is chipset dependent and therefore may not be available on all Qseven® modules. TMDS interface signals are shared with the DisplayPort interface. The TMDS interface enables Qseven® modules to support DVI or HDMI.

3.13.1 HDMI Implementation

The HDMI signals on Qseven® modules are provided by the internal graphics chipset. On modules with x86 processor based technology the integrated HDMI signals are usually multiplexed with the Display Port interface. High speed HDMI level shifters are required to translate the signals to the HDMI compliant open-drain current driven Rx terminated differential output. As the outputs are platform-dependent, these level shifters shall be on the Qseven module.

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HDMI level shifter examples include but are not limited to:

NXP PTN3380B (http://www.nxp.com)
Parade Technologies PS101QFN48G (http://www.paradetech.com)
Pericom Semiconductor PI3VDV411LSZDE (http://www.pericom.com)
Chrontel CH7318 (http://www.chrontel.com).

Modules with ARM processor based technology usually feature native, unmultiplexed HDMI outputs.

3.13.1.1 HDMI Connector Signals

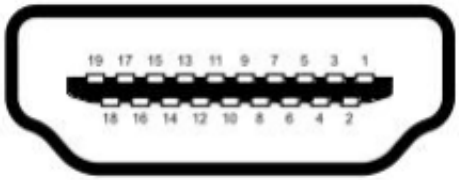


Figure 3-36 HDMI Connector

Table 3-29 Pinout HDMI Connector

Pin#	Signal	Description	Pin#	Signal	Description
1	TMDS Data 2+	HDMI Lane 2 (positive)	2	TMDS Data 2 Shield	Shield of Data 2 pair
3	TMDS Data 2-	HDMI Lane 2 (negative)	4	TMDS Data 1+	HDMI Lane 1 (positive)
5	TMDS Data 1 Shield	Shield of Data 1 pair	6	TMDS Data 1-	HDMI Lane 1 (negative)
7	TMDS Data 0+	HDMI Lane 0 (positive)	8	TMDS Data0 Shield	Shield of Data 0 pair
9	TMDS Data 0-	HDMI Lane 0 (negative)	10	TMDS Clock-	HDMI Clock (positive)
11	TMDS Clock Shield	Shield of Clock pair	12	TMDS Clock-	HDMI Clock (negative)
13	CEC	Consumer Electronics Control Interface	14	Reserved	N.C.
15	DDC Clock	DDC based control signal (clock)	16	DDC Data	DDC based control signal (data)
17	GND	Ground	18	+5V	+5V Power Supply
19	HPD	Hot plug detect			

Note

Native HDMI implementation is available with many ARM technology based modules.

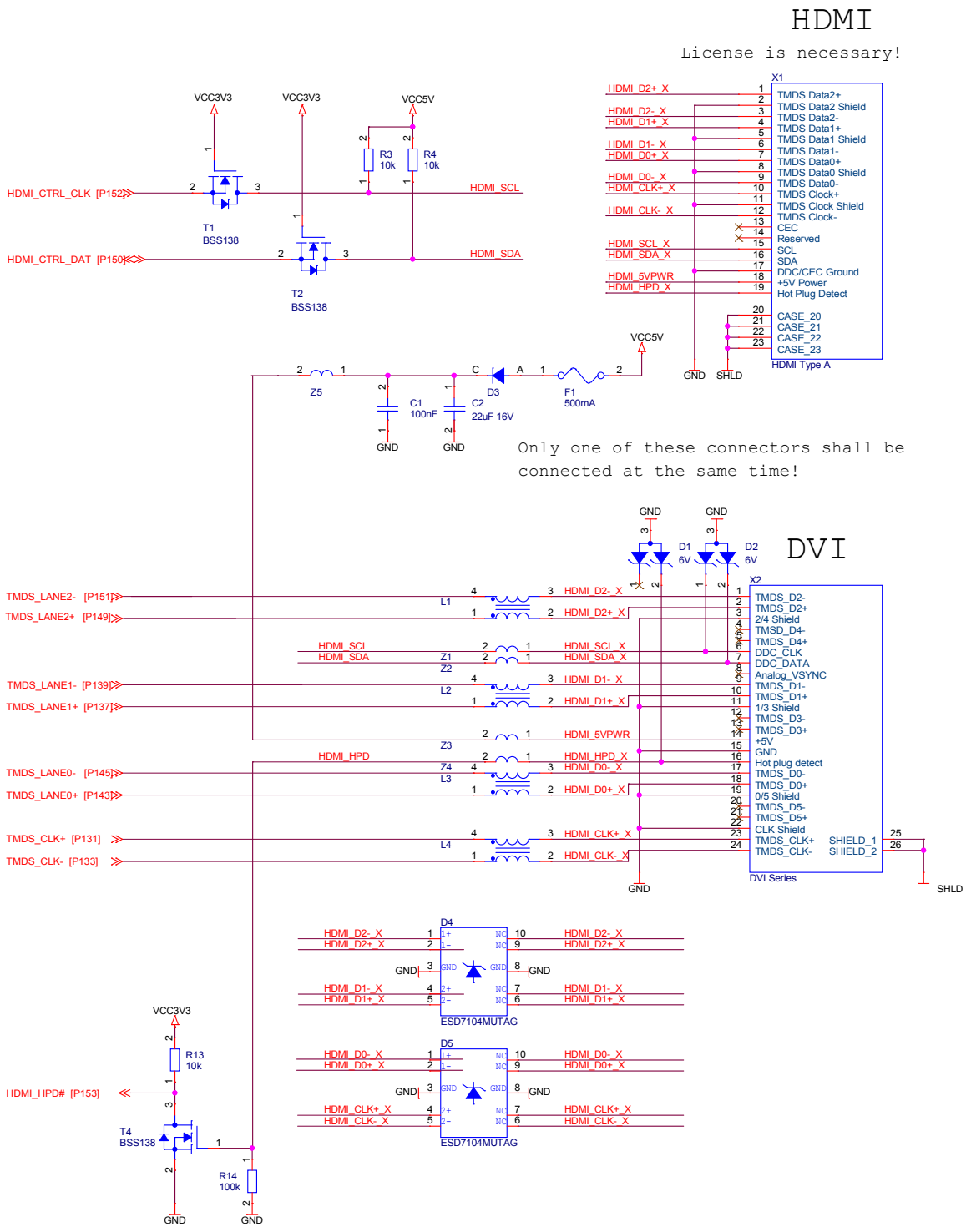
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3.13.2 Passive HDMI/DVI Transmitter Reference Circuitry

The example shows a passive wiring to either connect a HDMI or a DVI connector on the carrier board with native HDMI output from a module. In this case only level shifters are required for the I2C interface.

Figure 3-37 Passive HDMI to DVI/HDMI Transmitter Reference Circuitry



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3.14 LPC Interface Signals

The Low Pin Count Interface was defined by Intel® Corporation to facilitate the industry's transition towards legacy free systems. It allows the integration of low-bandwidth legacy I/O components within the system, which are typically provided by a Super I/O controller. Furthermore, it can be used to interface firmware hubs, Trusted Platform Module (TPM) devices and embedded controller solutions. Data transfer on the LPC bus is implemented over a 4 bit serialized data interface, which uses a 33MHz LPC bus clock. For more information about LPC bus refer to the 'Intel® Low Pin Count Interface Specification Revision 1.1'.

Since Qseven® is designed to be a legacy free standard for embedded modules, it does not support legacy functionality such as PS/2 keyboard/mouse, serial and parallel ports. Instead it provides an LPC interface that can be used to add peripheral devices to the carrier board design. The reduced pin count of the LPC interface makes it easy to implement such devices. All corresponding signals can be found on the module connector.

Table 3-30 Signal Definition LPC

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
LPC_AD[0..3]	185 to 188	Multiplexed Command, Address and Data.	CMOS 3.3V		I/O
LPC_FRAME#	190	LPC frame indicates the start of a new cycle or the termination of a broken cycle.	CMOS 3.3V		O
LPC_LDRQ#	192	LPC DMA request.	CMOS 3.3V		I
LPC_CLK	189	LPC clock.	CMOS 3.3V		O
SERIRQ	191	Serialized Interrupt.	CMOS 3.3V		I/O

Note

1) *While LPC interface is useful in x86 systems for backward compatibility it is not relevant at all for ARM systems.*

2) *Implementing external LPC devices on the Qseven® carrier board always requires customization of the Qseven® module's BIOS in order to support basic initialization for the LPC device. Otherwise the functionality of LPC device will not be supported by a Plug&Play or ACPI capable system.*

3) *All Examples in this chapter except the ones shown in Figure 3-38 (LPC Clock Buffer Reference Circuitry), Figure 3-41 and Figure 3-42 (LPC Super I/O SMSC SCH3114 Reference Circuitry) and Figure 3-48 (LPC Firmware Hub Reference Circuitry) have been taken from the current Qseven V2.0 reference carrier board.*

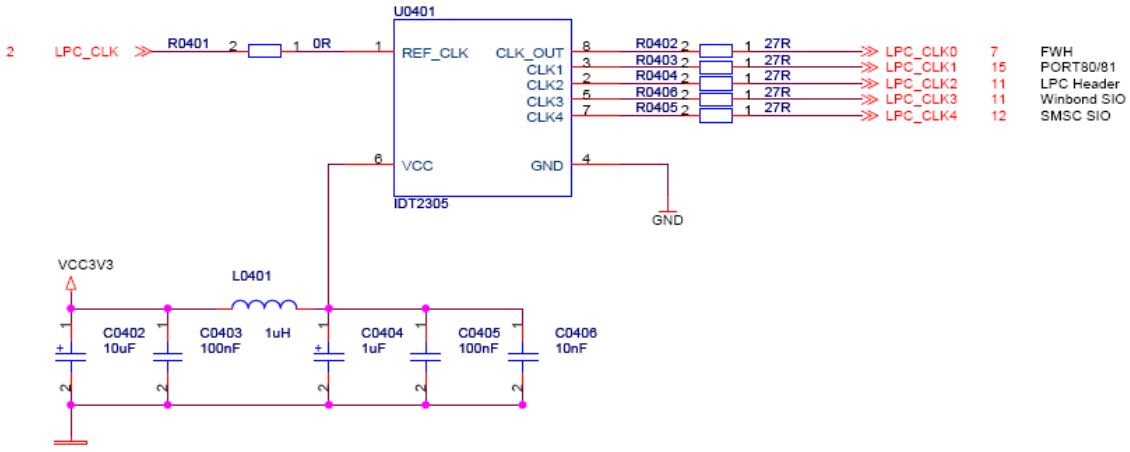
3.14.1 LPC Bus Clock Signal

Qseven® specifies a single LPC reference clock signal called *'LPC_CLK'* on the modules connector on pin 189. If more than one LPC clock signal is required on the carrier board to supply several LPC devices, a zero delay buffer must be used to expand the number of LPC clock lines. Figure 3-38 shows an example of how to implement a Integrated Device Technology IDT2305 zero delay clock buffer (http://www.idt.com).

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Figure 3-38 LPC Clock Buffer Reference Circuitry



Note

1. *Qseven® modules based on the Intel® Atom™ Processor and Intel® System Controller Hub US15W can not be booted from external BIOS Firmware Hubs (FWH) that are clocked by a buffered or delayed clock signal.*

2. *This is just an example. The Qseven 2.0 reference carrier board does not include an LPC Clock Buffer.*

3.14.1.1 Routing Considerations for LPC Clock

The LPC clock implementation should follow the routing guidelines for the PCI clock defined in the 'PCI Local Bus Specification Revision 2.3'.

3.14.2 LPC Reset Signal

The LPC interface should use a reset signal that is generated by splitting the PCI Express reset (PCIE_RST#, pin 158 of the Qseven® connector) signal with a zero delay buffer. An example can be found in Figure 3-6 of this document. This solution is also used on the SGeT e.V. V2.0 evaluation carrier board. Here the LPC reset signal is called *'PLT_RESET#'.* If the carrier board implements more than one LPC device, it is recommended that the LPC reset signal be split so that each LPC device will be provided with a separate reset signal.

3.14.3 LPC Super I/O Support

The Qseven® BIOS firmware includes integrated support for the following external LPC Super I/O controllers in order to provide additional legacy COM ports:

- Nuvoton W83627DHG LPC Super I/O with 2 COM ports (http://www.nuvoton.com)
- SMSC SCH3114 LPC Super I/O with 4 COM ports (http://www.smsc.com)
- EXAR X28V384 LPC Super I/O with 4 COM ports http://www.exar.com

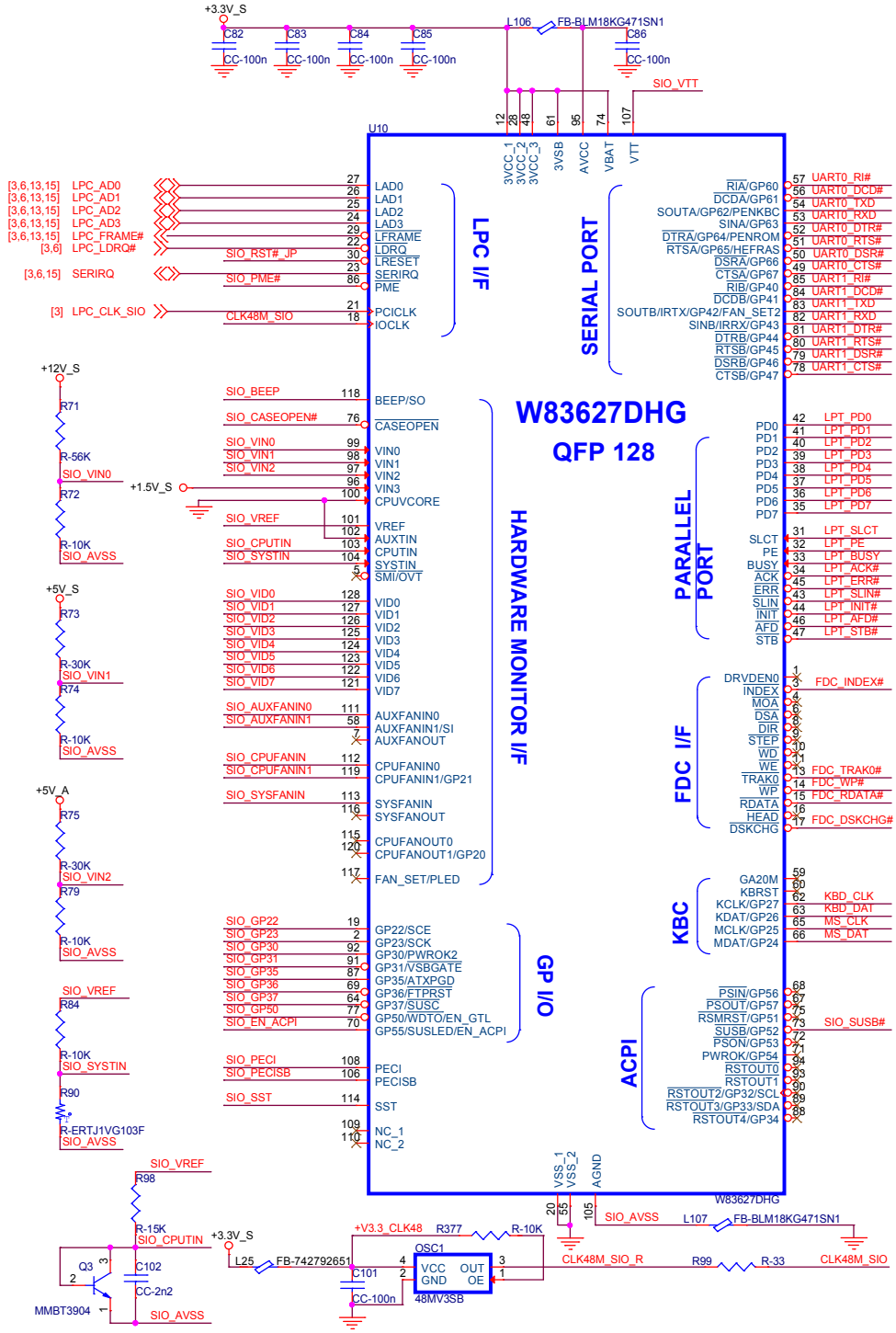
If any of the additional functionality of the Super I/O is required by the application, then it may be implemented via the application's software program. There are Super I/O functions that can be configured by hardware straps, which is defined within the datasheet of that particular Super I/O (for example PS/2 keyboard functionality).

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The base address for these Super I/O controllers shall be 0x2E to be sure that the legacy COM port devices of the Super I/O controller can be initialized by the BIOS.

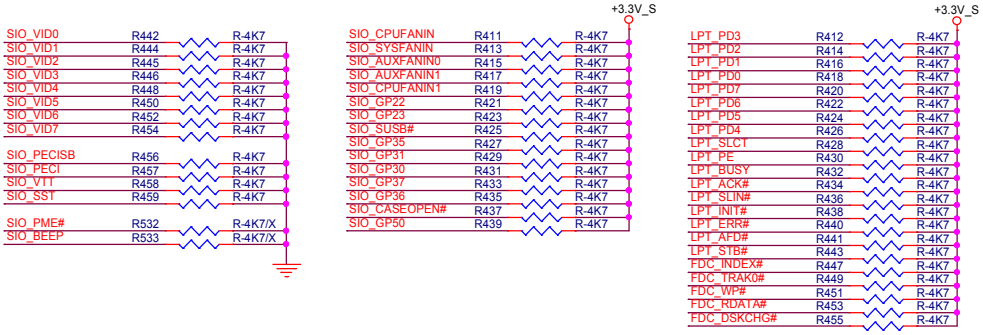
3.14.3.1 LPC Super I/O with Nuvoton W83627DHG

Figure 3-39 LPC Super I/O Nuvoton W83627DHG Reference Circuitry



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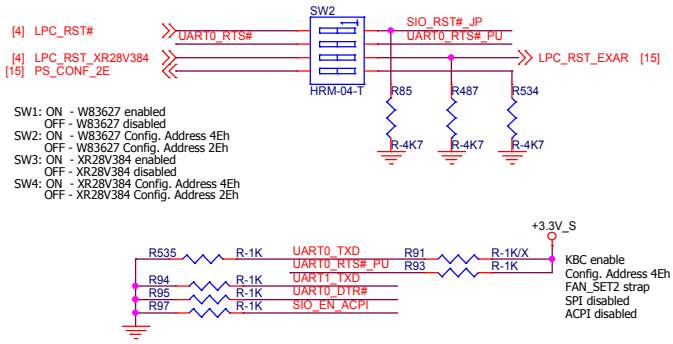
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3.14.3.2 Boot Up Configuration for Nuvoton W83627DHG

The default configuration of the Nuvoton W83627DHG LPC Super I/O controller during power-on can be implemented by hardware strap options. The hardware strap pins are located on the serial port interface of the Super I/O controller. They can be enabled by placing a 10kΩ pull-up resistor between +3.3V supply voltage and one of the dedicated hardware strap pins. Figure 3-40 shows the boot strap configuration options for the Nuvoton W83627DHG LPC Super I/O controller.

Figure 3-40 Nuvoton W83627DHG Boot Strap Configuration



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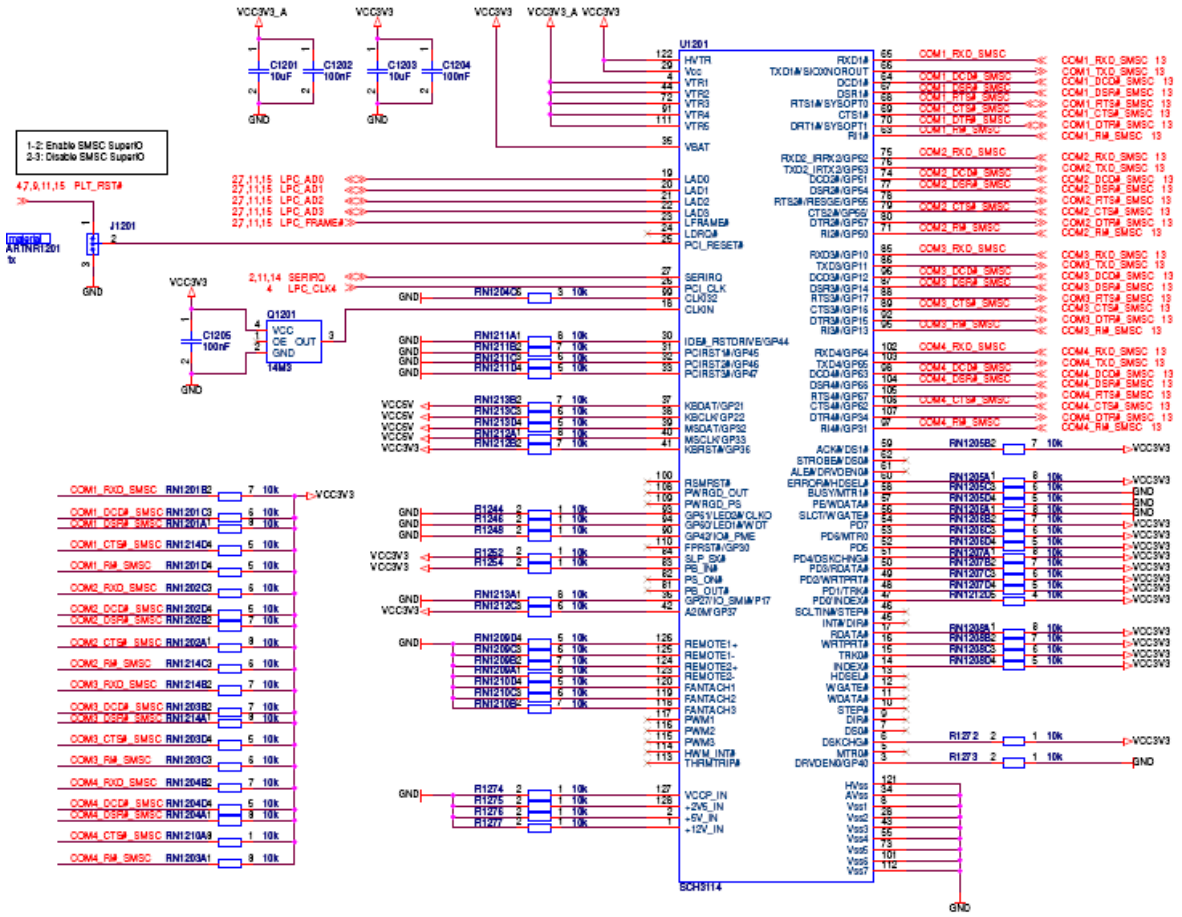
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3.14.3.3 LPC Super I/O with SMSC SCH3114

Note

This is just an example. The Qseven 2.0 reference carrier board does not use an SMSC SCH3114 in its LPC Super I/O circuitry.

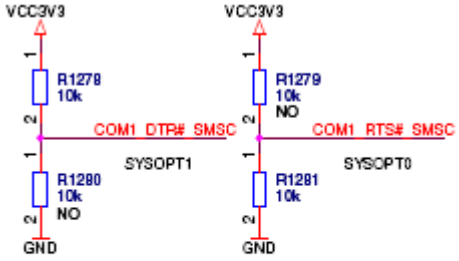
Figure 3-41 LPC Super I/O SMSC SCH3114 Reference Circuitry



3.14.3.4 LPC Boot Up Configuration for SMSC SCH3114

The default configuration of the SMSC SCH3114 LPC Super I/O controller during power-on can be implemented by hardware strap options. The hardware strap pins are located on the serial port interface of the Super I/O controller. They can be enabled by placing a 4.7kΩ pull-up resistor between +3.3V supply voltage and one of the dedicated hardware strap pins. Figure 3-42 shows the boot strap configuration options for the SMSC SCH3114 LPC Super I/O controller.

Figure 3-42 SMSC SCH3114 Boot Strap Configuration



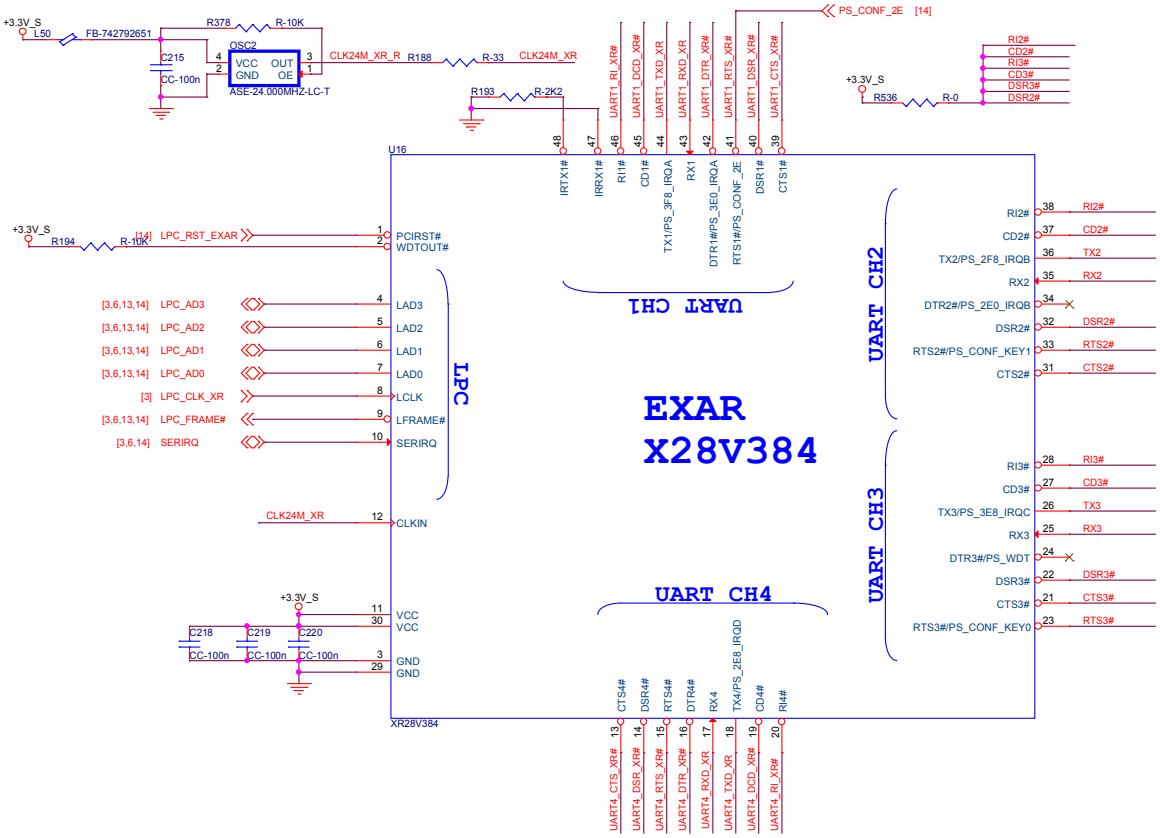
SYSOPT1	SYSOPT2	Address
1	0	0x2Eh
1	1	0x4Eh
0	0	0x162Eh
0	1	0x164Eh

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3.14.3.5 LPC Super I/O with EXAR X28V384

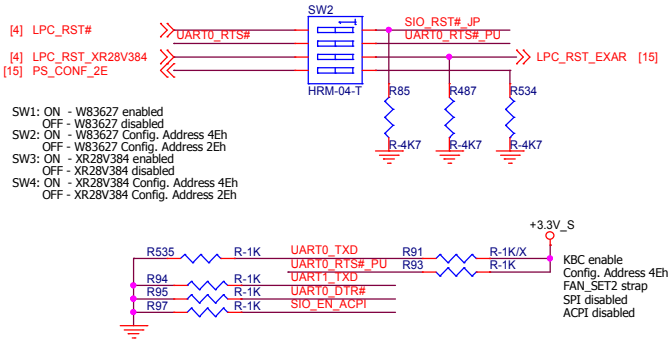
Figure 3-43 LPC Super I/O EXAR X28V34 Reference Circuit



3.14.3.6 LPC Boot Up Configuration for EXAR X28V384

The default configuration of the EXAR X28V384 LPC Super I/O controller during power-on can be implemented by hardware strap options. The hardware strap pins are located on the serial port interface of the Super I/O controller. They can be enabled by placing a 4.7kΩ pull-up resistor between +3.3V supply voltage and one of the dedicated hardware strap pins. Figure 3-43 shows the boot strap configuration options for the EXAR X28V384 LPC Super I/O controller.

Figure 3-44 EXAR X28V384 Boot Strap Configuration

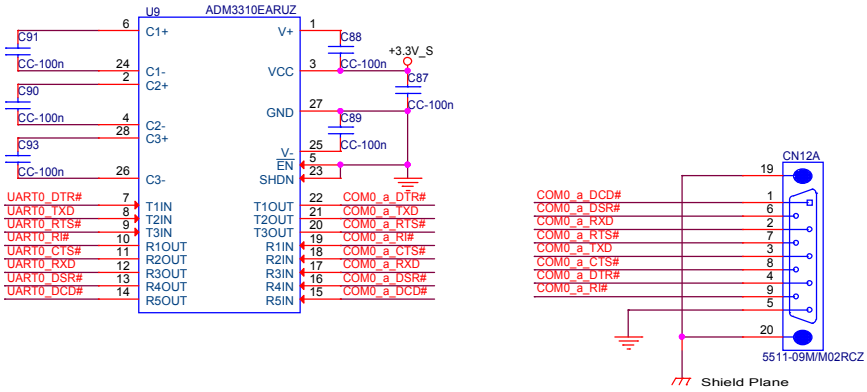


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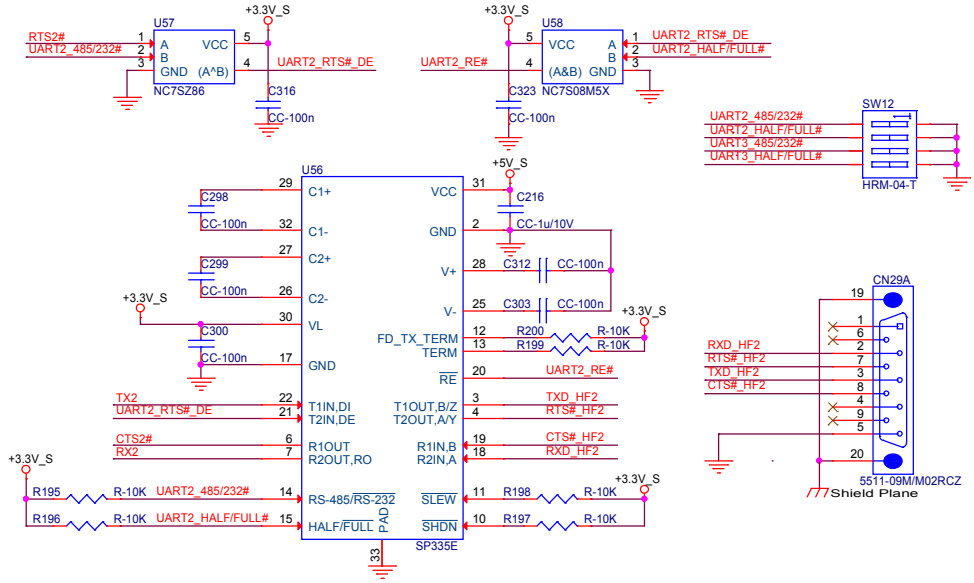
3.14.3.7 LPC RS232 Serial Port Reference Circuitry

Figure 3-45 COM Port Reference Circuit (RS-232)



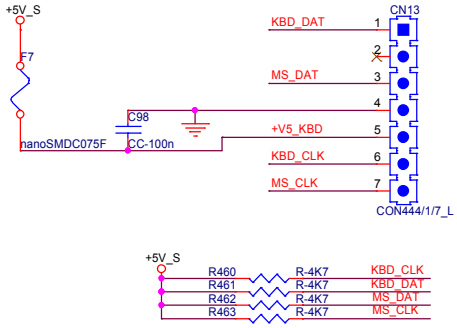
3.14.3.8 LPC configurable RS232 Serial Port Reference Circuitry

Figure 3-46 COM Port Reference Circuit (RS-232/485/422)



3.14.3.9 LPC PS2 Keyboard Port Reference Circuitry

Figure 3-47 PS2 Keyboard Port Reference Circuit



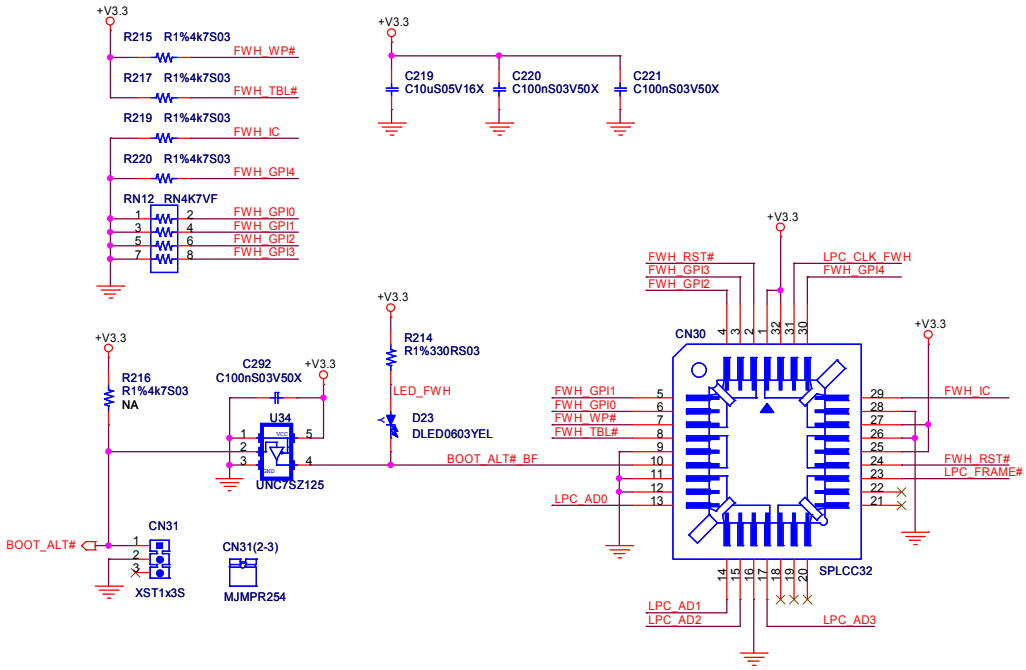
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3.14.4 LPC Firmware Hub

The LPC bus interface on Qseven® modules offers the possibility to boot the module using BIOS code programmed into an external firmware hub (FWH). The external FWH can be implemented on the carrier board. A hardware jumper must be provided on the carrier board to disable the module's onboard FWH and to enable the external FWH. The corresponding signal '*BIOS_DISABLE#*' can be found on pin 41 of the Qseven® connector. Figure 3-48 shows a reference circuitry for an external 32-pin PLCC FWH socket.

Figure 3-48 LPC Firmware Hub Reference Circuitry



Note

For many new chipsets the Firmware Hub is no longer supported.

This is just an example. There is no firmware hub implemented on the Qseven V2.0 reference carrier board.

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3.15 CAN Bus Interface Signals

Controller Area Network (CAN or CAN-bus) is a message based protocol designed specifically for automotive applications but now is also used in other areas such as industrial automation and medical equipment.

Starting with Qseven® Specification revision 1.20, Qseven® modules can optionally support one CAN bus.

Table 3-31 Signal Definition CAN Bus

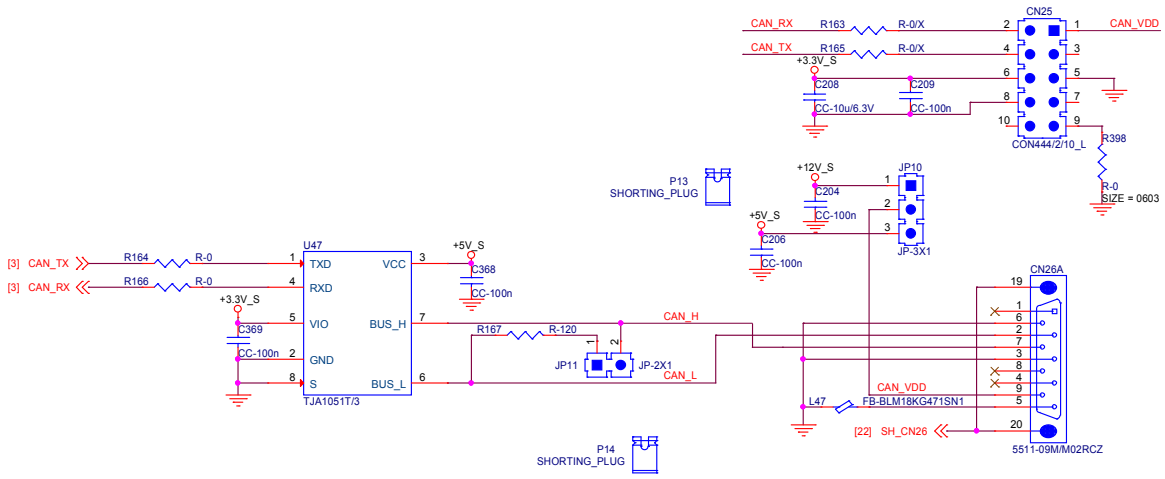
Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
CAN0_TX	129	CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	CMOS 3.3V		O
CAN0_RX	130	CAN0_RX RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	CMOS 3.3V		I

Note

If the CAN Bus interface is not used, and/or the Qseven® module's chipset does not support CAN Bus, then these pins shall be left unconnected.

Termination of all signals (e.g. required pullup/pulldown resistors) will be always on the module unless explicitly otherwise noted.

Figure 3-49 CAN Bus Reference Circuitry



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3.16 SPI Interface Signals

The Serial Peripheral Interface (SPI) is a 4-pin interface that provides a potentially lower-cost alternative for system devices such as EEPROM and flash components.

Starting with Qseven® Specification revision 1.20, Qseven® modules can optionally support one SPI interface. Check module vendor's user guide whether general purpose SPI can be used.

Figure 3-50 SPI Interface Connector Reference Circuitry

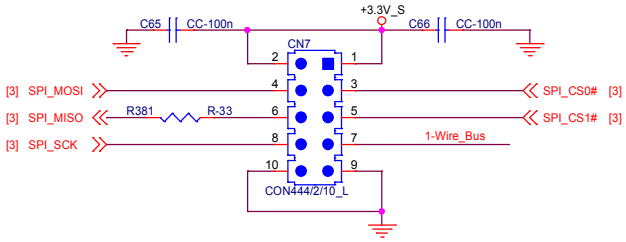
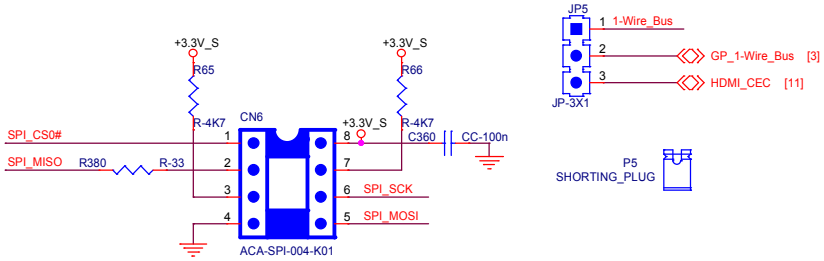


Table 3-32 Signal Definition SPI Interface

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
SPI_MOSI	199	Master serial output/Slave serial input signal. SPI serial output data from Qseven® module to the SPI device.	CMOS 3.3V		O
SPI_MISO	201	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven® module.	CMOS 3.3V		I
SPI_SCK	203	SPI clock output.	CMOS 3.3V		O
SPI_CS0#	200	SPI chip select 0 output.	CMOS 3.3V		O
SPI_CS1#	202	SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.	CMOS 3.3V		O

Figure 3-51 Shows a reference circuitry for an external SPI flash.

Figure 3-51 SPI Flash Reference Circuitry



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3.17 Input Power

Qseven® modules are designed to be driven with a single +5V input power rail. Additionally, two optional power rails are specified by Qseven® to provide a +5V standby voltage (5V-Always) on the Qseven® module as well as a +3V Real Time Clock (RTC) supply voltage, which is provided by a battery cell located on the carrier board.

If the carrier board does not require standby functionality, then the +5V standby power rail can be omitted. In this case the VCC_5V_SB pins shall be connected to the +5V input power rail. The same applies to the +3V RTC battery voltage rail. If no RTC/CMOS backup functionality is required by the system during power-off, then the +3V RTC supply battery voltage can be omitted. During standby and power-on the RTC/CMOS should be supplied by the 3.3V standby rail on the carrier board (see Figure 3-58).
Please refer to the Qseven specification for the power up and power down power rail sequencing.

The following practices should be implemented in order to prevent possible damage to the customized carrier board and/or injury to the operator.

Over-current Protection

For safety reasons, the main power supply path should be fused. There should be a fuse placed between the system's power supply output and the customized carrier board's power supply input. This fuse may be a standard fuse or could also be a poly fuse. Either one is sufficient. The maximum current must be tested and determined by the carrier board designer.

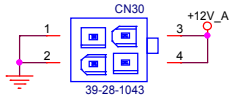
This mechanism will protect the system from serious damage if too much current is drawn from the power supply.

Reverse Polarity Protection

There are two options to ensure that a system is not damaged by reverse polarity.

One way is to use a power supply connector that is mechanically keyed and prevents reverse insertion. Figure 3-52 Shows an example for a coded connector for reverse polarity protection

Figure 3-52 Coded Power Connector for Reverse Polarity Protection



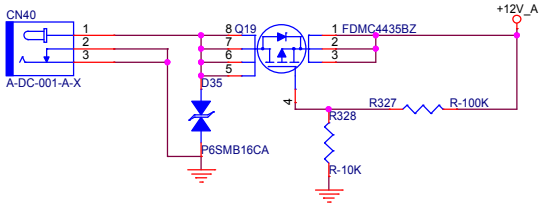
The second option is to use electronic components to guarantee reverse polarity protection. One way to do this is to use a Schottky diode or an active power switch. This should be placed in the main power supplying path of the carrier board to avoid current flow into the system when system power is connected with reversed polarity. The maximum current must be set and tested by the carrier board designer.

Figure 3-53 Shows an example for a reverse polarity protection circuitry

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Figure 3-53 Reverse Polarity Protection Circuit



For more information about the power input, ripple tolerances and input power sequencing refer to the Qseven® 2.0 Specification.

Table 3-33 Signal Definition Input Power

Signal	Pin#	Description	I/O
VCC	211 to 230	Power Supply +5VDC ±5%.	P
VCC_5V_SB	205, 206	Standby Power Supply +5VDC ±5%.	P
VCC_RTC	193	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.4 - 3.3 V).	P
GND	1, 2, 23, 24, 25, 26, 34, 39, 40, 57, 58, 73, 74, 97, 98, 117, 118, 135, 136, 141, 142, 147, 148, 159, 160, 165, 166, 183, 184, 197, 198	Power Ground.	P

Note
If the standby 5V power rail 'VCC_5V_SB' is not provided by the carrier board, then the VCC_5V_SB pins (pins 205-206) of the Qseven® module must be connected with the main VCC power rail pins (pins 211-230).

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3.17.1 Single Source Power Supply

Figures show examples for voltage regulating/power supply circuitry as used in the Qseven 2.0 reference carrier board. Shown are instances for 12V carrier board voltage as implemented on the Qseven V2.0 reference carrier board.

Figure 3-54 Power Enable Circuit for 5V_Always

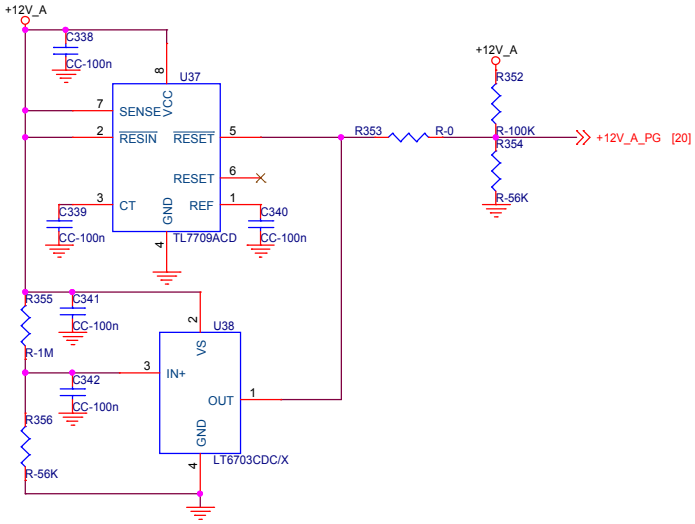


Figure 3-55 Power Regulator Circuit for 5V_Always

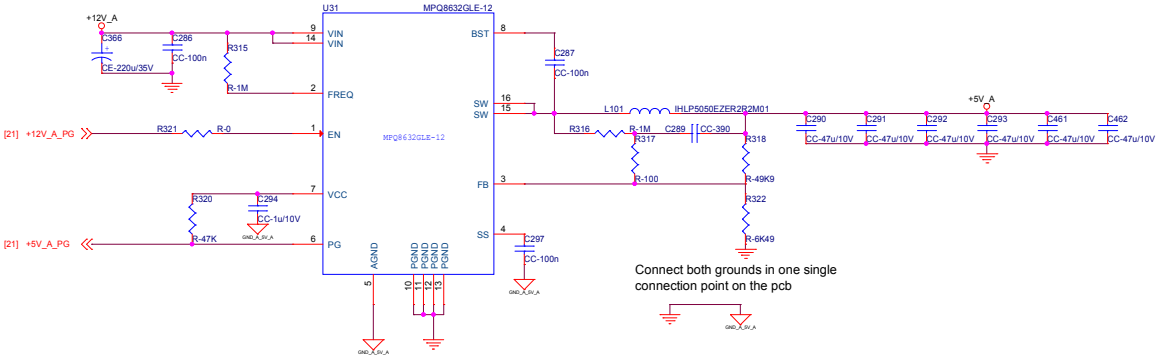
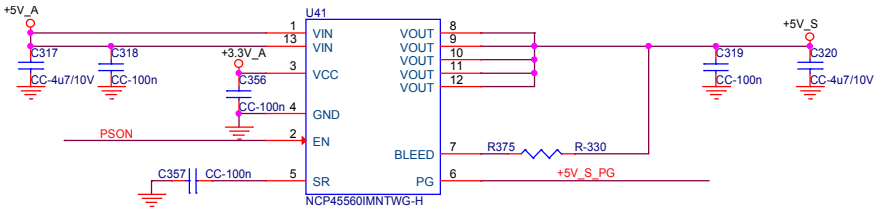


Figure 3-56 Power Regulator Circuit for 5V_Switched



Note

For details on PSON signaling see Chapter 3.18.3 .

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3.17.2 ATX Power Supply

ATX power supplies are widely used for consumer PC motherboards and they are also a cost effective and reliable solution for embedded designs. ATX power supplies provide all the necessary power rails required for a carrier board design and may be an alternative to a custom power supply design. Table 3-34 and Table 3-36 describe the signals provided by the ATX power supply connectors.

Note

This is an example only.

The Qseven V2.0 reference carrier board is not using an ATX power supply.

3.17.2.1 ATX Power Connector

Table 3-34 ATX Connector 24 PIN

Signal	Pin	Description	Signal	Pin	Description
3.3V	1	+3.3V Power Supply	3.3V	13	+3.3V Power Supply
3.3V	2	+3.3V Power Supply	-12V	14	-12V Power Supply
COM	3	Ground	COM	15	Ground
5V	4	+5V Power Supply	PS_ON#	16	Active low signal, which is controlled by the Qseven® module to turn on or off the ATX power supply.
COM	5	Ground	COM	17	Ground
5V	6	+5V Power Supply	COM	18	Ground
COM	7	Ground	COM	19	Ground
PWR_OK	8	Status signal generated by the ATX power supply to notify the Qseven® module that the DC operating voltages are within the ranges required for proper operation.	Reserved	20	N.C.
5VSB	9	+5V Standby Voltage	+5V	21	+5V Power Supply
+12V	10	+12V Power Supply	+5V	22	+5V Power Supply
+12V	11	+12V Power Supply	+5V	23	+5V Power Supply
+3.3V	12	+3.3V Power Supply	COM	24	Ground

Note

The above table describes the pinout of a 24-pin ATX connector. When using a 20-pin ATX connector omit the following four pins: 11, 12, 23 and 24.

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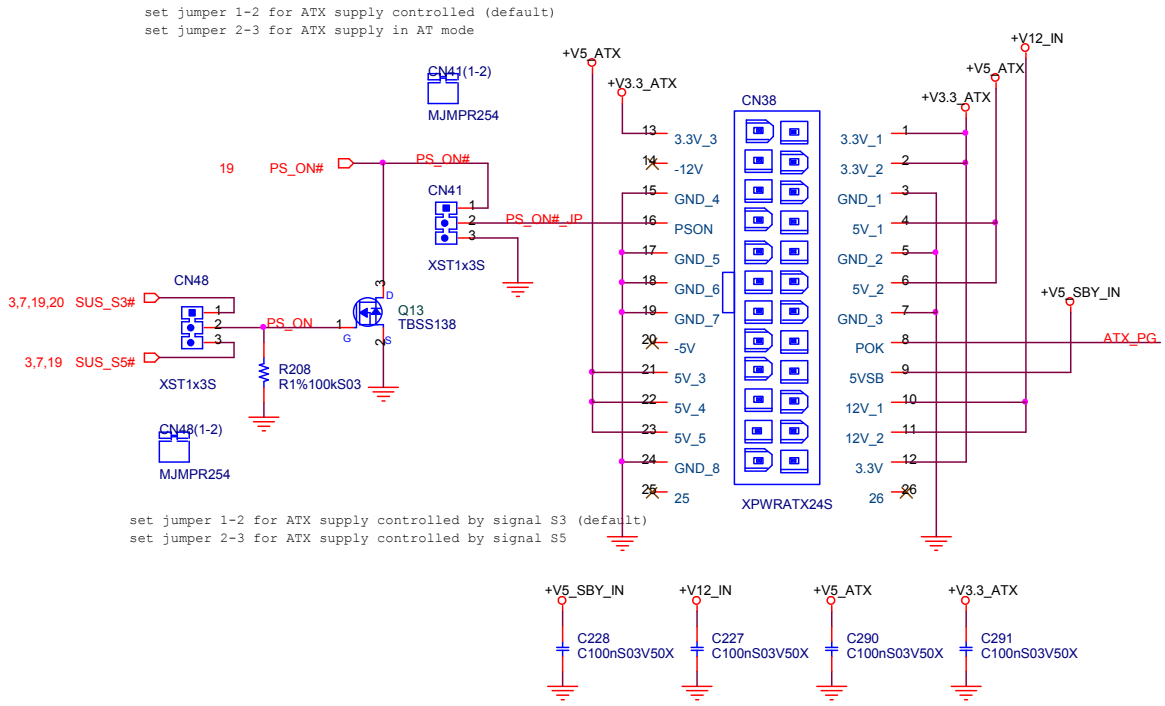
Table 3-35 ATX Connector 20 Pin

Signal	Pin	Description	Signal	Pin	Description
3.3V	1	+3.3V Power Supply	3.3V	11	+3.3V Power Supply
3.3V	2	+3.3V Power Supply	-12V	12	-12V Power Supply
COM	3	Ground	COM	13	Ground
5V	4	+5V Power Supply	PS_ON#	14	Active low signal, which is controlled by the Qseven® module to turn on or off the ATX power supply.
COM	5	Ground	COM	15	Ground
5V	6	+5V Power Supply	COM	16	Ground
COM	7	Ground	COM	17	Ground
PWR_OK	8	Status signal generated by the ATX power supply to notify the Qseven® module that the DC operating voltages are within the ranges required for proper operation.	Reserved	18	N.C.
5VSB	9	+5V Standby Voltage	+5V	19	+5V Power Supply
+12V	10	+12V Power Supply	+5V	20	+5V Power Supply

Table 3-36 +12V Power Connector 4 Pin

Signal	Pin	Description	Signal	Pin	Description
GND	1	Ground	GND	2	Ground
+12V	3	+12V Power Supply	+12V	4	+12V Power Supply

Figure 3-57 Schematic of 24 Pin ATX Power Connector



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3.17.3 RTC Battery

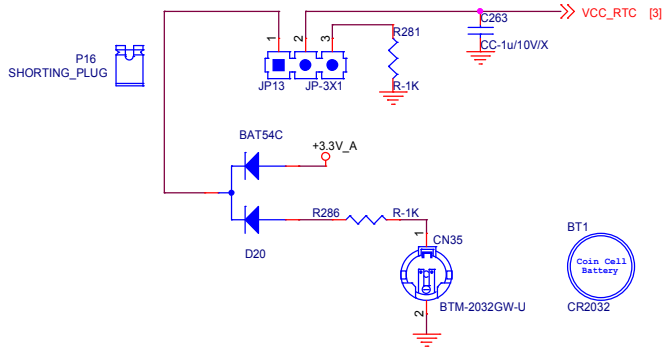
The Real Time Clock (RTC) is responsible for maintaining the time and date even when the Qseven® module is not connected to a main power supply. Usually a +3V lithium battery cell is used to supply the internal RTC of the module. The Qseven® specification defines an extra power pin *'VCC_RTC',* which connects the RTC of the module to the external battery. The specified input voltage range of the battery is defined between +2.4V and +3.3V. The signal *'VCC_RTC'* can be found on the module's connector pin 193.

3.17.3.1 RTC Battery Reference Circuitry

To implement the RTC Battery according to the Underwriters Laboratories Inc® (UL) guidelines, battery cells must be protected against a reverse current going to the cell. This can be done by either a series Schottky diode or a series resistor. The safest way, and the one recommended by the SGeT e.V., is to implement a RTC battery circuitry using a Schottky diode (D1404) as shown in Figure 3-58.

This method offers protection against a possible explosion hazard as a result of reverse current flowing to the battery. Moreover, this implementation offers more flexibility when choosing battery type and manufacturer. Lithium batteries are the most common form of battery used in this scenario.

Figure 3-58 RTC Battery Circuitry with Serial Schottky Diode



Note

The SGeT e.V. recommends that a warning label is placed on or near the carrier board battery socket to indicate the appropriate manufacturer and model of battery that must be used to avoid creating an explosion hazard. This applies regardless of which RTC battery circuitry method has been implemented on the carrier board.

3.17.3.2 RTC Battery Lifetime

The RTC battery lifetime determines the time interval between system battery replacement cycles. Current leakage from the RTC battery circuitry on the carrier board is a serious issue and must be considered during the system design phase. The current leakage will influence the RTC battery lifetime and must be factored in when a specific life expectancy of the system battery is being defined.

In order to accurately measure the value of the RTC current it should be measured when the complete system is disconnected from AC power.

The RTC power plane is normally ored with the 3V3 Voltage on the module, so it may not be necessary to perform this on the carrier board. Please consult the module vendor's documentation.

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3.18 Power Control Signals

Table 3-37 Signal Definition Power Control

Signal	Pin#	Description of Power Control signals	I/O Type	I_{OL}/I_{IL}	I/O
PWGIN	26	High active input for the Qseven® module indicates that power from the power supply is ready.	CMOS 5V	≥ 4 mA	I
PWRBTN#	20	Power Button: Low active power button input. This signal is triggered on the falling edge.	CMOS OD 3.3V Standby	≥ 10 mA	I

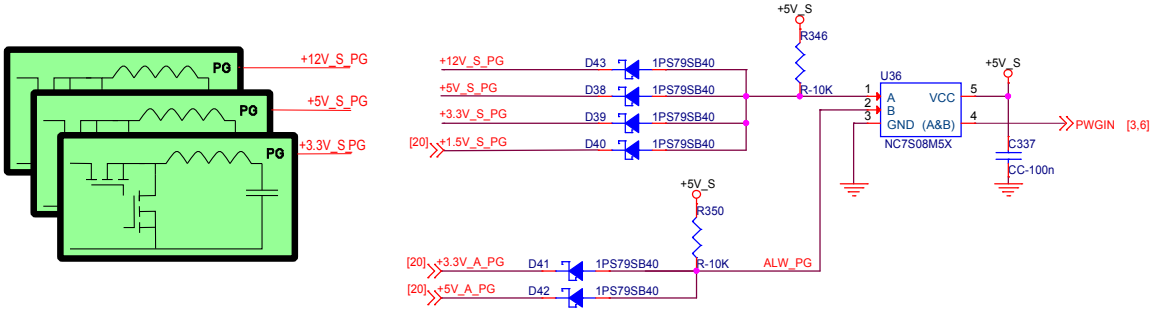
Note

Termination of all signals (e.g. required pullup/pulldown resistors) will be always on the module unless explicitly otherwise noted.

3.18.1 Power Good Input Signal PWGIN

This signal is optionally generated by the power supply circuitry and indicates that the operating voltages are within the ranges required for proper operation of the Qseven® module and carrier board components. The example in Figure 3-59 shows the implementation on the Qseven V2.0 reference carrier board.

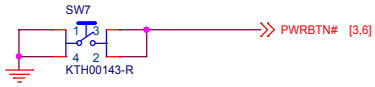
Figure 3-59 PWGIN Generation Circuit



3.18.2 Power Button Signal PWRBTN#

The power button signal is used to turn on the Qseven® based system when using an ATX power supply or to wake up the system from ACPI power states S3 and S5.
If the Power button is pressed for 4 seconds or longer a power override occurs and the power will be turned off (for x86 based modules only- check with your module vendor's user's guide for ARM based modules).

Figure 3-60 Power Button Implementation Example



Note

In a case where the system does not require a power button (system boots automatically when the power is supplied) the PS_ON# signal of the ATX power supply must be pulled to ground (see Figure 3-61 jumper J1603).

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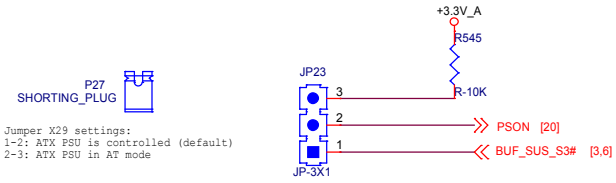
3.18.3 Power Up Control

The power up control is responsible for switching the Qseven V2.0 reference carrier board on or off when a power-up or a power-down event occurs. A power event can be generated by pressing the power button or by another system event, which can originate from or be detected by the Qseven® module's chipset.

The native system power-up support of Qseven® modules utilize the *'SUS_S3#'* signal to control the *'PSON'* signal, which is used to switch the supply rails on or off. When using the *SUS_S3#'* signal, Qseven® modules are capable of supporting Suspend to RAM (S3).

When the system goes to Suspend to RAM (S3) or Soft Off (S5), the *'SUS_S3#'* signal is asserted by the chipset of the module. Through this behavior the signal can be used to drive 'PSON' and switches off the power rails of the carrier. Vice versa, if the system is in a power-down system state, any system wake-up event invokes the module's chipset to deassert the *'SUS_S3#'* signal and transfers the system to Full-On (S0) state.

Figure 3-61 Power Up Control Circuitry



Note

See also Figure 3-57

PSON signal implementation on the Qseven V2.0 reference carrier board is high active while PSON# signal is low active when an ATX power supply is used.

A Qseven® based system using an AT power supply, with no standby voltage present, does not need the circuitry shown in Figure 3-61. In this case the Qseven® module will automatically boot up after the AT power supply is switched on.

3.18.4 ATX Power Up Control

The power up control is responsible for switching the ATX power supply on or off when a power-up or a power-down event occurs. A power event can be generated by pressing the power button or by another system event, which can originate from or be detected by the Qseven® module's chipset.

The native system power-up support of Qseven® modules utilize the *'SUS_S3#'* signal to control the *'PS_ON#'* signal, which is used to switch the ATX power supply on or off. When using the *SUS_S3#'* signal, Qseven® modules are capable of supporting Suspend to RAM (S3).

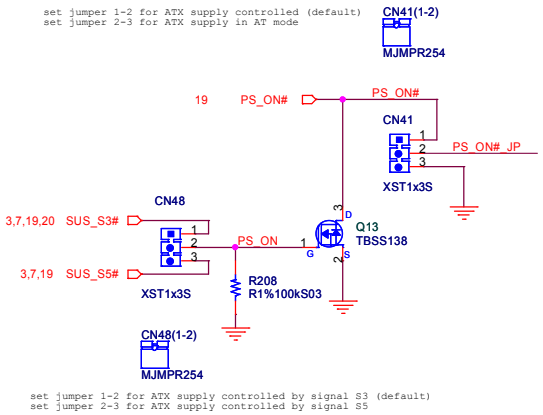
When the system goes to Suspend to RAM (S3) or Soft Off (S5), the *'SUS_S3#'* signal is asserted by the chipset of the module. Through the use of an inverter, the low active *'PS_ON#'* signal goes high and switches off the ATX power supply. Vice versa, if the system resides in a power-down system state, any system wake-up event invokes the chipset of the module to deassert the *'SUS_S3#'* signal. This results in a system transition to Full-On (S0).

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The way Suspend to RAM is implemented on a Qseven® module may differ depending on the module manufacturer. For this reason it is recommended that a hardware jumper be implemented on the carrier board in order to provide the ability to choose if the *'PS_ON#'* signal should be controlled either by the *'SUS_S3#'* signal or '*SUS_S5#'* signal.

Figure 3-62 ATX Power Up Control Circuitry



Note

See also Figure 3-57

PSON signal implementation on the Qseven V2.0 reference carrier board is high active while PSON# signal is low active when an ATX power supply is used.

When the Qseven® based system uses an AT power supply (with no standby voltage present), the circuit shown in Figure 3-42 is not required. The Qseven® module will automatically boot up after the AT power supply is switched on.

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3.19 Power Management Signals

Qseven® specifies a set of signals to control the system power states such as the power-on and reset conditions. This enables the system designer to implement a fully ACPI compliant system supporting system states from S0 to S5. The minimum hardware requirements for an ACPI compliant system is an ATX conforming power supply and a power button.

The following table provides a short description of the ACPI defined system states S0 to S5, including the corresponding power rail state. For more information about ACPI and the several system power states, refer to the 'Advanced Configuration and Power Interface Specification Revision 3.0.

Table 3-38 System States S0-S5 Definitions

System State	Description	Power Rail State
S0 Full On	During S0 state, all components are powered and the system is fully functional.	Full power on all power rails.
S1 Power-on Standby (POS)	In S1 sleep state, no system context is lost, hardware maintains all system context. During S1 operation some system components are set into low power state.	Full power on all power rails.
S2	Not supported.	
S3 Suspend to RAM (STR)	In S3 state, the current system state and context is stored in main memory and all unnecessary system logic is turned off.	Only main memory and logic required to wake-up the system remain powered by the standby voltages. All other power rails are switched off.
S4 Suspend to Disk (STD)	In S4 state the contents of the main memory are written to non-volatile storage such as a hard disk, as a file or on a separate partition, before powering off the computer.	See note below.
S5 Soft Off	In S5 state the system is switched off. Restart is only possible with the power button or by a system wake-up event such as 'Wake On LAN' or RTC alarm.	Standby power rails may or may not be powered, depending on if system wake-up is supported.

Note

Two types of S3 mode are defined : S3-Hot and S3-Cold.
S3-Hot - In the S3 (suspend to RAM) mode both VCC_5V and VCC_5V_SBY are applied to module.
S3-Cold - In the S3 (suspend to RAM) mode only VCC_5V_SBY are applied to module. Please check the module provider implementation

S4 (Suspend to Disk) might be not supported by all Qseven® BIOSes (S4_BIOS) but is supported with state-of-the-art operating systems (S4_OS = Hibernate).

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Table 3-39 Signal Definition Power Management

Signal	Pin#	Description of Power Management signals	I/O Type	I_{OL}/I_{IL}	I/O
RSTBTN#	28	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module.	CMOS 3.3V	≥ 10 mA	I
BATLOW#	27	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	CMOS 3.3V Suspend	≥ 10 mA	I
WAKE#	17	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	CMOS 3.3V Suspend	≥ 10 mA	I
SUS_STAT#	19	Suspend Status: indicates that the system will be entering a low power state soon.	CMOS 3.3V Suspend	max. 1 mA	O
SUS_S3#	18	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to RAM), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	CMOS 3.3V Suspend	max. 1 mA	O
SUS_S5#	16	S5 State: This signal indicates S4 or S5 (Soft Off) state.	CMOS 3.3V Suspend	max. 1 mA	O
SLP_BTN#	21	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.	CMOS 3.3V Suspend	≥ 10 mA	I
LID_BTN#	22	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. TBD: Open/Close state.	CMOS 3.3V Suspend	≥ 10 mA	I

Note

All carrier board power rails, which are originating from the VCC power rail, MUST be enabled by the SUS_S3# signal.

There are two types of S3 mode defined : S3-Hot and S3-Cold.

S3-Hot - In the S3 (suspend to RAM) mode both VCC_5V and VCC_5V_SBY are applied to the module.

S3-Cold - In the S3 (suspend to RAM) mode only VCC_5V_SBY are applied to the module. Please check the module manufacturer's implementation guidelines.

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3.20 I²C Bus

The I²C Bus is a frequently used low speed bus interface for connecting embedded devices such as sensors, converters or data storage. Qseven® modules provide one I²C bus interface on the module's connectors.

Table 3-40 I²C bus Signals

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
I2C_CLK	66	Clock line of I²C bus.	CMOS 3.3V OD		I/O
I2C_DAT	68	Data line of I²C bus.	CMOS 3.3V OD		I/O

Note

Required termination (pullup and/or pulldown resistors) is on the module unless otherwise noted.

These signals are NOT powered by the suspend rail.

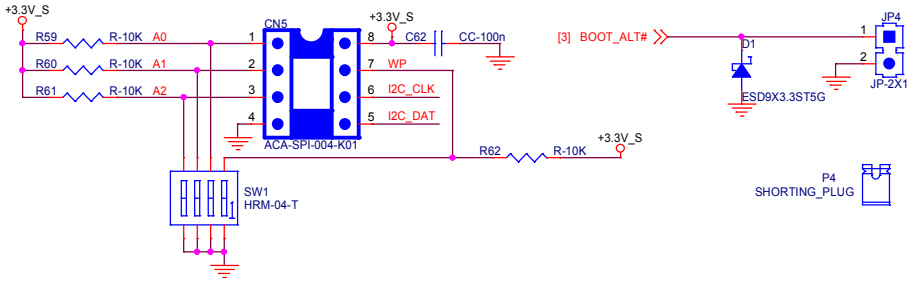
The I²C Bus of the Qseven® module can be accessed and programmed by using the API (Application Program Interface) called Embedded Application Programming Interface (EAPI). For more details about EAPI, refer to the Qseven® specification and the module vendor's EAPI Programmers Guide.

Starting with specification Rev. 1.20, Qseven® modules offer a second General Purpose I²C Bus. This I²C Bus is available on the Qseven® connector pins 125 (GP_I2C_DAT) and 127 (GP_I2C_CLK) and is multiplexed with the LVDS flat panel detection signals LVDS_DID_DAT and LVDS_DID_CLK

3.20.1 I²C Implementation Example

The example below shows the implementation of an an I²C EEPROM (DIP8 Socket) on the Qseven® carrier board. In this example, the I²C address of the EEPROM can be set by a DIP switch.

Figure 3-63 I²C Implementation Example



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3.21 Miscellaneous Signals

Table 3-41 Miscellaneous Signals

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
WDTRIG#	70	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse.	CMOS 3.3V	≥ 10 mA	I
WDOUT	72	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	CMOS 3.3V	max. 5 mA	O
SMB_CLK	60	Clock line of System Management Bus.	CMOS 3.3V OD Suspend		I/O
SMB_DAT	62	Data line of System Management Bus.	CMOS 3.3V OD Suspend		I/O
SMB_ALERT#	64	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	CMOS 3.3V OD Suspend		I
SPKR /GP_PWM_OUT2	194	Primary functionality is output for audio enunciator, the “speaker” in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output.	CMOS 3.3V		O
BIOS_DISABLE# /BOOT_ALT#	41	Module BIOS disable input signal. Pull low to disable module's on-board BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a bootloader.	CMOS 3.3V		I
MFG_NC0 MFG_NC1 MFG_NC2 MFG_NC3 MFG_NC4	207, 209, 208, 210, 204	Do not connect on the carrier board. These pins are reserved for manufacturing purposes.	n.a.	n.a.	NC
RSVD	56, 124, 129, 130, 199, 200, 201, 202, 203	Reserved. Do not connect.	n.a.	n.a.	NC

3.21.1 Watchdog Control Signals

The Watchdog on Qseven® modules can be initialized and controlled by the API (Application Program Interface) called Embedded Application Programming Interface (EAPI). For more details about EAPI, refer to the Qseven® specification and the module vendor's EAPI Programmers Guide.

In addition to the software trigger available via EAPI, the Watchdog on a Qseven® module can be hardware-triggered by an external control circuitry. When generating a low level pulse on the Qseven® module's *'WDTRIG#'* (Watchdog trigger signal) signal, the Watchdog timer will be reset and restarted.

If the Watchdog timer has expired without a software or hardware trigger occurrence, the Qseven® module will signal this with a high level output on the *'WDOUT'* (Watchdog event indicator) signal.

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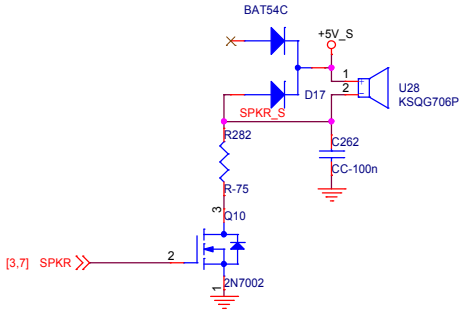
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3.21.2 PC Speaker Output

The Qseven® module provides a speaker output signal called *'SPKR',* which is intended to drive an external FET or a logic gate to connect a PC speaker. The *'SPKR'* signal can be found on the module's pin 194.

The *'SPKR'* signal is often used as a configuration strap for the module's chipset. It should not be connected to a pull-up or pull-down resistor, which could overwrite the internal chipset configuration and result in a malfunction of the module.

Figure 3-64 PC Speaker Implementation Example



3.21.3 External BIOS Flash Signal BIOS_DISABLE

Please refer to sections 3.14.4 LPC Firmware Hub and 3.16 SPI Interface Signals of this document for more information about this signal.

3.22 Thermal Management Signals

Qseven® modules provide the *'THRM#'* and *'THRMTRIP#'* signals, which are used for system thermal management. In most current system platforms, thermal management is closely associated with system power management. For more detailed information about the thermal management capabilities of the Qseven® module refer to the module's user's guide.

Table 3-42 Signal Definition Thermal Management

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
THRM#	69	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	CMOS 3.3V		I
THRMTRIP#	71	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off).	CMOS 3.3V OD		O

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3.23 Fan Control Implementation

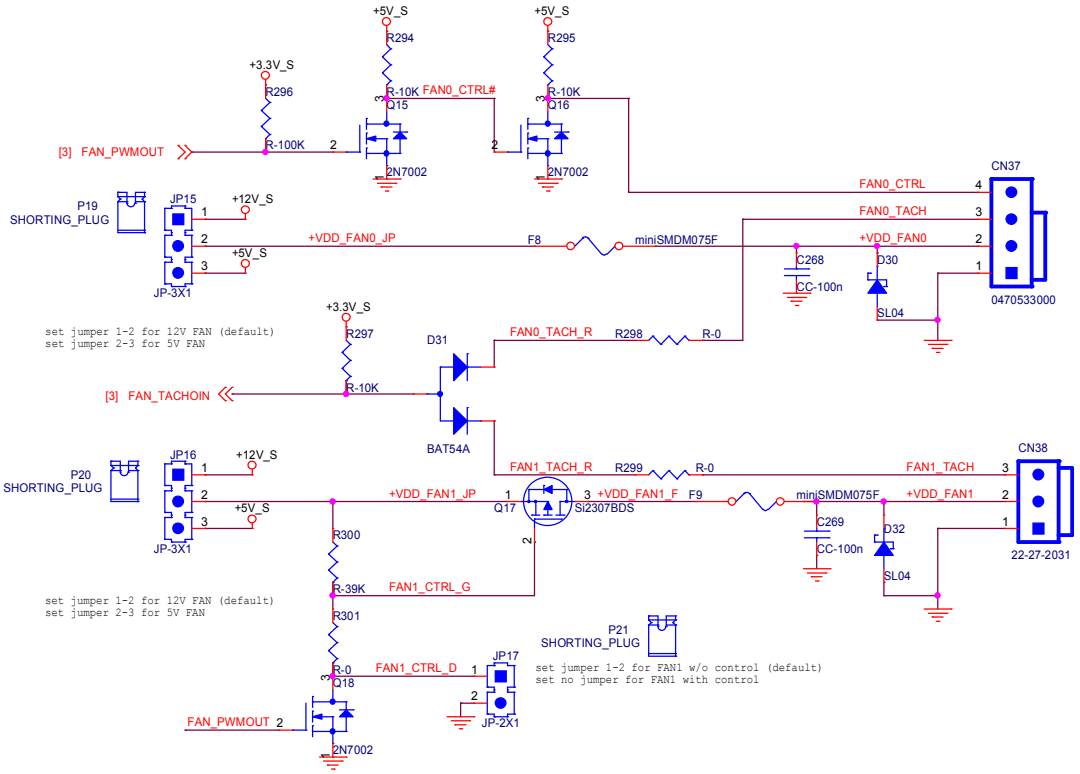
Qseven® modules provide additional support for fan speed control through the use of two signals named *'FAN_TACHOIN'* and *'FAN_PWMOUT'*. In order to easily implement fan speed control in customer specific application software, there is a software API (Application Program Interface) called Embedded Application Programming Interface (EAPI). For more information about EAPI, refer to the Qseven® specification and the Module vendor's EAPI Programmers Guide.

Table 3-43 Signal Definition Fan Control

Signal	Pin#	Description	I/O Type	I_{OL}/I_{IL}	I/O
FAN_PWMOUT / GP_PWM_OUT1	196	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output.	CMOS 3.3V OC		O
FAN_TACHOIN / GP_TIMER_IN	195	Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input.	CMOS 3.3V		I

3.23.1 Fan Control Reference Schematics

Figure 3-65 Fan speed control circuitry



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4 Layout and Design Constraints

This chapter provides routing guidelines for layout and design of a printed circuit board using high-speed interfaces such as PCI Express, Serial ATA, LVDS, Gigabit Ethernet and USB. The signal integrity rules for high-speed interfaces need to be considered. In fact, it is highly recommended that a board design simulation is performed to determine optimum layout for signal integrity and quality.

Keep in mind that this document can only highlight the most important issues that should be considered when designing a Qseven® carrier board. The designer has to take into account the relevant information (specification, design guidelines, etc.) contained in the documentation for all interfaces that are implemented on the carrier board.

Note

For more information about PCB design considerations we recommend you refer to the book "PCI Express Electrical Interconnect Design" available from Intel (http://www.intel.com/intelpress/) ISBN 0-9743649-9-1.

4.1 Microstrip or Stripline

Either edge-coupled microstrip or edge-coupled stripline are recommended for designs with differential signals.

Designs with microstrip lines offer the advantage that a lower number of layers can be used. Also, with microstrip lines it may be possible to route from a connector pad to the device pad without any via. This provides better signal quality on the signal path which connects devices. A limitation of microstrip lines is that they can only be routed on the two outside layers of the PCB, thus routing channel density is limited. In addition microstrip lines show higher far end crosstalk compared to stripline routing.

Differential striplines should be edge-coupled. Broad-side coupled striplines are not recommended due to limitations in the stackup and worse impedance control. Some PCB vendors offer better impdance control on stripline vs. microstrip lines. Stripline designs provide additional shielding since they are embedded in the board stack and are typically sandwiched between ground and/or power planes. This reduces radiation and noise coupling onto the lines. Striplines have the disadvantage that they require the use of vias to connect to them.

4.2 Printed Circuit Board Stackup Example

It is recommended to use PCBs that have a mininum of four layers. The first layer (top layer) should be used for high speed differential signaling. The bottom layer (layer 4) should be used for other periodic signals (CMOS/TTL). The dedicated power planes (layer 2 - GND and layer 3 - VCC) are required as referenced layers for high-speed signals. The solid ground plane is necessary to establish a controlled (known) impedance for the transmission line interconnects.

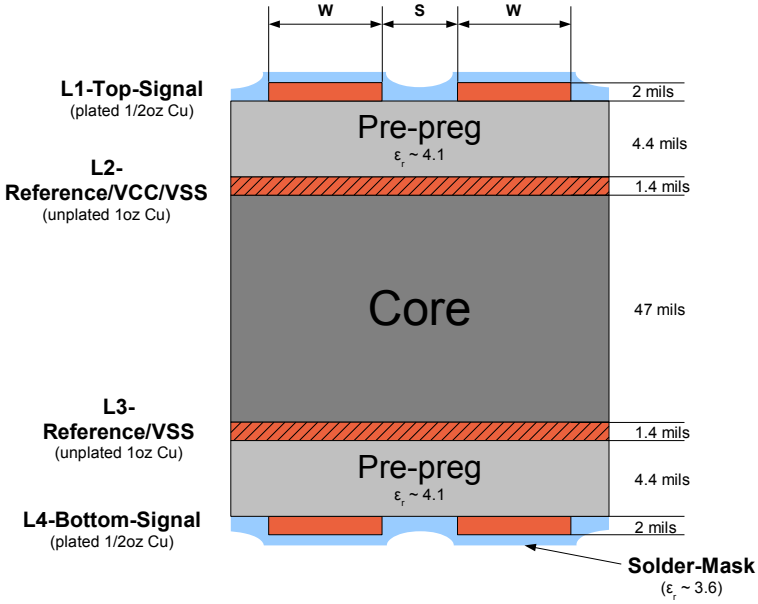
The example in Figure 4-1 shows a four layer PCB stackup using microstrip trace routing.

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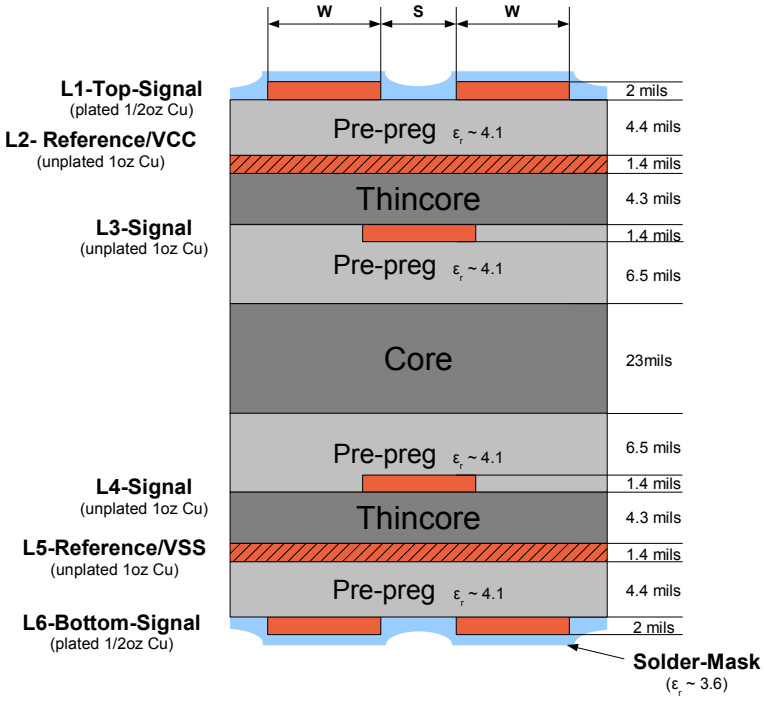
A good rule to follow for microstrip designs is to keep the value for the pre-preg thickness between signal layer and reference plane small (e.g. 4.4 mils in Figures 4-1 and 4-2). This limits crosstalk to other layers and will result in a smaller trace width that allows higher routing density. W and S need to be calculated and adjusted according to the required impedance of the traces.

Figure 4-1 4 Layer PCB Microstrip Routing



For stripline routing a PCB stackup of at least 6 layers is necessary. The internal layers (L3 and L4) can be used for routing differential signals as stripline traces while the outer layers (L1 and L6) can be used for microstrip routing.

Figure 4-2 6 Layer PCB Stripline and Microstrip Routing



For stackups with higher number of layers a narrow spacing between power and ground planes will additionally create an excellent high frequency bypass capacitance.

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4.3 General Considerations for High-Speed Differential Interfaces

The following is a list of suggestions for designing with high-speed differential signals. This should help implement these interfaces while providing maximum Qseven® carrier board performance.

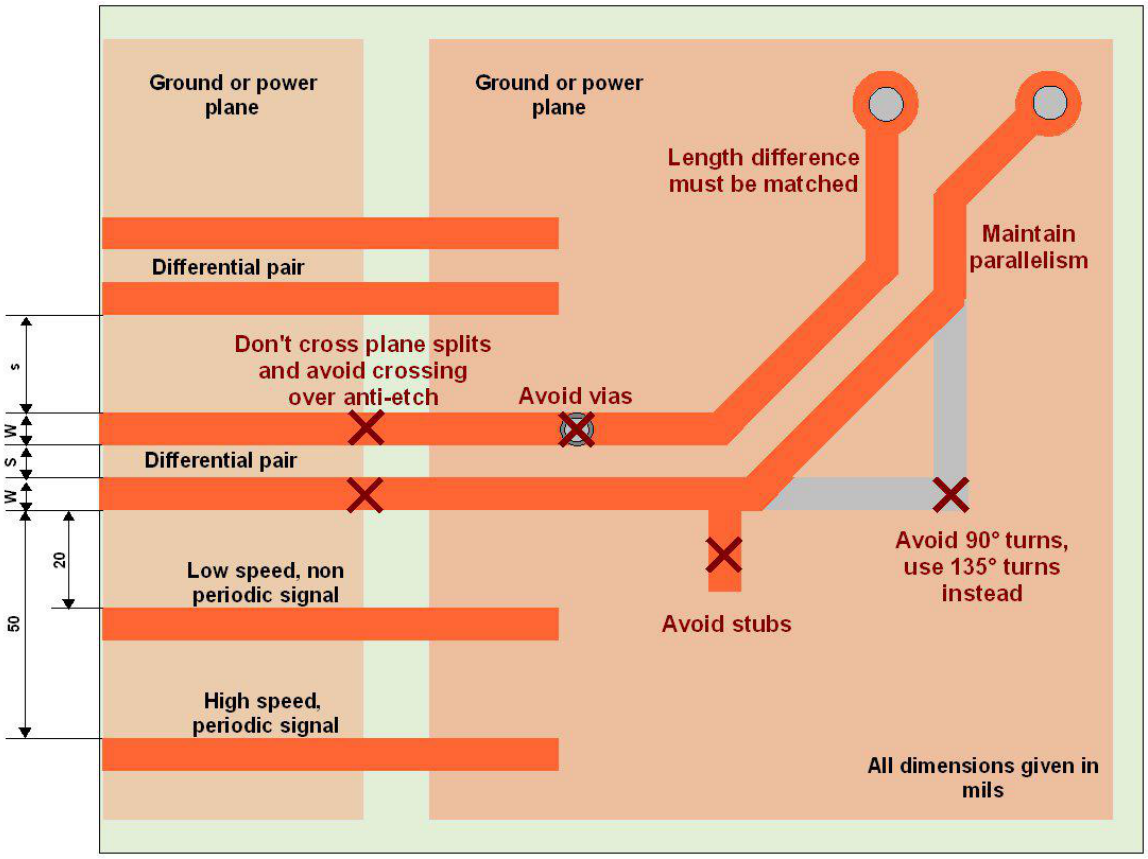
- Use controlled impedance PCB traces that match the specified differential or single ended impedance.
- Keep the trace lengths of the differential signal pairs as short as possible.
- The differential signal pair traces should be trace-length matched (intra pair trace length matching between p and n signal) and the maximum trace-length mismatch should not exceed the specified values. A length mismatch should be compensated where it occurs (Length matching per segment).
- Maintain parallelism and symmetry between differential signals with the trace spacing needed to achieve the specified differential impedance. Especially trace to via connections should be routed symmetrically.
- Maintain maximum possible separation between high speed differential pairs and any clocks/periodic signals (CMOS/TTL) and any connector going off-PCB (such as, I/O connectors, control and signal headers, or power connectors).
- Route differential signals on the signal layer nearest to the ground plane using a minimum of vias and sharp angles. This will reduce signal reflections and impedance changes. Use GND stitching vias when changing layers.
- For signal rates higher than 5Gb/s use cutouts underneath SMD pads, e. g. DC-blocking or connector SMD pads. Open the GND with the same size as the pad.
- For most stackups vias will show a capacitive behavior. Therefore larger anti-pads will improve via impedance matching.
- It is best to put CMOS/TTL and differential signals on different layer(s), which should be isolated by the power and ground planes.
- Avoid tight bends. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn.
- Do not route traces under crystals, crystal oscillators, clock synthesizers, magnetic devices or ICs that use, and/or generate clocks.
- Stubs on differential signals should be avoided due to the fact that stubs will cause signal reflections and affect signal quality.
- Keep the length of high-speed clock and periodic signal traces that run parallel to high-speed signal lines at a minimum to avoid crosstalk. The minimum suggested spacing to clock signals is 50mil.
- Use a minimum of 20mil spacing between the differential signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.
- Route all traces over continuous planes (VCC or GND) with no interruptions. Avoid crossing over small anti-etch areas if possible.
- Crossing of split planes in refencing layers should be completely avoided. This increases crosstalk, violates impedance and increases radiation level causing EMI issues.

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- Give the current return path of signals the same level of attention as the signal routing itself!

Figure 4-3 Layout Considerations



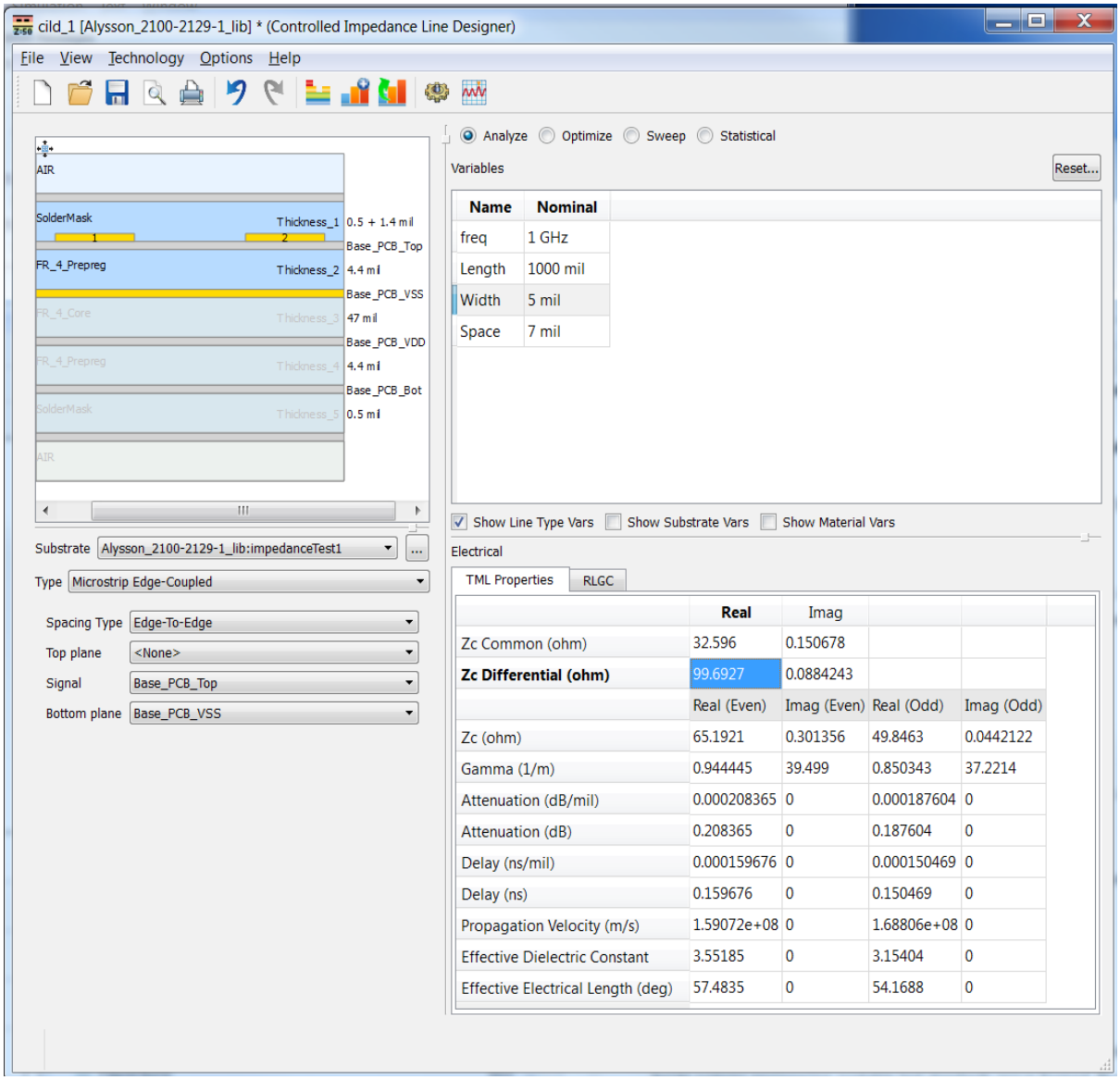
Note

In order to determine the necessary trace width, trace height and spacing to fulfill the requirements of the interface specification, it's necessary to use an impedance calculator.

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Figure 4-4 Impedance calculation example in ADS



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4.4 PCI Express Trace Routing Guidelines

Table 4-1 PCI Express Gen1/2(/3) Trace Routing Guidelines

Parameter	Trace Routing			Notes
Transfer Rate / PCIe Lane	2.5 GT/s	5.0GT/s	8-0GT/s	(1)
Signal length allowance on the Qseven® carrier board to PCIe device (solder down)	TX: 14.5 inch RX: 15.7 inch	TX: 14.5 inch RX: 15.7 inch	TX: tbd RX: tbd	(2)
Signal length allowance on the Qseven® carrier board to PCIe slot	TX: 7.7 inch RX: 7.7 inch	TX: 7.7 inch RX: 7.7 inch	TX: tbd RX: tbd	(2)
Differential Impedance	85 Ohm +/-15%			(3)
Trace width (W)	6 mil (microstrip routing)			(4)
Spacing between differential pairs (intra-pair) (S)	5 mil (microstrip routing)			(4)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 25 mil			
Spacing between TX and TX pairs (inter-pair) (s)	Min. 15 mil			(5)
Spacing between differential pairs and high-speed periodic signals	Min. 50 mil			
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mil			
Length matching inside differential pairs (intra-pair)	Max. 5 mil			
Length matching inside TX pair group (inter-pair)	Max. 7 inch, but keep difference within 3.0 inch delta to minimize latency.			(5)
Transport delay delta between Signal and Clock (including buffer delays)	11 ns			
Length matching between RX and TX pairs groups (inter-group)	No strict electrical requirements.			
Length matching between reference clock differential pairs REFCLK+ and REFCLK- (intra-pair)	Max. 5 mil			
Length matching between ref clock pairs (inter-pair)	No electrical requirements.			
Reference plane	GND referenced			
Spacing from edge of plane	Min. 40mils			
Via Usage	Max. 4 vias per TX trace Max. 2 vias per RX trace			(6)
AC coupling capacitors	The AC coupling capacitors for the TX lines are incorporated on the Qseven® module. The AC coupling capacitors for RX signal lines have to be implemented on the customer Qseven® carrier board. Capacitor type: X7R, 220nF +/-10%, 16V, shape 0402.			(7)

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Note

([1]) Column for 8GT/s is for future compatibility and will be updated once devices with 8GT/s are widely in use on Qseven.

([2]) This number is just based on signal degradation due to dielectric losses. Other factors (e. g. reflections due to stubs, crosstalk due to spacing, ...) can contribute much more to the overall signal degradation. Valid for a PCB trace attenuation of 0.4 dB/inch @ 2.5GHz (common value for FR-4 based material with loss tangent DF=0.035).

([3]) Impedance target according PCIe spec Rev. 3.0 which is valid for 2.5GT/s, 5GT/s and 8GT/s signaling.

([4]) It is recommended to use a suitable impedance calculator to determine the required parameters for the high speed signal. Stackup and material do also impact the characteristic impedance.

([5]) It is strongly recommended to route groups of TX lanes and RX lanes seperately (non interleaved). It is prefered to interleaved routing of single TX and RX lanes.

([6]) Vias should be optimized by accurate via design if more vias are required. Vias will show capacitve behaviour in most Stackups. Therefore reduction of capacitance (e.g. increased antipad size) will help. To reduce impedance mismatch the impedance tolerance should be reduced to +/-10% in such cases.

(7) 220nF used for future compatibility with PCIe @ 8GT/s.
Systems limited to 2.5GT/s and 5GT/s only may use 100nF.

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4.5 USB Trace Routing Guidelines

Table 4-2 USB 2.0 Trace Routing Guidelines

Parameter	Trace Routing	Notes
Transfer rate / Port	480 MT/s	
Signal length allowance for the Qseven® carrier board	14.0 inch	(1)
Differential Impedance	90 ohm +/-15%	
Trace width (W)	6 mil (microstrip routing)	(2)
Spacing between differential pairs (intra-pair) (S)	6 mil (microstrip routing)	(2)
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 20 mil	
Spacing between differential pairs and high-speed periodic signals	Min. 50 mil	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mil	
Length matching inside differential pair (intra-pair)	Max. 10 mil	
Reference plane	GND referenced preferred	
Spacing from edge of plane	Min. 40 mils	
Via Usage	Try to minimize number of vias	

Note

(1) This number is just based on signal degradation due to dielectric losses. Other factors (e. g. reflections due to stubs, crosstalk due to spacing, ...) can contribute much more to the overall signal degradation. Valid for a PCB trace attenuation of 0.4 dB/inch @ 2.5GHz (common value for FR-4 based material with loss tangent DF=0.035).

(2) It is recommended to use a suitable impedance calculator to determine the needed geometry of the high speed signal. Stackup and material have also impact to the characteristic impedance.

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Table 4-3 USB 3.0 SuperSpeed Trace Routing Guidelines

Parameter	Trace Routing	Notes
Transfer rate / Port	5.0GT/s	
Signal length allowance for the Qseven® carrier board	5 inch	(1)
Differential Impedance	90 ohm +/-15%	
Trace width (W)	6mil (microstrip routing) (*)	(2)
Spacing between differential pairs (intra-pair) (S)	6mil (microstrip routing) (*)	(2)
Spacing between pairs-to-pairs (inter-pair) (s)	Min. 20mil	
Spacing between differential pairs and high-speed periodic signals	Min. 50mil	
Spacing between differential pairs and low-speed non periodic signals	Min. 20mil	
Length matching inside differential pair (intra-pair)	5 mil	
Reference plane	GND referenced	
Spacing from edge of plane	Min. 40 mil	
Via Usage	Max. 2 via per differential pair	(3)

Note

(1) This number is just based on signal degradation due to dielectric losses. Other factors (e. g. reflections due to stubs, crosstalk due to spacing, ...) can contribute much more to the overall signal degradation. Valid for a PCB trace attenuation of 0.4 dB/inch @ 2.5GHz (common value for FR-4 based material with loss tangent DF=0.035).

(2) It is recommended to use a suitable impedance calculator to determine the needed geometry of the high speed signal. Stackup and material have also impact to the characteristic impedance.

(3) Vias should be optimized by accurate via design if more vias are required. Vias will show capacitve behaviour in most Stackups. Therefore reduction of capacitance (e.g. increased antipad size) will help. To reduce impedance mismatch the impedance tolerance should be reduced to +/-10% in such cases.

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4.6 TMDS Trace Routing Guidelines

Table 4-4 TMDS Trace Routing Guidelines

Parameter	Trace Routing	Notes
Transfer Rate / TMDS Lane	Up to 2.0GT/s	
Signal length allowance for the Qseven® carrier board	4.5 inch to device	(1)
Differential Impedance	100 Ohm +/-15%	
Trace width (W)	5 mil (microstrip routing)	(2)
Spacing between differential pairs (intra-pair) (S)	7 mil (microstrip routing)	(2)
Spacing between pairs-to-pair	Min. 20 mil	
Spacing between differential pairs and high-speed periodic signals	Min. 50 mil	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mil	
Length matching inside differential pair (intra-pair)	Max. 5 mil	
Length matching between differential pairs (inter-pair)	Keep difference within a 2.0 inch delta.	
Spacing from edge of plane	Min. 40 mil	
Via Usage	Max. 4 vias per differential signal trace	
AC coupling capacitors (if required)	Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.	

Note

(1) This number is just based on signal degradation due to dielectric losses. Other factors (e. g. reflections due to stubs, crosstalk due to spacing, ...) can contribute much more to the overall signal degradation. Valid for a PCB trace attenuation of 0.4 dB/inch @ 2.5GHz (common value for FR-4 based material with loss tangent DF=0.035).

(2) In order to determine the value for trace width, trace height and differential pair spacing that matches the differential impedance determined by your PCB (Stackup and Material), it's necessary to use a suitable impedance calculator.

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4.7 Display Port Trace Routing Guidelines

Table 4-5 DisplayPort Trace Routing Guidelines

Parameter	Trace Routing		Notes
Transfer Rate / DP Lane	Up to 2.7GT/s (1.1a)	Up to 5.4GT/s (1.2)	(1)
Signal length allowance for the Qseven® carrier board	4.5 inch to conn.	tbd	(2)
Differential Impedance	100 Ohm +/-15%		
Trace width (W)	5 mil (microstrip routing)		(3)
Spacing between differential pairs (intra-pair) (S)	7 mil (microstrip routing)		(3)
Spacing between pairs-to-pair	Min. 20 mil		
Spacing between differential pairs and high-speed periodic signals	Min. 50 mil		
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mil		
Length matching inside differential pair (intra-pair)	Max. 5 mil		
Length matching between differential pairs (inter-pair)	Keep difference within a 2.0 inch delta.		
Spacing from edge of plane	Min. 40 mil		
Via Usage	Max. 4 vias per differential signal trace		
AC coupling capacitors (if required)	Capacitor type: X7R, 100nF +/-10%, 16V, shape 0402.		

Note

(1) Column for 5.4GT/s is for future compatibility (DisplayPort Versions 1.2 and above only) and will be updated once devices with 5.4GT/s are widely used on Qseven.

(2) This number is just based on signal degradation due to dielectric losses. Other factors (e. g. reflections due to stubs, crosstalk due to spacing, ...) can contribute much more to the overall signal degradation. Valid for a PCB trace attenuation of 0.4 dB/inch @ 2.5GHz (common value for FR-4 based material with loss tangent DF=0.035).

(3) In order to determine the value for trace width, trace height and differential pair spacing that matches the differential impedance determined by your PCB (Stackup and Material), it's necessary to use a suitable impedance calculator.

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4.8 LAN Trace Routing Guidelines

Table 4-6 LAN Trace Routing Guidelines

Parameter	Trace Routing	Notes
Transfer Rate	1.0 GT/s (4x250MT/s)	
Signal length allowance for the Qseven® carrier board	4.0 inches to the magnetics module	(1)
Maximum signal length between isolating magnetics module and RJ45 connector on the carrier board	1.0 inch	
Differential Impedance	100 Ohm +/-15%	
Trace width (W)	5 mil (microstrip routing)	(2)
Spacing between differential pairs (intra-pair) (S)	7 mil (microstrip routing)	(2)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 50 mil	
Spacing between differential pairs and high-speed periodic signals	Min. 100 mil	
Spacing between differential pairs and low-speed non periodic signals	Min. 50 mil	
Length matching inside differential pair (intra-pair)	Max. 5 mil	
Length matching between RX and TX pairs (inter-pair)	Max. 30 mil	
Spacing between digital ground and analog ground plane (between the magnetics module and RJ45 connector)	Min. 100 mil	
Spacing from edge of plane	Min. 40 mil	
Via Usage	Max. of 2 vias	

Note

(1) This number is just based on signal degradation due to dielectric losses. Other factors (e. g. reflections due to stubs, crosstalk due to spacing, ...) can contribute much more to the overall signal degradation. Valid for a PCB trace attenuation of 0.4 dB/inch @ 2.5GHz (common value for FR-4 based material with loss tangent DF=0.035).

(2) In order to determine the value for trace width, trace height and differential pair spacing that matches the differential impedance determined by your PCB (Stackup and Material), it's necessary to use a suitable impedance calculator.

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4.9 Serial ATA Trace Routing Guidelines

Table 4-7 Serial ATA Trace Routing Guidelines

Parameter	Trace Routing			Notes
Transfer Rate	1.5GT/s	3.0GT/s	6.0GT/s	
Signal length available for the Qseven® carrier board	4.5 inch		tbd	(1)
Differential Impedance	90 Ohm +/-15%			
Trace width (W)	6 mil (microstrip routing)			(2)
Spacing between differential pairs (intra-pair) (S)	6 mil (microstrip routing)			(2)
Spacing between RX and TX pairs (inter-pair) (s)	Min. 20 mil			
Spacing between differential pairs and high-speed periodic signals	Min. 50 mil			
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mil			
Length matching inside differential pairs (intra-pair)	Max. 5 mil			
Length matching between RX and TX pairs (inter-pair)	No electrical requirement			
Spacing from edge of plane	Min. 40 mil			
Reference plane	GND			
Via usage	Max. 2 vias, recommended to use max. 1 via and SMD based SATA connector			(3)
AC Coupling capacitors	The AC coupling capacitors for the TX and RX lines are implemented on the Qseven® module.			

Note

(1) This number is just based on signal degradation due to dielectric losses. Other factors (e. g. reflections due to stubs, crosstalk due to spacing, ...) can contribute much more to the overall signal degradation. Valid for a PCB trace attenuation of 0.4 dB/inch @ 2.5GHz (common value for FR-4 based material with loss tangent DF=0.035).

(2) In order to determine the value for trace width, trace height and differential pair spacing that matches the differential impedance determined by your PCB (Stackup and Material), it's necessary to use a suitable impedance calculator.

(3) If more vias are required Vias should be optimized by accurate via design. In most Stackups vias will show capacitve behaviour. Therefore reduction of capacitance (e. g. increased antipad size) will help. To reduce impdeance mismatch the impedance tolerance should be reduced to +/-10% for such cases.

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4.10 LVDS Trace Routing Guidelines

Table 4-8 LVDS Trace Routing Guidelines

Parameter	Trace Routing	Notes
Transfer Rate	5.38 GT/s	
Signal length allowance for the Qseven® carrier board	3.8 inches to LVDS Connector (maximum LVDS cable length is 7 inches)	(1)
Differential Impedance	100 Ohm +/-15%	
Trace width (W)	5 mil (microstrip routing)	(2)
Spacing between differential pair signals (intra-pair) (S)	7 mil (microstrip routing)	(2)
Spacing between pair to pairs (inter-pair) (s)	Min. 20 mil	
Spacing between differential pairs and high-speed periodic signals	Min. 50 mil	
Spacing between differential pairs and low-speed non periodic signals	Min. 20 mil	
Length matching inside differential pairs (intra-pair)	Max. 5 mil	
Length matching between clock and data pairs (inter-pair)	Max. 20 mil	
Length matching between data pairs (inter-pair)	Max. 40 mil	
Spacing from edge of plane	Max. 40 mil	
Reference plane	GND referenced preferred	
Via Usage	Max. of 4 vias per line	

Note

(1) This number is just based on signal degradation due to dielectric losses. Other factors (e. g. reflections due to stubs, crosstalk due to spacing, ...) can contribute much more to the overall signal degradation. Valid for a PCB trace attenuation of 0.4 dB/inch @ 2.5GHz (common value for FR-4 based material with loss tangent DF=0.035).

(2) In order to determine the value for trace width, trace height and differential pair spacing that matches the differential impedance determined by your PCB (Stackup and Material), it's necessary to use a suitable impedance calculator.

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5 Industry Specifications

The list below provides links to industry specifications used to define the Qseven® interface specification.

Table 5-1 Industry Specifications

Specification	Description	Link
1000BASE T	IEEE standard 802.3ab 1000BASE T Ethernet	www.ieee.org/portal/site
ACPI	Advanced Configuration and Power Interface Specification Rev. 3.0a	www.acpi.info
DisplayID	Display Identification Data (DisplayID) Structure, Version 1.0	www.vesa.org
DisplayPort	DisplayPort Standard - Version 1.1a / Version 1.2	www.vesa.org
DVI	Digital Visual Interface, Rev 1.0, April 2, 1999, Digital Display Working Group	www.ddwg.org
ExpressCard	ExpressCard Standard Release 1.0	www.expresscard.org
HDA	High Definition Audio Specification, Rev. 1.0	www.intel.com/standards/hdaudio
I2C	The I2C Bus Specification, Version 2.1, January 2000, Philips Semiconductors, Document order number 9398 393 4001 1	www.semiconductors.philips.com
IEEE 802.3-2002	IEEE Standard for Information technology, Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications	www.ieee.org
LPC	Low Pin Count Interface Specification, Revision 1.0 (LPC)	developer.intel.com/design/chipsets/industry/lpc.htm
LVDS	Open LVDS Display Interface (Open LDI) Specification, v0.95, May 13, 1999	www.ti.com
LVDS	LVDS Owner's Manual	www.ti.com
LVDS	ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001.	www.ansi.org
PCI Express	PCI Express Base Specification, Revision 3.1, October 8, 2014, Copyright © 2002-2014 PCI Special Interest Group.	www.pcisig.com
PCI Express	PCI Express Card Electromechanical Specification, Revision 3.0 July 21, 2013 Copyright © 2002-2014 PCI Special Interest Group.	www.pcisig.com/specifications
SATA	Serial ATA: High Speed Serialized AT Attachment, Revision 3.1 July 18, 2011 Copyright © 2000-2011, APT Technologies, Inc., Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved	www.sata-io.org
Smart Battery	Smart Battery Data Specification, Revision 1.1, December 11, 1998	www.sbs-forum.org
SMBUS	System Management Bus (SMBUS) Specification, Version 2.0, August 3, 2000 Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, PowerSmart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc.	www.smbus.org
USB	Universal Serial Bus (USB) Specification, Revision 3.0	www.usb.org/home

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