Spectra IP Core ORB (ICO) Whitepaper



www.adlinktech.com
2017

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Table of Contents

1. Introduction .... P 3

2. Test Scenarios .... P 3

3. Test Environment .... P 4

4. Test Results .... P 4

5. Conclusion .... P 5

6. References .... P 6

Notices .... P 7

LRi Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

1. Introduction

ADLINK's Spectra IP Core ORB (ICO) is a standards based integration technology targeted at Field Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs). ICO is used in the latest generation of signal processing applications such as Software Defined Radio (SDR) but is equally applicable in other high performance computing applications that utilize FPGAs.

The following paper provides a set of metrics detailing the message processing performance of the latest ICO v2 product. Data is also provided to illustrate the number of logic elements and memory consumed (footprint) when implementing a simple Common Object Request. Broker Architecture (CORBA) application on an FPGA using ICO v2.

2. Test Scenarios

Performance Tests

The tests were designed to measure the CORBA message processing performance of ICO. They measure the time it takes for ICO to process CORBA requests for interfaces supporting each type of CORBA directional parameter (IN, OUT, INOUT and RETURN) and for a varying message payload size. The measurements show the time it takes to process each message from the time that the first byte of the General Inter-ORB Protocol (GIOP) message is received by the FPGA to the time that the last byte of the reply message leaves the FPGA. The times recorded do not include any time spent in the transport.

Each group of tests consists of sending bi-directional CORBA requests configured to use each of CORBA parameter directional types in turn and for a payload containing a varying size Sequence of Octets, specifically 512, 1024 2048, 4096, 8192, 16384, 32768 elements respectively. Tests were repeated for a number of different FPGA devices from Altera. These include Stratix II, III, IV and Cyclone III FPGAs.

Footprint Tests

The tests were designed to measure the number of FPGA resources consumed when implementing a CORBA application that is based on the performance test IDL (see Figure 1) described previously and using ICO. Tests were repeated for a number of different FPGA devices from Altera. These included Stratix II, III, IV and Cyclone III FPGAs.

```
interface Performance
{
   typedef sequence<octet> OctetSeq;

   void setLength (in long seqLength);
   void testOctetSeqIn (in OctetSeq inSeq);
   void testOctetSeqOut (out OctetSeq outSeq);
   void testOctetSeqInout (inout OctetSeq inoutSeq);
   OctetSeq testOctetSeqRet ();

   void shutdown ();
};
```

Figure 1 – IDL Used In Footprint Tests

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

3. Test Environment

Performance Tests

All performance tests were carried out using Modelsim Altera Edition v10.1. Messages were injected into the simulator via a software ORB (Spectra ORB) and a socket connection to the simulator. The simulator was clocked at 100MHz and the message processing times calculated. The project from the simulation was then fitted to each FPGA in turn, using the same compiler settings for each chip. Following successful fitting of the test application to each FPGA using Altera's Quartus II v10.1 synthesis tool, the maximum clock rate that the test application could run at was determined. From the base times measured in the simulator at 100Mhz and the maximum frequency value for each FPGA a set of message processing times per device was calculated.

Footprint Tests

Footprint tests were carried out using Altera's Quartus II v10.1 synthesis tool. Using the same project, with the same set of configuration settings the test design was fitted to each FPGA device considered.

4. Test Results

For each specific Altera FPGA, Table 1 provides data on the time taken to process each type of CORBA messages tested with ICO. Table 2 provides the logic consumption figures for the same performance test application used in the message processing tests.

Request Type	Octet Sequence Size	ICO v2 Stratix II Time (µS)	ICO v2 Stratix III Time (µS)	ICO v2 Stratix IV Time (µS)	ICO v2 Cyclone III Time (µS)
IN	512	0.86	0.62	0.59	1.08
IN	1024	1.49	1.07	1.02	1.88
IN	2048	2.75	1.97	1.89	3.48
IN	4096	5.27	3.79	3.62	6.67
IN	8192	10.31	7.41	14.01	13.05
IN	16384	20.39	14.66	27.86	25.81
IN	32768	40.56	29.15	41.235	51.34
INOUT	512	2.15	1.54	1.47	2.72
INOUT	1024	4.04	2.90	2.77	5.11
INOUT	2048	7.82	5.62	5.37	9.90
INOUT	4096	15.38	11.06	10.57	19.47
INOUT	8192	30.49	21.93	20.96	38.61
INOUT	16384	60.75	43.67	41.73	76.9
INOUT	32768	121.24	87.16	83.29	153.48
OUT	512	1.50`	1.08	1.03	1.90
OUT	1024	2.76	1.99	1.90	3.5
OUT	2048	5.28	3.80	3.63	6.69
OUT	4096	10.32	7.42	7.09	13.07
OUT	8192	20.41	14.67	14.02	25.83
OUT	16384	40.57	29.16	27.87	51.36
OUT	32768	80.9	58.16	55.58	102.41
RETURN	512	1.50	1.08	1.03	1.90
RETURN	1024	2.76	1.99	1.90	3.50
RETURN	2048	5.28	3.80	3.63	6.69
RETURN	4096	10.32	7.42	7.09	13.07
RETURN	8192	20.41	14.67	14.02	25.83

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

RETURN	16384	40.57	29.16	27.87	51.36
RETURN	32768	80.90	58.16	55.58	102.41

Table 1 – Spectra ICO v2 Message Processing Times

	ICO v2 Stratix II	**ICO v2 Stratix III**	**ICO v2 Stratix IV**
Logic Utilization			
Combinational ALUTs	2193	1948	2298
Dedicated logic registers	1826	1808	1987
Total Registers	1826	1808	1987
Total pins	102	102	102
Total virtual pins	0	0	0
DSP block 9-bit elements	0	0	0
Total PLLs	0	0	0
Total DLLs	0	0	0

	ICO v2 Cyclone III
Total Logic Elements	4242
Total Combinational Functions	3853
Dedicated logic registers	1923
Total Registers	1923
Total pins	102
Total virtual pins	0
DSP block 9-bit elements	0
Embedded Multiplier 9-bit elements	0

Table 2 – Spectra ICO v2 Logic Consumption

5. Conclusion

Performance

The test results show that for an IDL interface that supports a two-way synchronous CORBA call and is passed a payload of 1024 bytes as an IN parameter (implemented on a Altera Cyclone III FPGA, clocked at 160MHz), it takes approximately 1.88µS to process the message from the first byte of the incoming message being read by ICO from the transport to the last byte of the reply message being written to the transport by ICO. This represents a data throughput of over 540Mbytes/sec. At higher clock speeds and with a more powerful FPGA, for example an Altera Stratix IV, a data throughput rate of over 1Gbyte/sec can be achieved.

Footprint

The test results show that for the Altera FPGAs considered in this paper the test application consumes approximately 2% of available registers on each device. Of this 2% the majority of the logic is consumed by ICO core protocol engine. A much smaller fraction of the 2% is consumed by the server implementation logic, approximately 0.2%. This means that to add additional application instances onto the FPGA then the extra logic required increases linearly at about 0.2% per instance based on IDL used in the test application.

For the footprint tests the IDL compiler generates a memory block to cope with the largest payload (32K Sequence of Octets, INOUT), this corresponds to approximately 65 KBytes in ICO v2 to hold message header and payload information.

In summary, the footprint of ICO v2 has been highly optimized to help ensure that as much of the FPGA's resources as possible are available to accommodate the application business logic.

LRI Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

6. References

1. Software Communications Architecture 2.2.2
http://jtrs.spawar.navy.mil/sca/downloads.asp

2. CORBA/e and RT CORBA
http://www.omg.org/technology/documents/specialized_corba.htm

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000

Web: www.adlinktech.com

Email: ist_info@adlinktech.com

Notices

© 2017 ADLINK. All rights reserved. This document may be reproduced in whole but not in part. The information contained in this document is subject to change without notice and is made available in good faith without liability on the part of ADLINK Corporation. All trademarks acknowledged.

Distribuída no Brasil pela LRI | vendas@lri.com.br | 51 2129-3000