VPX6000 Series

Performance Rugged Conduction Cooled
6U VPX 4th Gen Intel® Core™ i7
Processor Blade



Manual Rev.: 1.0

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Part No: 50-15097-1000

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Revision History

Revision	Release Date	Description of Change(s)
1.0	25/04/2019	Initial release

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Preface

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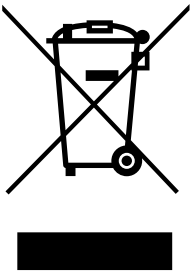
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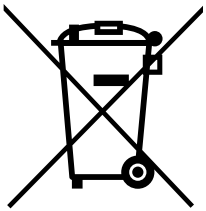
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WARNING: This product can expose you to chemicals including acrylamide, arsenic, benzene, cadmium, Tris(1,3-dichloro-2-propyl)phosphate (TDCPP), 1,4-Dioxane, formaldehyde, lead, DEHP, styrene, DINP, BBP, PVC, and vinyl materials, which are known to the State of California to cause cancer, and acrylamide, benzene, cadmium, lead, mercury, phthalates, toluene, DEHP, DIDP, DnHP, DBP, BBP, PVC, and vinyl materials, which are known to the State of California to cause birth defects or other reproductive harm. For more information go to www.P65Warnings.ca.gov**.**

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

NOTE: Additional information, aids, and tips that help users perform tasks.

CAUTION: Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

WARNING: Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

1.1 Overview

The VPX6000 is a dual-CPU 4th Generation Intel® Core™ i7 processor 6U VPX blade with Mobile Intel® QM87 Express Chipset in a rugged conduction cooled or air cooled, VPX REDI (VITA 48) form factor. The VPX6000 features two CPU sub-systems, each with up to 16GB DDR3L-1600 dual channel ECC memory soldered onboard and 32GB SLC SATA solid state drive. Rear I/O per node includes 2x 10GbE, 2x 1000BASE-BX/KX and 2x 1000BASE-T, 2x PCIe x1, HD audio (Line-in, Line-out), 3x SATA 6 Gb/s, 2x USB 3.0, 2x USB 2.0, 8x GPIO, HDMI, DVI and RS-232/422.

A VPX-R6000 Rear Transition Module is available to access rear I/O signals from the VPX6000 and a tBP-VPX6000 Test Backplane supporting five payload slots is available for users to validate VPX6000 functionality.

The VPX6000 Series is a rugged conduction/air-cooled 6U VPX blade with optional conformal coating, making it ideal for mission critical applications such as military and aerospace platforms.

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1.2 Features

- 6U VPX (VITA 46), OpenVPX (VITA 65), VPX REDI (VITA 48)
- Rugged conduction cooled 0.85" pitch 6U VPX blade with conformal coating
- Two CPU sub-systems: Node A, Node B
- 4th generation Intel® Core™ i7-4700EQ Processor (4 cores, 6M L3 cache, 2.4/1.7 GHz, 47/37W TDP)
- Dual channel DDR3L-1600 SDRAM with ECC, 16 GB per node
- Intel® QM87 Chipset
- Intel® HD Graphics 4600 with DX11.1 and OCL 1.2
- Graphics (each node):
  - 1x analog VGA port to front panel
  - 2x DVI/HDMI routed to rear (P5 for CPU-A, to P6 for CPU-B)
  - Supports three independent displays
- Onboard 32GB SLC mode SATA flash by mezzanine card per node
- SATA 6Gb/s to rear:
  - Node A: 1x SATA to P3, 2x SATA to P5
  - Node B: 1x SATA to P4, 2x SATA to P6
- I/O Ports (each node):
  - 2x 10GbE, 2x 1000BASE-T, 2x 1000BASE-BX/KX
  - 2x USB 3.0, 2x USB 2.0 to rear; 1x USB 3.0 to front panel
  - 2x RS-232/422 serial ports, 8x GPIO, PS/2 keyboard/mouse
- Expansion (each node):
  - PCIe x8 or 2x PCIe x4 to P2 (Gen2)
  - 2x PCIe x1 (Node A to P3, Node B to P4)
- uEFI BIOS 16MB flash
- Module profile: MOD6-PAY-4F1Q2U2T-12.2.1-8
- Slot Profile SLT6-PAY-4F1Q2U2T-10.2.1

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1.3 Functional Block Diagrams

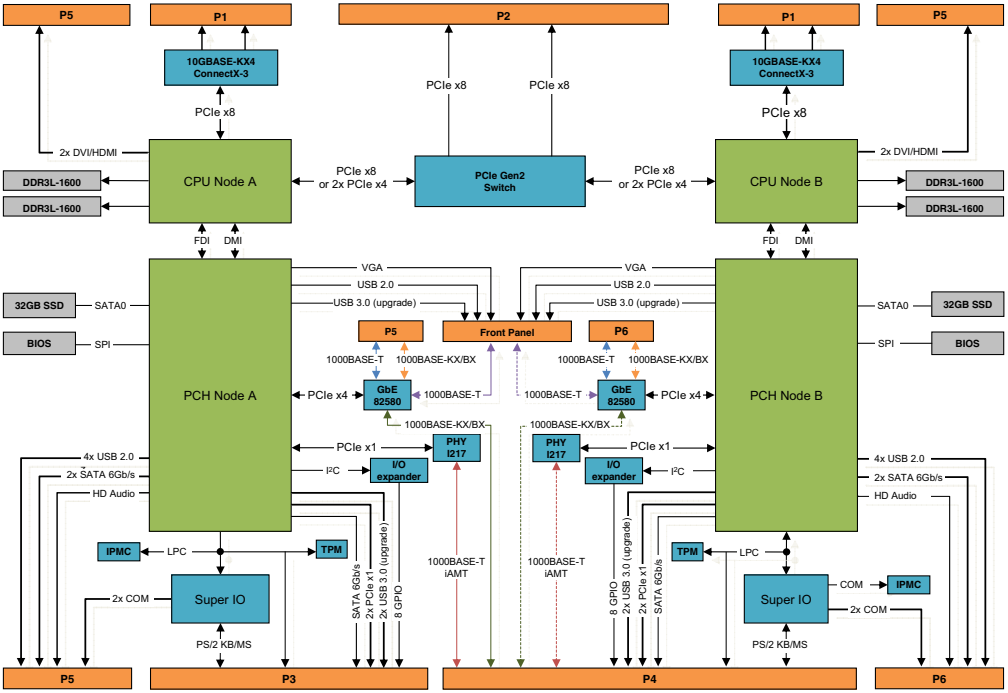


Figure 1-1: VPX6000 Functional Block Diagram

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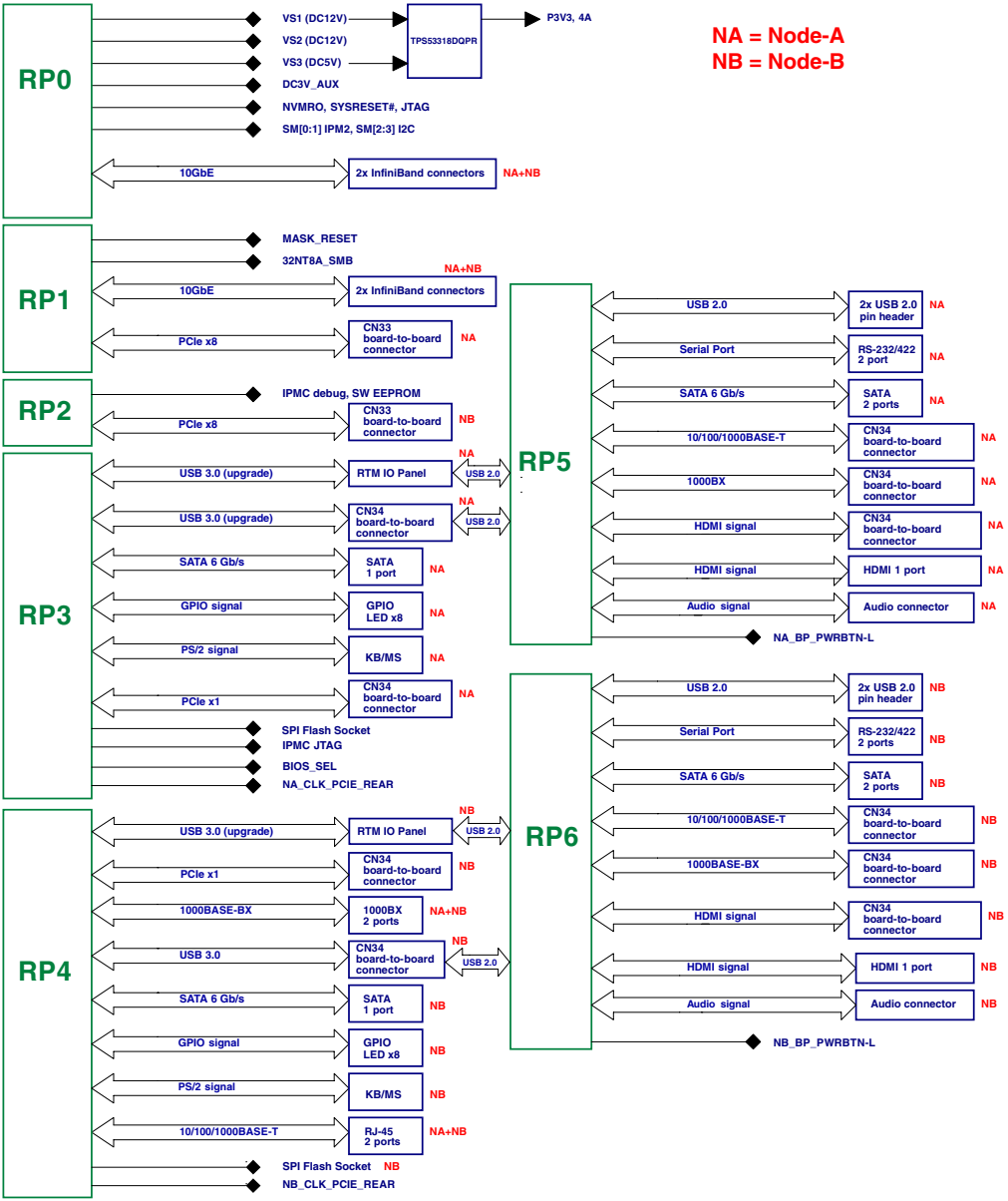


Figure 1-2: VPX-R6000 RTM Functional Block Diagram

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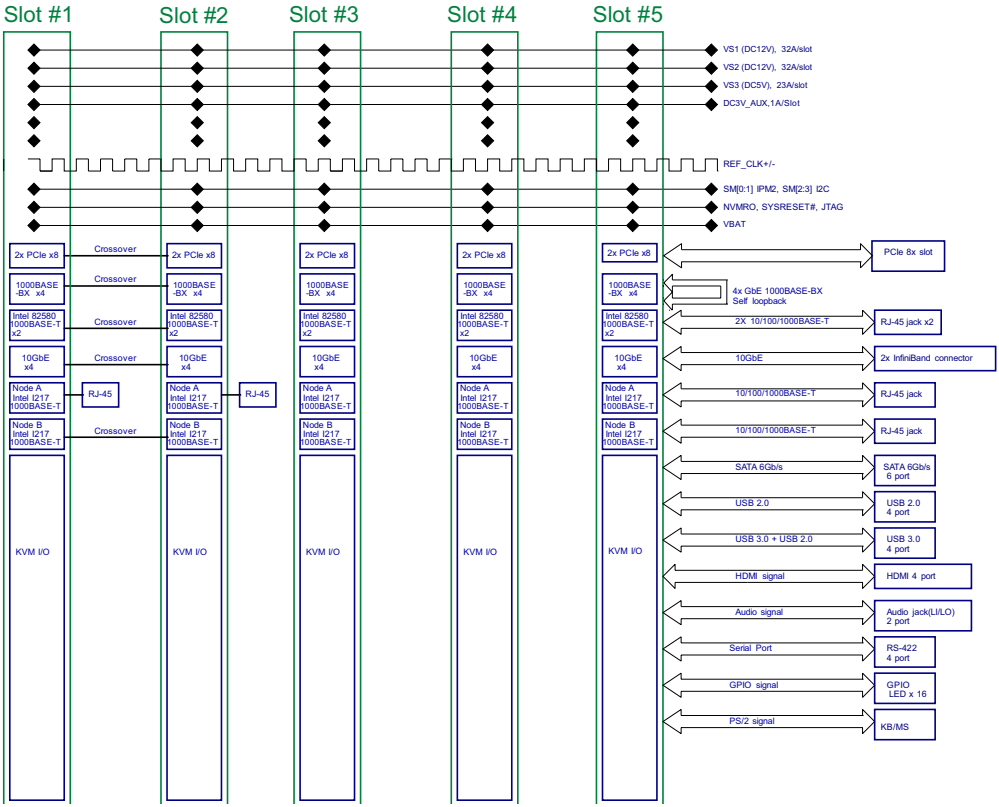
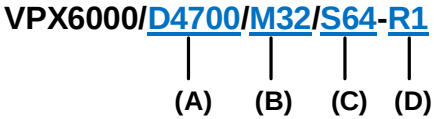


Figure 1-3: tBP-VPX6000 Test Backplane Functional Block Diagram

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1.4 Model Number Decoder - Processor Blade



(A) CPU Code

- ▷ **S4700** = Single 4-core Intel® Core™ i7-4700EQ processor
- ▷ **D4700** = Dual 2-core Intel® Core™ i7-4700EQ processor

(B) Memory Size Code

- ▷ **M16** = Onboard 16GB DDR3L-1600 memory (Node A)
- ▷ **M32** = Onboard 32GB DDR3L-1600 memory (Node A + B)

(C) SATA NAND Flash Size Code

- ▷ **S64** = Onboard 64GB (Node A + B)
- ▷ **S32** = Onboard 32GB (Node A)

(D) Ruggedized Level Code

- ▷ **R1** = Conduction cooled version supporting -40°C to +75°C at card edge
- ▷ **R2** = Conduction cooled version supporting -40°C to +85°C at card edge
- ▷ **A** = Air cooled version supporting 0°C to +60°C
- ▷ **A1** = Air cooled version supporting -40°C to +75°C
- ▷ **A2** = Air cooled vesion supporting -40°C to +85°C

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1.5 Package Contents

The VPX6000 is packaged with the following components. If any of the items on the contents list are missing or damaged, retain the shipping carton and packing material and contact the dealer for inspection. Please obtain authorization before returning any product to ADLINK. The packing contents of the VPX6000 are non-standard configurations and may vary depending on customer requests.

Processor Blade

- VPX6000
  - CPU and memory specifications will differ depending on options selected
  - Thermal module is assembled on the board
- ADLINK Driver USB Flash Drive

Rear Transition Module

- VPX-R6000 RTM

Test Backplane

- tBP-VPX6000 test backplane



The contents of non-standard VPX6000 configurations may vary depending on the customer requirements.



This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

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2 Specifications

2.1 VPX6000 Blade Specifications

VITA Standards	• 6U VPX (VITA 46) • OpenVPX (VITA 65) • VPX REDI (VITA 48)
Dual System	• Two CPU sub-systems: Node A and Node B (single node on S4700 SKU)
Processor	• Quad-core Intel® Core™ i7-4700EQ processor, 2.4/1.7GHz, 6MB L3 cache, 47/37W TDP
Chipset	• Intel® QM87 Chipset
VRD	• VRM12.5 compliant
Memory	• Dual channel DDR3L-1600 MHz with ECC soldered, max. 16GB (each node)
Data Transport (each node)	• Two Fat Pipes 10GbE to P1 for Data Plane by Mellanox ConnectX-3 • Intel® 82580EB Quad GbE Controller on PCIe x4 Gen2 • Two 1000BASE-T to P4/P5 from Node A, two to P4/P6 from Node B • Two 1000BASE-BX/KX to P4/P5 from Node A, two to P4/P6 from Node B for Control Plane • Intel® Ethernet Connection I217-LM, one GbE with Intel® AMT to rear IO
Graphics	• 1x analog VGA port to front panel • 2x DVI/HDMI routed to rear P5 for CPU-A, to P6 for CPU-B • Three independent displays supported
I/O Ports (each node)	• 2x 10GbE • 2x 1000BASE-T • 2x 1000BASE-KX • 2x USB 3.0 ports to rear, 1x USB 3.0 to front panel • 2x USB 2.0 ports • 3x SATA 6Gb/s interface • 2x RS-232/422 serial ports • 8x GPIO • PS/2 keyboard mouse
Expansion	• 1x PCIe x16 or 2x PCIe x8 or 4x PCIe x4 (Gen2) from 32-lane PCIe switch to P2 (16 lanes per node) • Four PCIe x1 ports to P3/P4 (2 lanes per node)

Table 2-1: VPX6000 Blade Specifications

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Audio	• Stereo audio, single-ended Line-in, Line-out to RTM (each node)
Super IO	ITE IT8783E/AX-L (each node) • 2 Serial ports • Keyboard/Mouse routed to RTM
BIOS	• AMI® EFI BIOS, SPI flash memory • Dual failover BIOS per node
Storage (each node)	• One 32GB SLC mode SATA flash by mezzanine card • Three SATA 6Gb/s to rear P3/P4 ,P5/P6
Watchdog Timer	• System Reset and NMI, with programmable interval via IPMC
GPIO	• 8 GPIO pins per node routed to RTM
Miscellaneous	• Front panel LEDs: CPU, PCH, RAM, P12V, P5V Power Good, Port 80 • Recessed reset button
Mechanical	• Dimensions: 233.35 mm x 160 mm (0.85" pitch) • Weight: 1407.3 g
Environmental	• Operating Temperature: ETT (R2): -40°C to +75°C air cooled CC 1 (R1): -40°C to +75°C conduction cooled CC 2 (R2): -40°C to +85°C conduction cooled • Storage Temperature: -50°C to 100°C • Humidity: 95%, non-condensing • Shock: ETT (R2): 20g peak, 11ms CC 1/2 (R1/R2): 40g peak, 11ms • Vibration: ETT (R2): Random: 0.002G2/Hz, 10~2000Hz; Sine: 2G 5~500Hz CC 1/2 (R1/R2): Random: 0.1G2/Hz, 15~2000Hz; 12Grms (MIL-STD-810F Fig 514.4-8 for aircraft) • Conformal Coating: ETT (R2): optional CC 1/2 (R1/R2): default
Operating Systems	• Microsoft Windows 7 32/64-bit • Red Hat Enterprise Linux • Wind River VxWorks 6.9.3
EMI	• CE/FCC Class A

Table 2-1: VPX6000 Blade Specifications

Note: Specifications are subject to change without prior notice.

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2.2 VPX-R6000 RTM Specifications

VITA Standards	• VITA 46.10 Rear Transition Module on VPX
Mechanical	• 233.35mm x 80mm
Front I/O	• 2x 1000BASE-BX • 2x 1000BASE-T; RJ-45 connectors • 2x 10GbE via Infiniband connectors • 2xUSB 3.0 port • 2x mini-HDMI connectors • 1x Mini UART connector
Onboard Interfaces	• 2x 10GbE via Infiniband connectors • 4x USB 2.0 by 2 headers • 1x UART header • 6x SATA connectors • Battery

Table 2-2: VPX-R6000 RTM Specifications

Note: Specifications are subject to change without prior notice.

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2.3 Power Consumption

This section provides information on the power consumption of the VPX6000.

Test Configuration (Node A / Node B)	
Processor	Intel® Core™ i7-4700EQ Processor 2.4GHz (6M L3 Cache)
Memory Channel 1	Onboard soldered memory 8GB
Memory Channel 2	Onboard soldered memory 8GB
Graphics	Intel® HD Graphics 4600
Power Supply	FSP FSP460-60PFG 460W ATX, 460W

OS / Mode*	Power Consumption (W)
DOS	70.41
Windows 7, Idle Load	43.69
Windows 7, Typical Load	123.61
Windows 7, Max. Load	129.63

Table 2-3: VPX6000 Power Consumption

Notes*:

- Idle Load: Windows 7 login prompt
- Typical Load: Run BurnInTest to execute CPU, memory, 2D/3D graphics and video playback items
- Max. Load: Run Intel TAT for maximum power consumption

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3 Functional Description

The following sections describe the VPX6000 features and functions.

3.1 Processors

The 4th Generation Intel® Core™ i7 Processor is the next generation of 64-bit, multi-core mobile processors built on 22-nanometer process technology. Based on a new micro-architecture, the processor is designed for a two-chip platform. The two-chip platform consists of a processor and Platform Controller Hub (PCH). The platform enables higher performance, lower cost, easier validation, and improved x-y footprint. The processor includes an integrated display engine, processor graphics, integrated memory controller, and integrated I/O on a single silicon die.

Features	Core™ i7-4700EQ
Clock	2.4 GHz
Max. Single Core Turbo Freq.	3.4 GHz
Last Level Cache	6 MB
No. of Cores/Threads	4/8
Maximum Power (TDP[1])	47 W
$T_{junction,MAX}$ [2]	100°C

Notes:

1. The highest expected sustainable power while running known power intensive applications. TDP is not the maximum power that the processor can dissipate.
2. The maximum supported operating temperature.

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Supported Technologies

- ▷ Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- ▶ Intel® Virtualization Technology (Intel® VT-x)
- ▶ Intel® vPro Technology (Intel® VT)
- ▶ Intel® Trusted Execution Technology (Intel® TXT)
- ▶ Intel® Hyper-Threading Technology
- ▶ Intel® 64 Architecture
- ▶ Intel® Turbo Boost Technology 2.0
- ▶ AES New Instructions
- ▶ Intel® My WiFi Technology
- ▶ Enhanced Intel SpeedStep® Technology
- ▶ Thermal Monitoring Technologies
- ▶ Intel® Fast Memory Access
- ▶ Execute Disable Bit
- ▶ Intel® VT-x with Extended Page Tables (EPT)

Interfaces

- ▶ Dual channel DDR3L memory with one channel of unbuffered SODIMM and one channel of soldered SDRAM
- ▶ Memory DDR3L data transfer rates of 1333 MT/s and 1600 MT/s
- ▶ 64-bit wide channels plus 8-bits of ECC support for each channel
- ▶ System Memory Interface I/O Voltage of 1.5V
- ▶ 1-Gb, 2-Gb, and 4-Gb DDR3L DRAM technologies supported
  - ▷ Using 4Gb DRAM device technologies, the largest memory capacity possible is 8 GB.
  - ▷ Intel Fast Memory Access:
    Just-in-Time Command Scheduling
    Command Overlap
    Out-of Order Scheduling
- ▶ The PCI Express lanes are fully-compliant with the PCI Express Base Specification, Revision 3.0, including support for 8.0 GT/s transfer speeds.

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3.2 Chipset

The VPX6000 incorporates the Mobile Intel® QM87 Chipset (Intel® DH82QM87 PCH).

Mobile Intel® QM87 Express Chipset

- PCI Express Base Specification, Revision 2.0 support for up to eight ports with transfer rate up to 5 GT/s
- ACPI Power Management Logic Support, Revision 4.0a
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated Serial ATA host controllers with independent DMA operation on up to six ports SATA 3Gb/s and up to two ports SATA 6.0 Gb/s
- Supports USB 2.0, USB 3.0
- USB host interface with two EHCI high-speed USB 2.0 Host controllers and two rate matching hubs
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for I^2C devices
- Supports Intel® Trusted Execution Technology
- Support Intel® vPro Technology
- Supports Intel® High Definition Audio
- Supports Intel® Rapid Storage Technology
- Supports Intel® Virtualization Technology for Directed I/O
- Low Pin Count (LPC) interface
- Serial Peripheral Interface (SPI) support

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3.3 Intel® Turbo Boost Technology

Intel Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating core and/or render clock frequency when there is sufficient power headroom, and the product is within specified temperature and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads. The processor supports a Turbo mode where the processor can use the thermal capacity associated with package and run at power levels higher than TDP power for short durations. This improves the system responsiveness for short, bursty usage conditions.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

3.4 Intel® Hyper Threading Technology

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology), that allows an execution core to function as two logical processors. While some execution resources (such as caches, execution units, and buses) are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support.

3.5 Real Time Clock

The Intel® QM87 PCH contains a Motorola MC146818B-compatible real-time clock (RTC) with 256 bytes of RAM. The real-time clock performs two key functions: keeping track of the time of day and storing system data. The RTC operates on a 32.768 KHz crystal and is powered by P3V3_AUX or VBAT. There is no external RTC battery on the VPX6000 to power the RTC after the system is powered off.

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4 Board Interfaces

4.1 VPX6000 Board Layout

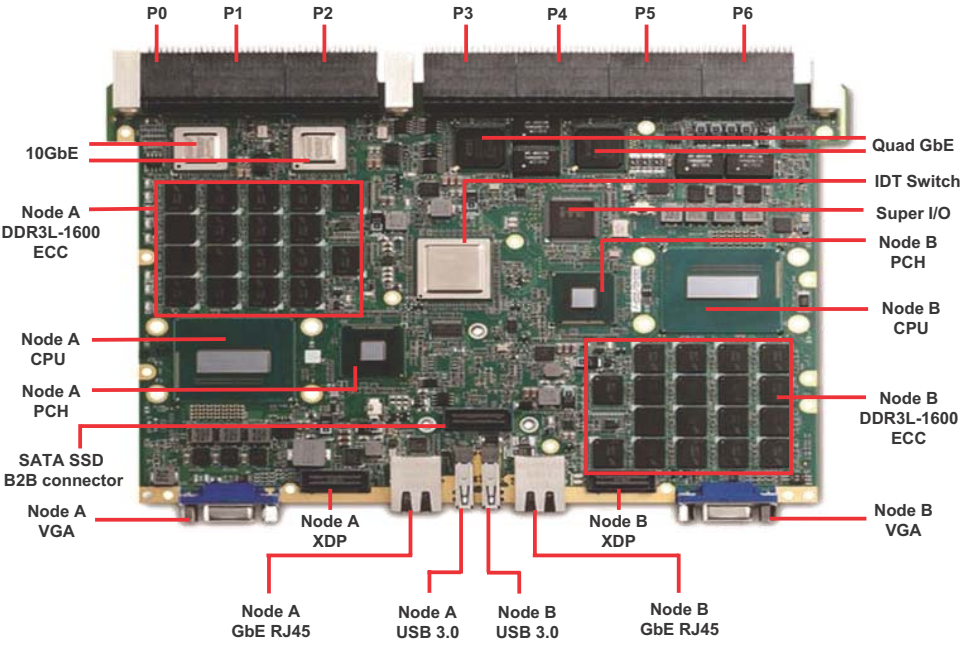


Figure 4-1: VPX6000 Board Layout - Top View



Figure 4-2: VPX6000 Front IO

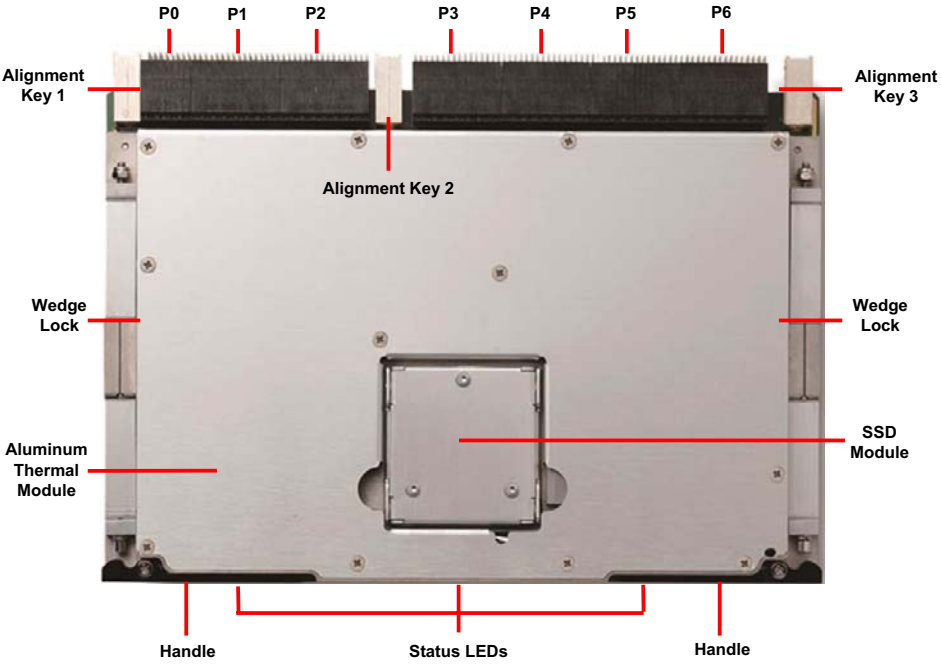
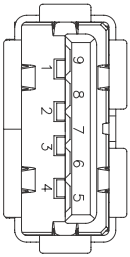


Figure 4-3: VPX6000 Board Layout - Back View

4.2 VPX6000 Onboard Connector Pin Assignments

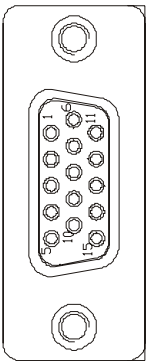
USB 3.0 Connector (Node A: CN3; Node B: CN12)

Pin #	Signal Name
1	+5V
2	Data-
3	Data+
4	GND
5	RX_N
6	RX_P
7	GND
8	TX_N
9	TX_P



DB-15 VGA Connector (Node A: CN1; Node B: CN6)

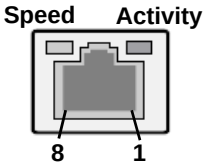
Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
+5V.	9	10	GND
N.C.	11	12	CRTDATA
HSYNC	13	14	VSYNC
CRTCLK	15		



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RJ-45 Gigabit Ethernet Connectors (CN9 and CN10)

Pin #	1000BASE-T
1	BI_DA+
2	BI_DA-
3	BI_DB+
4	BI_DC+
5	BI_DC-
6	BI_DB-
7	BI_DD+
8	BI_DD-

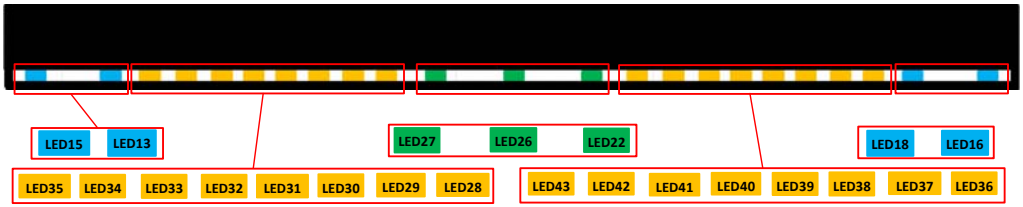


Status		Speed LED (Green/Yellow)	Activity LED (Green)
Network link is not established or system powered off		OFF	OFF
10 Mbps	Link	OFF	ON
	Active	OFF	Blinking
100 Mbps	Link	Green	ON
	Active	Green	Blinking
1000 Mbps	Link	Orange	ON
	Active	Orange	Blinking

LAN LED Status Definitions

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Status LEDs



LED Ref	Color	Description
LED15	Blue	Node A Vcore Power Good
LED13	Blue	Node A PCH P1V5 Power Good
LED28	Yellow	Node A Port 80 bit0
LED29	Yellow	Node A Port 80 bit1
LED30	Yellow	Node A Port 80 bit2
LED31	Yellow	Node A Port 80 bit3
LED32	Yellow	Node A Port 80 bit4
LED33	Yellow	Node A Port 80 bit5
LED34	Yellow	Node A Port 80 bit6
LED35	Yellow	Node A Port 80 bit7
LED18	Blue	Node B Vcore Power Good
LED16	Blue	Node B PCH P1V5 Power Good
LED36	Yellow	Node B Port 80 bit0
LED37	Yellow	Node B Port 80 bit1
LED38	Yellow	Node B Port 80 bit2
LED39	Yellow	Node B Port 80 bit3
LED40	Yellow	Node B Port 80 bit4
LED41	Yellow	Node B Port 80 bit5
LED42	Yellow	Node B Port 80 bit6
LED43	Yellow	Node B Port 80 bit7
LED26	Green	P5V Power Ready
LED27	Green	P12V Power Ready
LED22	Green	P3V3_AUX Power Ready

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4.3 VPX6000 VPX Connector Pin Assignments

P0 Connector Pin Assignment

Pin	A	B	C	D	E	F	G
1	P12V	P12V	P12V	NC	P12V	P12V	P12V
2	P12V	P12V	P12V	NC	P12V	P12V	P12V
3	P5V	P5V	P5V	NC	P5V	P5V	P5V
4	NVMRO	SYSTEM RESET	GND	NC	GND	I2C_DAT	I2C_CLK
5	IPMC_DAT	IPMC_CLK	GND	P3V3_AUX	GND	GA4	GAP
6	GA0	GA1	GND	NC	GND	GA2	GA3
7	JTAG_TRST	JTAG_TMS	GND	JTAG_TDI	JTAG_TDO	GND	JTAG_TCK
8	GND	NC	NC	GND	REF_CLK+	REF_CLK-	GND

Signal	I/O	Description
P12V	I	+12V power source
P5V	I	+5V power source
NVMRO	I/O	Non-Volatile Memory Read Only Derived by the system controller/plug in module
SYSTEM RESET	I/O	System Reset, generally input, sourced by the system controller
NC	-	Not Connected
I2C_DAT	I/O	Node A PCH SMBus data
I2C_CLK	I/O	Node A PCH SMBus clock
IPMC_DAT	I/O	IPMC I2C bus data
IPMC_CLK	I/O	IPMC I2C bus clock
P3V3_AUX	I	3.3V auxiliary power
GPA/GA[0..4]	I	Geographical Address Inputs 0-4, Parity
JTAG_*****	I/O	JTAG signals for G-LAN and PCIE-LAN
REF_CLK+/-	O	Provide 25MHz reference clock when P1 SYS_CON is low

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P1 Connector Pin Assignment

Pin	A	B	C	D	E	F	G
1	NA_10G_RX0_L0_P	NA_10G_RX0_L0_N	GND	NA_10G_TX0_L0_P	NA_10G_TX0_L0_N	GND	NC
2	GND	NA_10G_RX0_L1_P	NA_10G_RX0_L1_N	GND	NA_10G_TX0_L1_P	NA_10G_TX0_L1_N	GND
3	NA_10G_RX0_L2_P	NA_10G_RX0_L2_N	GND	NA_10G_TX0_L2_P	NA_10G_TX0_L2_N	GND	BAT_CN
4	GND	NA_10G_RX0_L3_P	NA_10G_RX0_L3_N	GND	NA_10G_TX0_L3_P	NA_10G_TX0_L3_N	GND
5	NB_10G_RX0_L0_P	NB_10G_RX0_L0_N	GND	NB_10G_TX0_L0_P	NB_10G_TX0_L0_N	GND	SYS_CON-L
6	GND	NB_10G_RX0_L1_P	NB_10G_RX0_L1_N	GND	NB_10G_TX0_L1_P	NB_10G_TX0_L1_N	GND
7	NB_10G_RX0_L2_P	NB_10G_RX0_L2_N	GND	NB_10G_TX0_L2_P	NB_10G_TX0_L2_N	GND	NC
8	GND	NB_10G_RX0_L3_P	NB_10G_RX0_L3_N	GND	NB_10G_TX0_L3_P	NB_10G_TX0_L3_N	GND
9	NA_10G_RX1_L0_P	NA_10G_RX1_L0_N	GND	NA_10G_TX1_L0_P	NA_10G_TX1_L0_N	GND	SYSBP_PWRBTN-L
10	GND	NA_10G_RX1_L1_P	NA_10G_RX1_L1_N	GND	NA_10G_TX1_L1_P	NA_10G_TX1_L1_N	GND
11	NA_10G_RX1_L2_P	NA_10G_RX1_L2_N	GND	NA_10G_TX1_L2_P	NA_10G_TX1_L2_N	GND	NC
12	GND	NA_10G_RX1_L3_P	NA_10G_RX1_L3_N	GND	NA_10G_TX1_L3_P	NA_10G_TX1_L3_N	GND
13	NB_10G_RX1_L0_P	NB_10G_RX1_L0_N	GND	NB_10G_TX1_L0_P	NB_10G_TX1_L0_N	GND	NC
14	GND	NB_10G_RX1_L1_P	NB_10G_RX1_L1_N	GND	NB_10G_TX1_L1_P	NB_10G_TX1_L1_N	GND
15	NB_10G_RX1_L2_P	NB_10G_RX1_L2_N	GND	NB_10G_TX1_L2_P	NB_10G_TX1_L2_N	GND	MASK_RESET-L
16	GND	NB_10G_RX1_L3_P	NB_10G_RX1_L3_N	GND	NB_10G_TX1_L3_P	NB_10G_TX1_L3_N	GND

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Signal	I/O	Description
BAT_CN	I	RTC battery power source
SYS_CON-L	I	Rule 4-33: The SYS_CON* line shall indicate if the module should or should not be the System Controller. SYS_CON* = grounded; indicates that this module is the System Controller SYS_CON* = open; indicates that this module is not the System Controller.
SYSBP_PWRBTN-L	I	Backplane Power Button. Drive low to assert "power button", then system boot up.
MASK_RESET-L	I	Makeable reset by software
NA_10G_TX[0/1] _L[3:0][P/N]	O	Node A 10GLAN transmit pairs from payload to backplane
NA_10G_RX[0/1] _L[3:0][P/N]	I	Node A 10GLAN receive pairs from backplane to payload
NB_10G_TX[0/1] _L[3:0][P/N]	O	Node B 10GLAN transmit pairs from payload to backplane
NB_10G_RX[0/1] _L[3:0][P/N]	I	Node B 10GLAN receive pairs from backplane to payload

Table 4-1: P1 Connector Signal Descriptions

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P2 Connector Pin Assignment

Pin	A	B	C	D	E	F	G
1	PCIE_BP1_RXP0	PCIE_BP1_RXN0	GND	PCIE_BP1_TXP0	PCIE_BP1_TXN0	GND	NC
2	GND	PCIE_BP1_RXP1	PCIE_BP1_RXN1	GND	PCIE_BP1_TXP1	PCIE_BP1_TXN1	GND
3	PCIE_BP1_RXP2	PCIE_BP1_RXN2	GND	PCIE_BP1_TXP2	PCIE_BP1_TXN2	GND	NC
4	GND	PCIE_BP1_RXP3	PCIE_BP1_RXN3	GND	PCIE_BP1_TXP3	PCIE_BP1_TXN3	GND
5	PCIE_BP2_RXP0	PCIE_BP2_RXN0	GND	PCIE_BP2_TXP0	PCIE_BP2_TXN0	GND	32NT8A_SMB_CLK
6	GND	PCIE_BP2_RXP1	PCIE_BP2_RXN1	GND	PCIE_BP2_TXP1	PCIE_BP2_TXN1	GND
7	PCIE_BP2_RXP2	PCIE_BP2_RXN2	GND	PCIE_BP2_TXP2	PCIE_BP2_TXN2	GND	32NT8A_SMB_DAT
8	GND	PCIE_BP2_RXP3	PCIE_BP2_RXN3	GND	PCIE_BP2_TXP3	PCIE_BP2_TXN3	GND
9	PCIE_BP3_RXP0	PCIE_BP3_RXN0	GND	PCIE_BP3_TXP0	PCIE_BP3_TXN0	GND	IPMI_PRG_RX
10	GND	PCIE_BP3_RXP1	PCIE_BP3_RXN1	GND	PCIE_BP3_TXP1	PCIE_BP3_TXN1	GND
11	PCIE_BP3_RXP2	PCIE_BP3_RXN2	GND	PCIE_BP3_TXP2	PCIE_BP3_TXN2	GND	IPMI_PRG_TX
12	GND	PCIE_BP3_RXP3	PCIE_BP3_RXN3	GND	PCIE_BP3_TXP3	PCIE_BP3_TXN3	GND
13	PCIE_BP4_RXP0	PCIE_BP4_RXN0	GND	PCIE_BP4_TXP0	PCIE_BP4_TXN0	GND	32NT8A_MSMBCLK
14	GND	PCIE_BP4_RXP1	PCIE_BP4_RXN1	GND	PCIE_BP4_TXP1	PCIE_BP4_TXN1	GND
15	PCIE_BP4_RXP2	PCIE_BP4_RXN2	GND	PCIE_BP4_TXP2	PCIE_BP4_TXN2	GND	32NT8A_MSMBDAT
16	GND	PCIE_BP4_RXP3	PCIE_BP4_RXN3	GND	PCIE_BP4_TXP3	PCIE_BP4_TXN3	GND

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Signal	I/O	Description
IPMI_PRG_RX / IPMI_PRG_TX	I/O	COM port for IMPC software develop
32NT8A_MSMBCLK / 32NT8A_MSMBDAT	I/O	I2C port for PCIE Switch Hub software develop
PCIE_BP1_ [N/P]TX(3:0)	O	PCIe channel A transmit pairs from payload to backplane
PCIE_BP1_ [N/P]RX(3:0)	I	PCIe channel A receive pairs from backplane to payload
PCIE_BP2_ [N/P]TX(3:0)	O	PCIe channel B transmit pairs from payload to backplane
PCIE_BP2_ [N/P]RX(3:0)	I	PCIe channel B receive pairs from backplane to payload
PCIE_BP3_[N/P]TX(3:0)	O	PCIe channel C transmit pairs from payload to backplane
PCIE_BP3_ [N/P]RX(3:0)	I	PCIe channel C receive pairs from backplane to payload
PCIE_BP4_ [N/P]TX(3:0)	O	PCIe channel D transmit pairs from payload to backplane
PCIE_BP4_ [N/P]RX(3:0)	I	PCIe channel D receive pairs from backplane to payload
32NT8A_SMB_CLK / 32NT8A_SMB_DAT	I/O	I2C port for PCIE Switch Hub software development

Table 4-2: P2 Connector Signal Descriptions

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P3 Connector Pin Assignment

Pin	A	B	C	D	E	F	G
1	NA_REAR-RXP1	NA_REAR-RXN1	GND	NA_REAR-TXP1	NA_REAR-TXN1	GND	NA_REAR_GPIO0
2	GND	NA_REAR-RXP2	NA_REAR-RXN2	GND	NA_REAR-TXP2	NA_REAR-TXN2	GND
3	NA_USB3_RX_2P	NA_USB3_RX_2N	GND	NA_USB3_TX_2P	NA_USB3_TX_2N	GND	NA_REAR_GPIO1
4	GND	NA_CLK_PCIE_REAR_P	NA_CLK_PCIE_REAR_N	GND	NA_RTM_BOOT#	NA_EXT_NODE_RST	GND
5	NA_SPI_SO_C2	NA_SPI_CS2#	GND	NA_SPI_SI_C2	NA_SPI_CLK_C2	GND	NA_REAR_GPIO2
6	GND	NA_MSCLK	NA_MSDATA	GND	NA_KBCLK	NA_KB DATA	GND
7	NA_LPC_AD0	NA_LPC_AD1	GND	NA_LPC_AD2	NA_LPC_AD3	GND	NA_REAR_GPIO3
8	GND	NA_LPC_FRAME-L	NA_CLK33_DBC	GND	NC	NA_PLTRST_BIOS-L	GND
9	NA_USB3_RX_5P	NA_USB3_RX_5N	GND	NA_USB3_TX_5P	NA_USB3_TX_5N	GND	NA_REAR_GPIO4
10	GND	NA_SATA_RXP3	NA_SATA_RXN3	GND	NA_SATA_TXP3	NA_SATA_TXN3	GND
11	PROG_TDI	PROG_TDO	GND	PROG_TMS	PROG_JTAG_VPX_TCK	GND	NA_REAR_GPIO5
12	GND	PROG_TDO_CTRL	NC	GND	NC	NC	GND
13	NC	NC	GND	NC	NC	GND	NA_REAR_GPIO6
14	GND	NA_BIOS_SEL1#	NB_BIOS_SEL1#	GND	NC	NC	GND
15	NC	NC	GND	NC	NC	GND	NA_REAR_GPIO7
16	GND	P12V	P12V	GND	P5V	P5V	GND

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Signal	I/O	Description
NA_REAR-RX[P/N]1	I	Node A PCIe port1 receive pair from backplane to PCH
NA_REAR-TX[P/N]1	O	Node A PCIe port1 transmit pair from PCH to backplane
NA_REAR-RX[P/N]2	I	Node A PCIe port2 receive pair from backplane to PCH
NA_REAR-TX[P/N]2	O	Node A PCIe port2 transmit pair from PCH to backplane
NA_REAR_GPIO[0:7]	I/O	Node A General Purpose IO, Channels 0-7
NA_USB3_RX_2[P/N]	I	Node A USB 3.0 port receive pair from backplane to PCH
NA_USB3_TX_2[P/N]	O	Node A USB 3.0 port transmit pair from PCH to backplane
NA_USB3_RX_5[P/N]	I	Node A USB 3.0 port receive pair from backplane to PCH
NA_USB3_TX_5[P/N]	O	Node A USB 3.0 port transmit pair from PCH to backplane
NA_RTM_BOOT#	I	Node A boot up from RTM BIOS when this pin pull low
NA_EXT_NODE_RST	I	Node A reset input
NA_SATA_RX[P/N]3	I	Node A SATA 6Gb/s port receive pair from backplane to PCH
NA_SATA_TX[P/N]3	O	Node A SATA 6Gb/s port transmit pair from PCH to backplane
NA_SPI_*	I/O	Node A SPI bus for RTM BIOS
NA_LPC_*	I/O	Node A LPC bus for RTM debug port
NA_MSCLK	I/O	Node A PS2 bus mouse signal clock
NA_MSDATA	I/O	Node A PS2 bus mouse signal data
NA_KBCLK	I/O	Node A PS2 bus keyboard signal clock
NA_KBDATA	I/O	Node A PS2 bus keyboard signal data
PROG_*	I/O	IPMC JTAG PORT
NA_CLK_PCIE_REAR_[P/N]	I/O	Node A PCIe reference clock
P12V	I	+12V Power source
P5V	I	+5V Power source
NA_BIOS_SEL1#	I	Boot from BIOS2 of Node A when this signal is low
NB_BIOS_SEL1#	I	Boot from BIOS2 of Node B when this signal is low

Table 4-3: P3 Connector Signal Descriptions

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P4 Connector Pin Assignment

Pin	A	B	C	D	E	F	G
1	NB_REAR-RXP1	NB_REAR-RXN1	GND	NB_REAR-TXP1	NB_REAR-TXN1	GND	NB_REAR_GPIO0
2	GND	NB_REAR-RXP2	NB_REAR-RXN2	GND	NB_REAR-TXP2	NB_REAR-TXN2	GND
3	NB_USB3_RX_2P	NB_USB3_RX_2N	GND	NB_USB3_TX_2P	NB_USB3_TX_2N	GND	NB_REAR_GPIO1
4	GND	NB_CLK_PCIE_REAR_P	NB_CLK_PCIE_REAR_N	GND	NB_RTM_BOOT#	NB_EXT_NODE_RST	GND
5	NB_SPI_SO_C2	NB_SPI_CS2#	GND	NB_SPI_SI_C2	NB_SPI_CLK_C2	GND	NB_REAR_GPIO2
6	GND	NB_MSCLK	NB_MSDATA	GND	NB_KBCLK	NB_KBDATA	GND
7	NB_LPC_AD0	NB_LPC_AD1	GND	NB_LPC_AD2	NB_LPC_AD3	GND	NB_REAR_GPIO3
8	GND	NB_LPC_FRAME-L	NB_CLK33_DBC	GND	NC	NB_PLTRST_BIOS-L	GND
9	NB_USB3_RX_5P	NB_USB3_RX_5N	GND	NB_USB3_TX_5P	NB_USB3_TX_5N	GND	NB_REAR_GPIO4
10	GND	NB_SATA_RXP3	NB_SATA_RXN3	GND	NB_SATA_TXP3	NB_SATA_TXN3	GND
11	NB_GLAN_KXR0_P	NB_GLAN_KXR0_N	GND	NB_GLAN_KXT0_P	NB_GLAN_KXT0_N	GND	NB_REAR_GPIO5
12	GND	NA_GLAN_KXR0_P	NA_GLAN_KXR0_N	GND	NA_GLAN_KXT0_P	NA_GLAN_KXT0_N	GND
13	MXA1-P	MXA1-N	GND	MXB1-P	MXB1-N	GND	NB_REAR_GPIO6
14	GND	MXC1-P	MXC1-N	GND	MXD1-P	MXD1-N	GND
15	MXA0-P	MXA0-N	GND	MXB0-P	MXB0-N	GND	NB_REAR_GPIO7
16	GND	MXC0-P	MXC0-N	GND	MXD0-P	MXD0-N	GND

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Signal	I/O	Description
NB_REAR-RX[P/N]1	I	Node B PCIe port1 receive pair from backplane to PCH
NB_REAR-TX[P/N]1	O	Node B PCIe port1 transmit pair from PCH to backplane
NB_REAR-RX[P/N]2	I	Node B PCIe port2 receive pair from backplane to PCH
NB_REAR-TX[P/N]2	O	Node B PCIe port2 transmit pair from PCH to backplane
NB_REAR_GPIO[0:7]	I/O	Node B General Purpose IO, Channels 0-7
NB_USB3_RX_2[P/N]	I	Node B USB 3.0 port receive pair from backplane to PCH
NB_USB3_TX_2[P/N]	O	Node B USB 3.0 port transmit pair from PCH to backplane
NB_USB3_RX_5[P/N]	I	Node B USB 3.0 port receive pair from backplane to PCH
NB_USB3_TX_5[P/N]	O	Node B USB 3.0 port transmit pair from PCH to backplane
NB_RTM_BOOT#	I	Node B boot up from RTM BIOS when this pin pull low
NB_EXT_NODE_RST	I	Node B reset input
NB_SATA_RX[P/N]3	I	Node B SATA 6Gb/s port receive pair from backplane to PCH
NB_SATA_TX[P/N]3	O	Node B SATA 6Gb/s port transmit pair from PCH to backplane
NB_SPI_*	I/O	Node B SPI bus for RTM BIOS
NB_LPC_*	I/O	Node B LPC bus for RTM debug port
NB_MSCLK	I/O	Node B PS2 bus mouse signal clock
NB_MSDATA	I/O	Node B PS2 bus mouse signal data
NB_KBCLK	I/O	Node B PS2 bus keyboard signal clock
NB_KBDATA	I/O	Node B PS2 bus keyboard signal data
MX[A:D]0-[P/N]	I/O	Node A 1Gb BASE-T Ethernet
MX[A:D]1-[P/N]	I/O	Node B 1Gb BASE-T Ethernet
NA_GLAN_KX[R/T]0 _[P/N]	I/O	Node A 1Gb BASE-KX Ethernet
NB_GLAN_KX[R/T]0 _[P/N]	I/O	Node B 1Gb BASE-KX Ethernet
NC		Not Connected
NB_CLK_PCIE_REAR _[P/N]	O	Node B PCIE reference clock

Table 4-4: P4 Connector Signal Descriptions

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P5 Connector Pin Assignment

Pin	A	B	C	D	E	F	G
1	NA_USB2-P2	NA_USB2-N2	GND	NA_USB2-P4	NA_USB2-N4	GND	NA_USB PWR1
2	GND	NA_USB2-P6	NA_USB2-N6	GND	NA_USB2-P9	NA_USB2-N9	GND
3	NA_COM1_RTS/TXP	NA_COM1_TXD/TXN	GND	NA_COM1_CTS/RXP	NA_COM1_RXD/RXN	GND	NA_USB PWR2
4	GND	NA_COM2_RTS/TXP	NA_COM2_TXD/TXN	GND	NA_COM2_CTS/RXP	NA_COM2_RXD/RXN	GND
5	NA_SATA_RXP1	NA_SATA_RXN1	GND	NA_SATA_TXP1	NA_SATA_TXN1	GND	NA_USB PWR3
6	GND	NA_SATA_RXP2	NA_SATA_RXN2	GND	NA_SATA_TXP2	NA_SATA_TXN2	GND
7	MXA11-P	MXA11-N	GND	MXB11-P	MXB11-N	GND	NA_USB PWR4
8	GND	MXC11-P	MXC11-N	GND	MXD11-P	MXD11-N	GND
9	NA_PCH_SPKR	NA_AGND_AU	GND	NA_BP_PWRBTN-L	NA_AGND_AU	GND	NA_DVI_HPD0
10	GND	NA_HP_R	NA_HP_L	GND	NA_L_IN_R	NA_L_IN_L	GND
11	NA_TMDSB_DATA0_P	NA_TMDSB_DATA0_N	GND	NA_TMDSB_CLK_P	NA_TMDSB_CLK_N	GND	NA_DVI_SCL0
12	GND	NA_TMDSB_DATA2_P	NA_TMDSB_DATA2_N	GND	NA_TMDSB_DATA1_P	NA_TMDSB_DATA1_N	GND
13	NA_TMDSC_DATA0_P	NA_TMDSC_DATA0_N	GND	NA_TMDSC_CLK_P	NA_TMDSC_CLK_N	GND	NA_DVI_SDA0
14	GND	NA_TMDSC_DATA2_P	NA_TMDSC_DATA2_N	GND	NA_TMDSC_DATA1_P	NA_TMDSC_DATA1_N	GND
15	NC	NA_DVI_HPD1	GND	NA_DVI_SCL1	NA_DVI_SDA1	GND	NA_P5V_DVI
16	GND	NA_GLAN_KXR1_P	NA_GLAN_KXR1_N	GND	NA_GLAN_KXT1_P	NA_GLAN_KXT1_N	GND

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Signal	I/O	Description
NA_USB2-[P/N]2 NA_USB2-[P/N]4 NA_USB2-[P/N]6 NA_USB2-[P/N]8	I/O	Node A USB 2.0 port connect to PCH
NA_USBPWR[1:4]	O	USB port power +5V
NA_COM[1:2]_RTS/TXP	O	Node A Serial Comms Channel (1/2) RTS Transmit Pos
NA_COM[1:2]_TXD/TXN	O	Node A Serial Comms Channel (1/2) Transmit Data Neg
NA_COM[1:2]_CTS/RXP	I	Node A Serial Comms Channel (1/2) CTS Receive Pos
NA_COM[1:2]_RXD/RXN	I	Node A Serial Comms Channel (1/2) Receive Data Neg
NA_SATA_RX[P/N]1	I	Node A SATA 6Gb/s port receive pair from backplane to PCH
NA_SATA_TX[P/N]1	O	Node A SATA 6Gb/s port transmit pair from PCH to backplane
NA_SATA_RX[P/N]2	I	Node A SATA 6Gb/s port receive pair from backplane to PCH
NA_SATA_TX[P/N]2	O	Node A SATA 6Gb/s port transmit pair from PCH to backplane
MX[A:D]11-[P/N]	I/O	Node A 1000BASE-Tx Nodal Ethernet
NA_GLAN_KX[R/T]1_[P/N]	I/O	Node A 1Gb BASE-KX Ethernet
NA_PCH_SPKR	O	Node A audio speaker output
NA_AGND_AU	GND	Node A audio ground
NA_BP_PWRBTN-L	I	Node A power button input
NA_HP_[R/L]	O	Node A audio line output
NA_L_IN_[R/L]	I	Node A audio line input
NA_TMDSB_*	O	Node A HDMI/DVI output 1
NA_TMDSC_*	O	Node A HDMI/DVI output 2
NA_DVI_HPD[0:1]	I	Node A DVI channel 0/1 Hot Plug Detect
NA_DVI_SCL[0:1]	I/O	Node A DVI channel 0/1 DDC Clock
NA_DVI_SDA[0:1]	I/O	Node A DVI channel 0/1 DDC Data
NA_P5V_DVI	O	Node A DDC 5V
NC		Not Connected

Table 4-5: P5 Connector Signal Descriptions

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P6 Connector Pin Assignment

Pin	A	B	C	D	E	F	G
1	NB_USB2-P2	NB_USB2-N2	GND	NB_USB2-P4	NB_USB2-N4	GND	NB_USB PWR1
2	GND	NB_USB2-P6	NB_USB2-N6	GND	NB_USB2-P9	NB_USB2-N9	GND
3	NB_COM1_RTS/TXP	NB_COM1_TXD/TXN	GND	NB_COM1_CTS/RXP	NB_COM1_RXD/RXN	GND	NB_USB PWR2
4	GND	NB_COM2_RTS/TXP	NB_COM2_TXD/TXN	GND	NB_COM2_CTS/RXP	NB_COM2_RXD/RXN	GND
5	NB_SATA_RXP1	NB_SATA_RXN1	GND	NB_SATA_TXP1	NB_SATA_TXN1	GND	NB_USB PWR3
6	GND	NB_SATA_RXP2	NB_SATA_RXN2	GND	NB_SATA_TXP2	NB_SATA_TXN2	GND
7	MXA10-P	MXA10-N	GND	MXB10-P	MXB10-N	GND	NB_USB PWR4
8	GND	MXC10-P	MXC10-N	GND	MXD10-P	MXD10-N	GND
9	NB_PCH_SPKR	NB_AGND_AU	GND	NB_BP_PWRBTN-L	NB_AGND_AU	GND	NB_DVI_HPD0
10	GND	NB_HP_R	NB_HP_L	GND	NB_L_IN_R	NB_L_IN_L	GND
11	NB_TMDSB_DATA0_P	NB_TMDSB_DATA0_N	GND	NB_TMDSB_CLK_P	NB_TMDSB_CLK_N	GND	NB_DVI_SCL0
12	GND	NB_TMDSB_DATA2_P	NB_TMDSB_DATA2_N	GND	NB_TMDSB_DATA1_P	NB_TMDSB_DATA1_N	GND
13	NB_TMDSC_DATA0_P	NB_TMDSC_DATA0_N	GND	NB_TMDSC_CLK_P	NB_TMDSC_CLK_N	GND	NB_DVI_SDA0
14	GND	NB_TMDSC_DATA2_P	NB_TMDSC_DATA2_N	GND	NB_TMDSC_DATA1_P	NB_TMDSC_DATA1_N	GND
15	NC	NB_DVI_HPD1	GND	NB_DVI_SCL1	NB_DVI_SDA1	GND	NB_P5V_DVI
16	GND	NB_GLAN_KXR1_P	NB_GLAN_KXR1_N	GND	NB_GLAN_KXT1_P	NB_GLAN_KXT1_N	GND

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Signal	I/O	Description
NB_USB2-[P/N]2 NB_USB2-[P/N]4 NB_USB2-[P/N]6 NB_USB2-[P/N]8	I/O	Node B USB 2.0 port connect to PCH
NB_USBPWR[1:4]	O	USB Port Power +5V
NB_COM[1:2]_RTS/TXP	O	Node B Serial Comms Channel (1/2) RTS Transmit Pos
NB_COM[1:2]_TXD/TXN	O	Node B Serial Comms Channel (1/2) Transmit Data Neg
NB_COM[1:2]_CTS/RXP	I	Node B Serial Comms Channel (1/2) CTS Receive Pos
NB_COM[1:2]_RXD/RXN	I	Node B Serial Comms Channel (1/2) Receive Data Neg
NB_SATA_RX[P/N]1	I	Node B SATA 6Gb/s port receive pair from backplane to PCH
NB_SATA_TX[P/N]1	O	Node B SATA 6Gb/s port transmit pair from PCH to backplane
NB_SATA_RX[P/N]2	I	Node B SATA 6Gb/s port receive pair from backplane to PCH
NB_SATA_TX[P/N]2	O	Node B SATA 6Gb/s port transmit pair from PCH to backplane
MX[A:D]11-[P/N]	I/O	Node B 1000BASE-Tx Nodal Ethernet
NB_GLAN_KX[R/T]1_[P/N]	I/O	Node B 1Gb BASE-KX Ethernet
NB_PCH_SPKR	O	Node B audio speaker output
NB_AGND_AU	GND	Node B Audio Ground
NB_BP_PWRBTN-L	I	Node B power button input
NB_HP_[R/L]	O	Node B audio LINE output
NB_L_IN_[R/L]	I	Node B audio LINE input
NB_TMDSB_*	O	Node B HDMI/DVI output 1
NB_TMDSC_*	O	Node B HDMI/DVI output 2
NB_DVI_HPD[0:1]	I	Node B DVI channel 0/1 Hot Plug Detect
NB_DVI_SCL[0:1]	I/O	Node B DVI channel 0/1 DDC Clock
NB_DVI_SDA[0:1]	I/O	Node B DVI channel 0/1 DDC Data
NB_P5V_DVI	O	Node B DDC 5V

Table 4-6: P6 Connector Signal Descriptions

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4.4 tBP-VPX6000 Board Layout

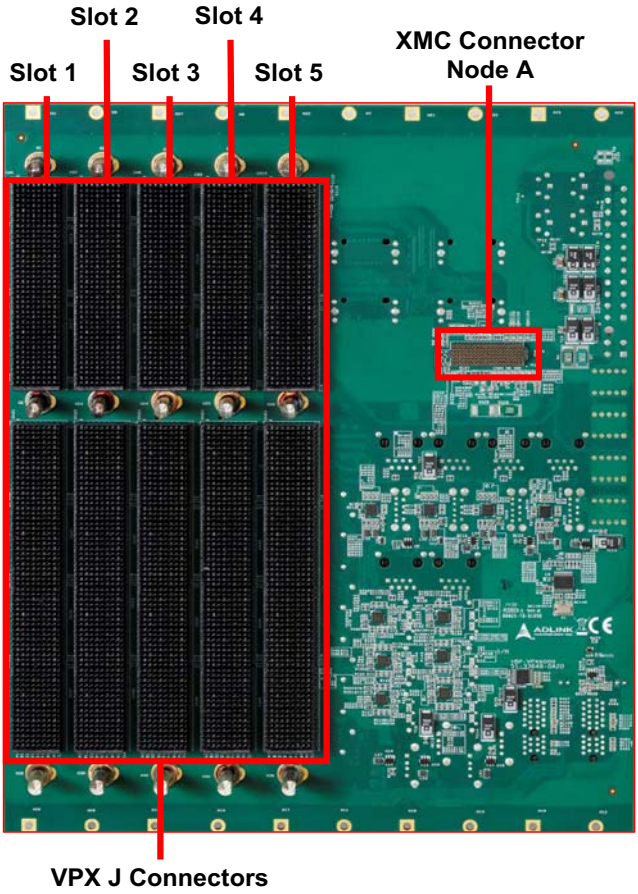


Figure 4-4: tBP-VPX6000 Board Layout - Front View

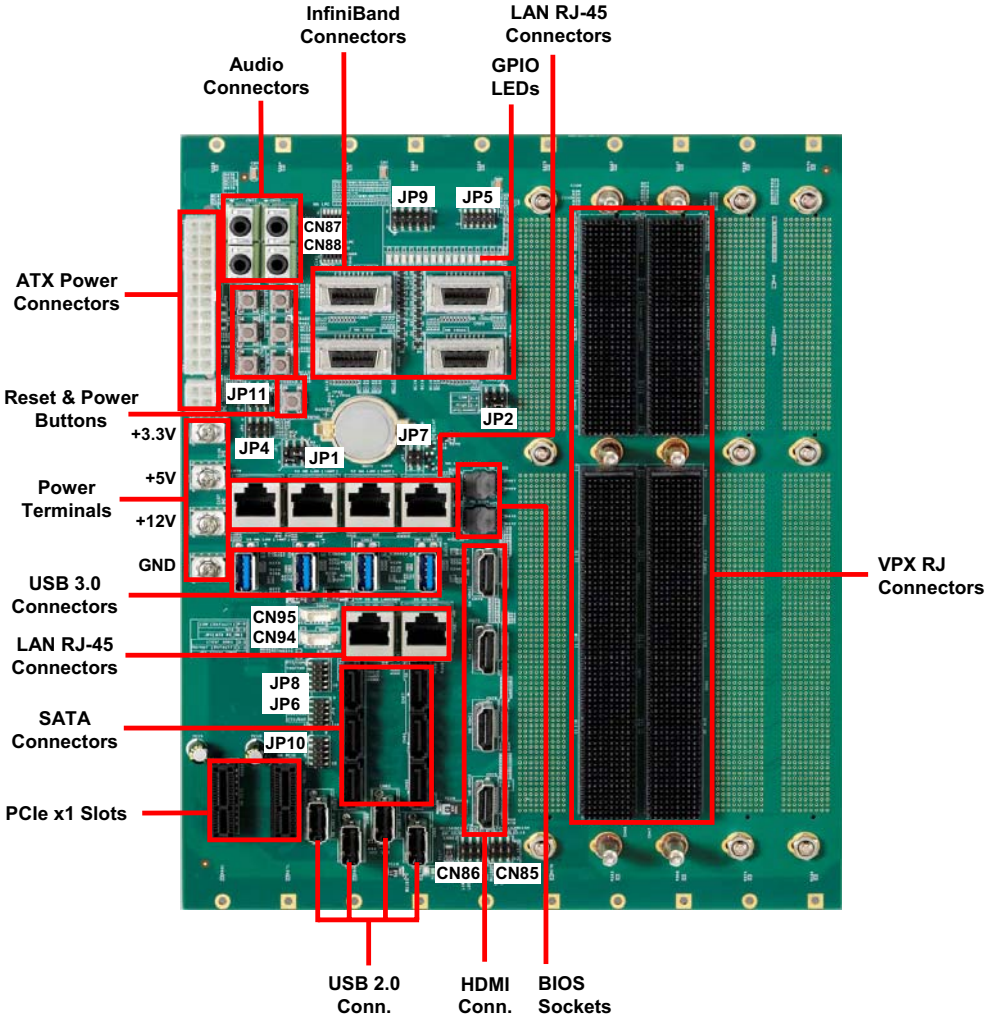


Figure 4-5: tBP-VPX6000 Board Layout - Rear View

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Connector	Description
JP1	BIOS Select Jumper
JP2	NVMRO Jumper
JP5	Speaker Out Connector
JP6/JP8	COM Connectors
JP7	Speaker Out Connector
JP9	IPMC JTAG Connector
JP10	IPMC UART Connector
JP11	VPX JTAG Connector
CN85/CN86	Keyboard/Mouse Connector
CN87/CN88	LPC Connector
CN94/CN95	VPX SM Connector

Table 4-7: tBP-VPX6000 Rear Connectors

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Signal	Connection to/from
USB 3.0	Slot5
USB 2.0	Slot5
HDMI	Slot5
DVI	Slot5
Gigabit Ethernet	Slot1,2,5
SATA	Slot5
XMC	Slot5
InfiniBand	Slot5
Line In	Slot5 (Node A: CN69; Node B: CN72)
Line Out	Slot5 (Node A: CN70; Node B:CN71)
IDT Switch Hub I2C	Slot5
BIOS Select	Slot5
COM	Slot5
IPMC JTAG	Slot5
VPX JTAG	Slot5
Speaker Out	Slot5
LPC Debug Port	Slot5
VPX SM	Slot5
IPMC UART	Slot5
Keyboard / Mouse	Slot5
Reset Button	Slot5
Power Button	Slot5
VPX J	Slot 1-5
VPX RJ	Slot 3,4
RTC and PSON	Battery and ATX power connector

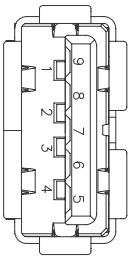
Table 4-8: tBP-VPX6000 Signal Routing Table

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4.5 tBP-VPX6000 Connector Pin Assignments

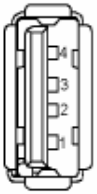
USB 3.0 Connector
(Node A: CN61, CN63; Node B: CN65,CN67)

Pin #	Signal Name
1	+5V
2	Data-
3	Data+
4	GND
5	RX_N
6	RX_P
7	GND
8	TX_N
9	TX_P



USB Connectors
(Node A: CN62,CN64; Node B: CN66,CN68)

Pin #	Signal Name
1	Vcc
2	USB-
3	USB+
4	GND



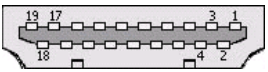
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SATA 7-pin Connector
(Node A: CN55-CN57; Node B CN58-CN60)

Pin #	Signal
1	GND
2	TXP
3	TXN
4	GND
5	RXN
6	RXP
7	GND



HDMI Connectors
(Node A: CN73, CN74; Node B CN75, CN76)



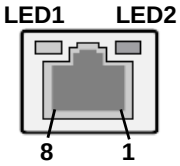
Pin #	Signal	Pin #	Signal
1	TMDS Data2+	2	TMDS Data2 Shield
3	TMDS Data2–	4	TMDS Data1+
5	TMDS Data1 Shield	6	TMDS Data1–
7	TMDS Data0+	8	TMDS Data0 Shield
9	TMDS Data0–	10	TMDS Clock+
11	TMDS Clock Shield	12	TMDS Clock–
13	CEC	14	Reserved
15	SCL	16	SDA
17	DDC/CEC Ground	18	+5 V Power
19	Hot Plug Detect		

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RJ-45 Gigabit Ethernet Connectors

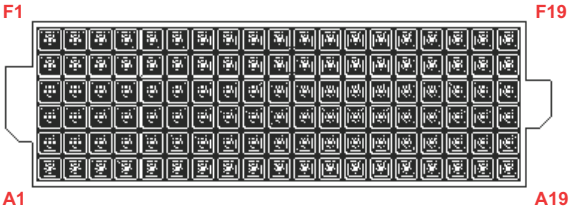
CN77 (Slot 1 w/ iAMT), CN78 (Slot 2 w/ iAMT), CN79 (Slot 5, Node A w/ iAMT), CN80 (Slot 5, Node B w/iAMT), CN81 (Slot 5, Node A w/o iAMT), CN82 (Slot 5, Node B w/o iAMT)

Pin #	1000BASE-T
1	BI_DA+
2	BI_DA-
3	BI_DB+
4	BI_DC+
5	BI_DC-
6	BI_DB-
7	BI_DD+
8	BI_DD-



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XMC Connectors
(Node A only)

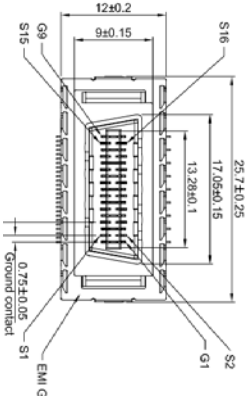


Pin	A	B	C	D	E	F
1	RXP0	RXN0	+3.3V	RXP1	RXN1	VPWR
2	GND	GND	TRST#	GND	GND	MRSTI#
3	RXP2	RXN2	+3.3V	RXP3	RXN3	VPWR
4	GND	GND	TCK	GND	GND	MRSTO#
5	RXP4	RXN4	+3.3V	RXP5	RXN5	VPWR
6	GND	GND	TMS	GND	GND	+12V
7	RXP6	RXN6	+3.3V	RXP7	RXN7	VPWR
8	GND	GND	TDI	GND	GND	-12V_AUX
9	NC	NC	NC	NC	NC	NC
10	GND	GND	TDO	GND	GND	GA0
11	TXP0	TXN0	MBIST#	TXP1	TXN1	VPWR
12	GND	GND	GA1	GND	GND	MPRSENT#
13	TXP2	TXN2	+3.3V_AUX	TXP3	TXN3	VPWR
14	GND	GND	GA2	GND	GND	DATA
15	TXP4	TXN4	NC	TXP5	TXN5	VPWR
16	GND	GND	MVMRO	GND	GND	CLK
17	TXP6	TXN6	NC	TXP7	TXN7	NC
18	GND	GND	NC	GND	GND	NC
19	CLK-P	CLK-N	NC	WAKE#	ROOT#	NC

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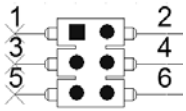
InfinBand Connectors
(Node A: CN90, CN91; Node B: CN92,CN93)

Pin	Signal	Pin	Signal
S1	RX0P	S14	TX1P
S2	RX0N	S15	TX0N
S3	RX1P	S16	TX0P
S4	RX1N	G1	GND
S5	RX2P	G2	GND
S6	RX2N	G3	GND
S7	RX3P	G4	GND
S8	RX3N	G5	GND
S9	TX3N	G6	GND
S10	TX3P	G7	GND
S11	TX2N	G8	GND
S12	TX2P	G9	GND
S13	TX1N		



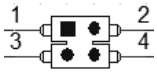
IDT Switch Hub I2C Connector (JP4)

Pin	Signal	Pin	Signal
S1	32NT8A_ SMB_CLK	S4	GND
S2	S5_32NT8A _MSMBCLK	S5	32NT8A_ SMB_DAT
S3	GND	S6	S5_32NT8A _MSMBDAT



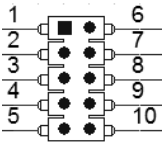
Speaker Out Connector (JP7)

Pin	Signal	Pin	Signal
1	Node A SPK OUT +	2	Node B SPK OUT +
3	Node A SPK OUT -	4	Node B SPK OUT -



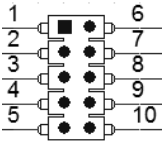
COM Connectors
(Node A: JP6; Node B: JP8)

Pin	Signal	Pin	Signal
1	COM1 RTS/TXP	6	COM2 RTS/TXP
2	COM1 TXD/TXN	7	COM2 TXD/TXN
3	COM1 RXD/RXN	8	COM2 RXD/RXN
4	COM1 CTS/RXP	9	COM2 CTS/RXP
5	GND	10	GND



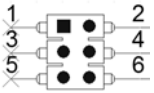
IPMC JTAG Connector (JP9)

Pin	Signal	Pin	Signal
1	TCK	6	GND
2	TKO	7	NC
3	TMS	8	P3V3
4	P3V3	9	TDO_CTRL
5	TDI	10	GND



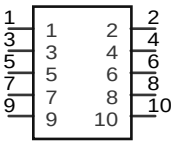
VPX JTAG Connector (JP11)

Pin	Signal	Pin	Signal
1	TDI	2	TCK
3	TDO	4	RST
5	TMS	6	GND



LPC Connectors
(Node A: CN87; Node B: CN88)

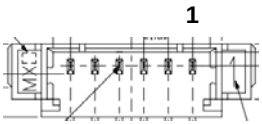
Pin	Signal	Pin	Signal
1	P3V3	2	GND
3	NC	4	LPC_AD3
5	PLTRST_LPC-L	6	LPC_AD2
7	CLK 33MHz	8	LPC_AD1
9	LPC_FRAME	10	LPC_AD0



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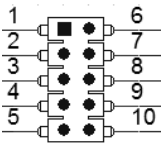
VPX SM Connectors
(SM01: CN94; SM23: CN95)

Pin	Signal
1	DATA
2	GND
3	CLOCK
4	P5V
5	ENABLE



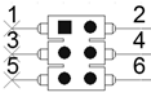
IPMC UART Connector (JP10)

Pin	Signal	Pin	Signal
1	NC	6	NC
2	TX	7	NC
3	RX	8	NC
4	NC	9	NC
5	GND	10	NC



Keyboard/Mouse Connectors
(Node A: CN85; Node B: CN86)

Pin	Signal	Pin	Signal
1	KB Data	2	KB Clock
3	MS Data	4	MS Clock
5	VCC	6	GND



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Power Terminals

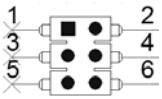
Pin	Signal
CN1	3.3 VDC
CN2	5 VDC
CN3	12 VDC
CN4	GND

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4.6 tBP-VPX6000 Switches and Jumpers

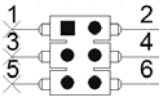
Clear CMOS & ATX PS_ON Jumper (JP1)

Shorted	Signal
1-3	Normal (default)
3-5	Clear CMOS
2-4	N/A
4-6	ATX PS_ON Low (default)



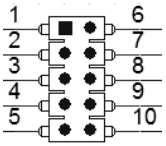
Non-Volatile Memory Read-Only (NVMRO) Jumper (JP2)

Shorted	Signal
2-4	NVMRO Normal (default)
4-6	NVMRO disabled



BIOS Select Jumper (JP5)

Pin	Signal	Pin	Signal
1	Node A Boot from RTM BIOS select	6	GND
2	Node B Boot from RTM BIOS select	7	GND
3	NA_BIOS_SEL1#	8	GND
4	NB_BIOS_SEL2#	9	GND
5	NC	10	NC



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Reset Buttons

- SW1: System Reset Button
- SW2: Maskable Reset Button
- SW3: Node A Reset Button
- SW4: Node B Reset Button

Power Buttons

- SW5: Node A Power Button
- SW6: Node B Power Button
- SW7: System Power Button

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5 Getting Started

This chapter describes the installation of the and VPX6000 blade and VPX-R6000 rear transition module.

5.1 Installing the VPX6000 to the Chassis

These instructions are for reference only. Refer to the user guide that comes with the chassis for more information.

1. Be sure to select the system slot to install the blade. The system power may be powered either on or off.
2. Align the module's top and bottom edges to the chassis card guides, and then carefully slide the module into the chassis. A slight resistance may be felt when inserting the module. If the resistance is too strong, check if there the wedge locks are tightened or if the board's connector pins are not properly aligned with connectors on the backplane. Then push the blade into the slot until it is completely flush with the chassis.
3. With the blade properly inserted, tighten the wedge locks to secure it to the chassis.

5.2 Installing the VPX-R6000 to the Chassis

The installation and removal procedures for a RTMs are the same as those for VPX blades. Because they are shorter than front boards, pay careful attention when inserting or removing RTMs.

Refer to previous sections for peripheral connectivity of all I/O ports on the RTM. When installing the VPX6000 Series and related RTMs, make sure the RTM is the correct matching model.

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5.3 Driver Installation

The VPX6000 drivers are available from the ADLINK website (**www.adlinktech.com**). ADLINK provides validated chipset, graphics and LAN drivers for Windows 7.

Follow the steps below to install the drivers for Windows 7 64-bit.

1. Install the **Windows operating system** before installing any driver. Most standard I/O device drivers are installed during Windows installation.
2. Install the **chipset driver** by extracting and running the program in **Intel Chipset Device Software_AllOS.zip**
3. Install the **1G LAN drivers** by extracting and running the program in **Intel 82580 Gigabit Network connection _Win7 64bit_12.7.28.0.zip**
4. Install the **10G LAN drivers** by extracting and running the program in **Mellanox 10 Gigabit Network connection_Win7 64bit_4.40.zip**
5. Install the **audio driver** by extracting and running the program in **Realtek_High Definition Audio_Win7_64 _6.0.1.7083.zip**
6. Install the **RAID Drivers** by extracting and running the program in **Intel Rapid Storage Technology_32bit and 64bit_12.5.0.1040.zip**
7. Install the **IME interface driver** by extracting and running the program in **Intel Management Engine Interface 9.0_5M_9.0.2.1345.zip**
8. Install the **USB 3.0 driver** by extracting and running the program in **Intel_USB_3.0_xHC_Driver_AllOS.zip**

We recommend using the drivers provided on the ADLINK website to ensure compatibility. VxWorks BSPs can aldo be downloaded from the VPX6000 product page.

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6 Utilities

6.1 Watchdog Timer

This section describes the operation of the VPX6000's watchdog timer (WDT). The primary function of the WDT is to monitor the VPX6000's operation and to reset the system if a software application fails to function as programmed. The following WDT functions may be controlled using a software application:

- enabling and disabling
- set and get current configuration
- reloading timeout value

The VPX6000 custom WDT circuit is implemented using the IPMC and operated by IPMI commands.

Watchdog Timer IPMI Commands

The following section describes the IPMI commands for controlling watchdog timer (WDT) functions. For more details about IPMI commands, please refer to the IPMI specification: "*Intelligent Platform Management Interface Specification Second Generation v2.0"* .

WDT Command Table

Command	NetFn Code	Cmd Code
Reset Watchdog Timer	App (18h)	22h
Set Watchdog Timer	App (18h)	24h
Get Watchdog Timer	App (18h)	25h

The WDT IPMI commands allow the user to set the countdown period and reload the timeout value periodically to keep it from resetting the system. If the timer countdown value is not reloaded, the watchdog resets the system hardware after its counter reaches zero.

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Reset Watchdog Timer

This command is used to reload the WDT.

Action	Byte	Value	Description
Request	0	18h	NetFn/LUN
	1	22h	Defined command
Response	0	Complete Code	00h means OK

Set Watchdog Timer:

This command is used to set the parameters of the WDT.

Action	Byte	Value	Description
Request	0	18h	NetFn/LUN
	1	24h	Defined command
	2	[7] - 1b = don't log [6] - 1b = don't stop timer [5:3] - reserved [2:0] - timer use 000b = reserved 001b = BIOS FRB2 010b = BIOS/POST 011b = OS Load 100b = SMS/OS 101b = OEM 110b -111b = reserved	Timer Use
	3	[7] - reserved [6:4] - pre-timeout interrupt 000b = none 001b = SMI (optional) 010b = NMI / Diagnostic Interrupt (optional) 011b = Messaging Interrupt 100b,111b = reserved [3] - reserved [2:0] - timeout action 000b = no action 001b = Hard Reset 010b = Power Down 011b = Power Cycle 100b,111b = reserved	Timer Actions

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Action	Byte	Value	Description
Request	4	1h~ffh (‘1h’ based.)	Pre-timeout interval in seconds.
	5	[7] - reserved [6] - reserved [5] - OEM [4] - SMS/OS [3] - OS Load [2] - BIOS/POST [1] - BIOS FRB2 [0] - reserved 0b = leave alone 1b = clear timer use expiration bit	Timer Use Expiration flags clear
	6	00h~ffh ,LS byte (100 ms/count)	Initial countdown value
	7	00h~ffh ,MS byte (100 ms/count)	Initial countdown value
Response	0	Complete Code	00h means OK

Get Watchdog Timer

This command is used to get the current configuration in WDT.

Action	Byte	Value	Description
Request	0	18h	NetFn/LUN
	1	25h	Defined command
Response	0	Complete Code	00h means OK
	1	[7] - 1b = don’t log [6] - 1b = don’t stop timer [5:3] - reserved [2:0] - timer use 000b = reserved 001b = BIOS FRB2 010b = BIOS/POST 011b = OS Load 100b = SMS/OS 101b = OEM 110b -111b = reserved	Timer Use

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Action	Byte	Value	Description
Response	2	[7] - reserved [6:4] - pre-timeout interrupt 000b = none 001b = SMI (optional) 010b = NMI / Diagnostic Interrupt (optional) 011b = Messaging Interrupt 100b,111b = reserved [3] - reserved [2:0] - timeout action 000b = no action 001b = Hard Reset 010b = Power Down 011b = Power Cycle 100b,111b = reserved	Timer Actions
	3	1h~ffh ('1h' based.)	Pre-timeout interval in seconds.
	4	[7] - reserved [6] - reserved [5] - OEM [4] - SMS/OS [3] - OS Load [2] - BIOS/POST [1] - BIOS FRB2 [0] - reserved 0b = leave alone 1b = clear timer use expiration bit	Timer Use Expiration flags clear
	5	00h~ffh ,LS byte (100 ms/count)	Initial countdown value
	6	00h~ffh ,MS byte (100 ms/count)	Initial countdown value
	7	00h~ffh ,LS byte (100 ms/count)	Present countdown value
	8	00h~ffh ,MS byte (100 ms/count)	Present countdown value

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Example of WDT Process

The sample program written in C shown below offers an interactive way to test the Watchdog Timer under DOS.

Configure WDT Parameters

```
0x40 : Don't stop timer.
0x01 : Hard Reset.
0x01 : Pre-timeout interval in 1 second.
0x08 : Timer Use Expiration flags clear by OS Load.
0x50 : 80 count. 100ms * 80 = 8000ms = 8 seconds.

[18 00 24 40 01 01 08 50 00]
```

Reset WDT

```
[18 00 22]
```


NOTE:

After setting a new configuration, the Reset WDT command must be sent. Then the WDT will be activated.

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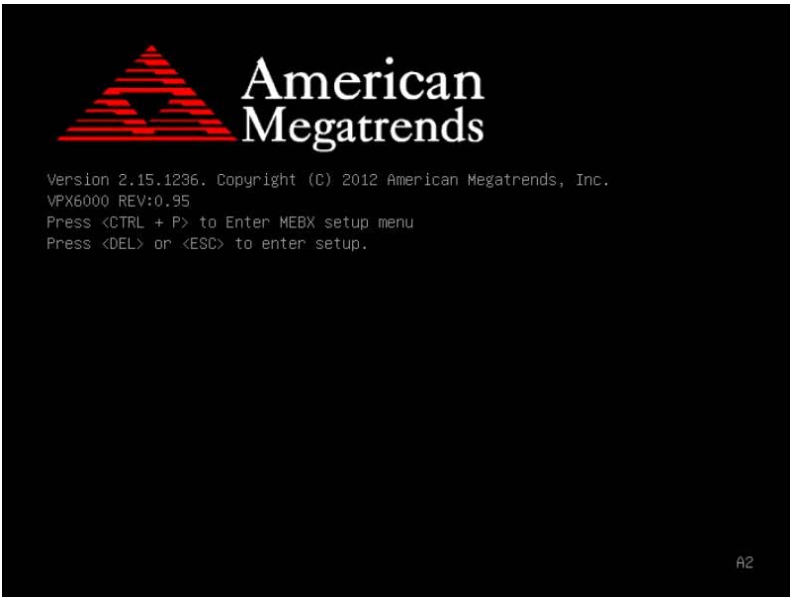
7 BIOS Setup

The following chapter describes basic navigation for the AMI EFI BIOS setup utility.

7.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:
   < Press DEL to run Setup >
3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu.



Note: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

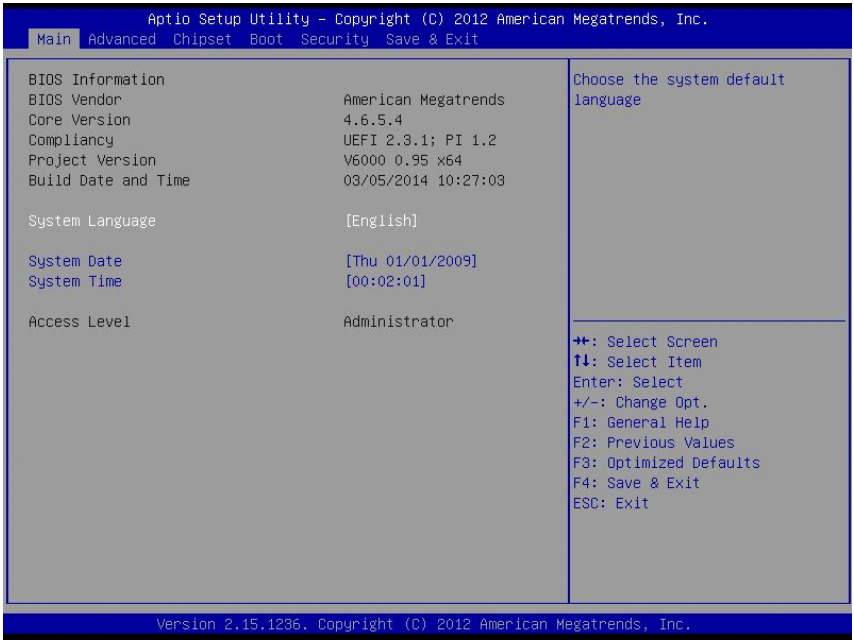
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Setup Menu

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

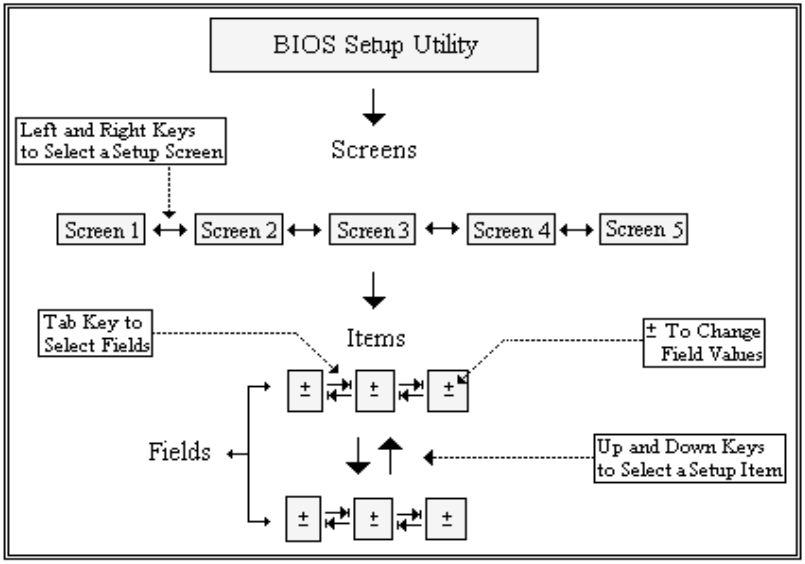
The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.



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Navigation



NOTE: There is a hot key legend located in the right frame on most setup screens.

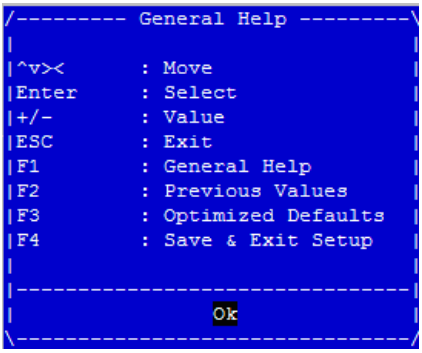
The < F8 > key on your keyboard is the Fail-Safe key. It is not displayed on the key legend by default. To set the Fail-Safe settings of the BIOS, press the < F8 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

Hotkey Descriptions

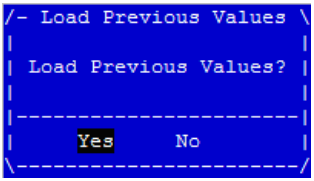
Enter The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

F1 The < F1 > key allows you to display the General Help screen. Press the < F1 > key to open the General Help screen.

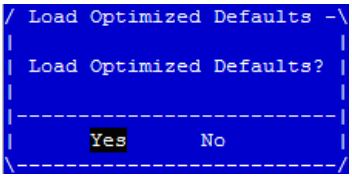
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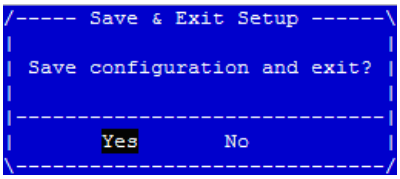
F2 The < F2 > key on your keyboard is the previous values key. It is not displayed on the key legend by default. To set the previous values settings of the BIOS, press the < F2 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The previous values settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.



F3 The < F3 > key on your keyboard is the optimized defaults key. To set the optimized defaults settings of the BIOS, press the < F3 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The optimized defaults settings allow the motherboard to boot up with the optimized defaults of options set. This can lessen the probability of conflicting settings.

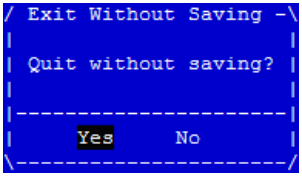


F4 The < F4 > key allows you to save any changes you have made and exit Setup. Press the < F10 > key to save your changes. The following screen will appear:



Press the < Enter > key to save the configuration and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

ESC The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. The following screen will appear:

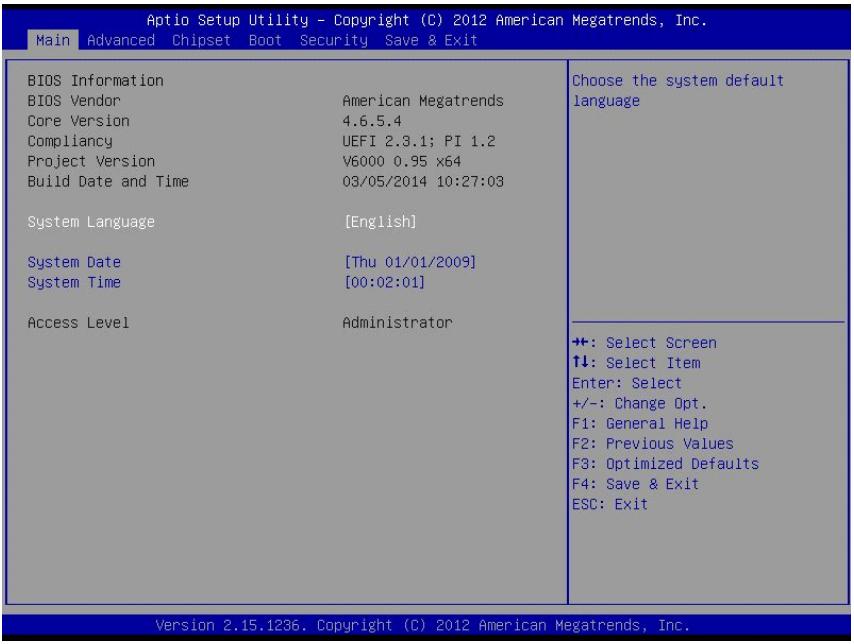


Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

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7.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



System Date/Time

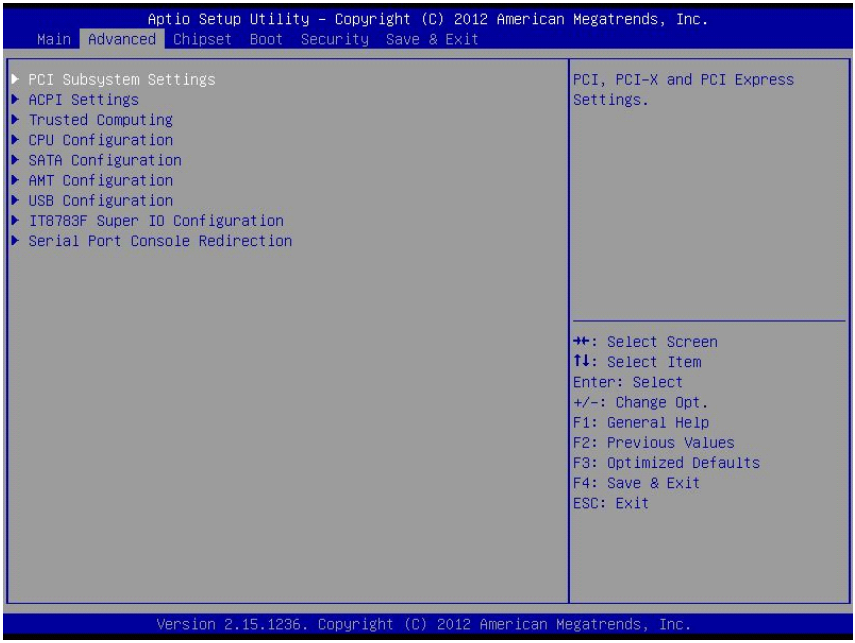
Use this option to change the system time and date. Highlight System Time or System Date using the < Arrow > keys. Enter new values using the keyboard. Press the < Tab > key or the < Arrow > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

Note: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

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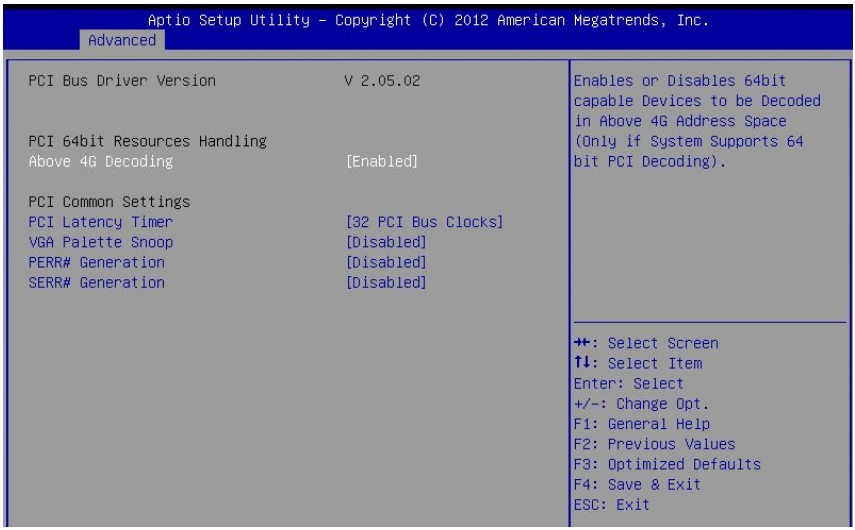
7.3 Advanced BIOS Setup

Select the Advanced tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. The Advanced BIOS Setup screen is shown below.



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7.3.1 PCI Subsystem Settings



Above 4G Decoding

This option allows 64-bit capable devices to be decoded in above 4G address space. Set this value to Enabled/Disabled.

PCI Latency Timer

Value to be programmed into PCI Latency Timer Register. Options: 32 PCI Bus Clocks, 64 PCI Bus Clocks, 96 PCI Bus Clocks, 128 PCI Bus Clocks, 160 PCI Bus Clocks, 192 PCI Bus Clocks, 224 PCI Bus Clocks, 248 PCI Bus Clocks.

VGA Palette Snoop

Enables or Disables VGA Palette Registers Snooping. Set this value to Disable/Enable.

PERR# Generation

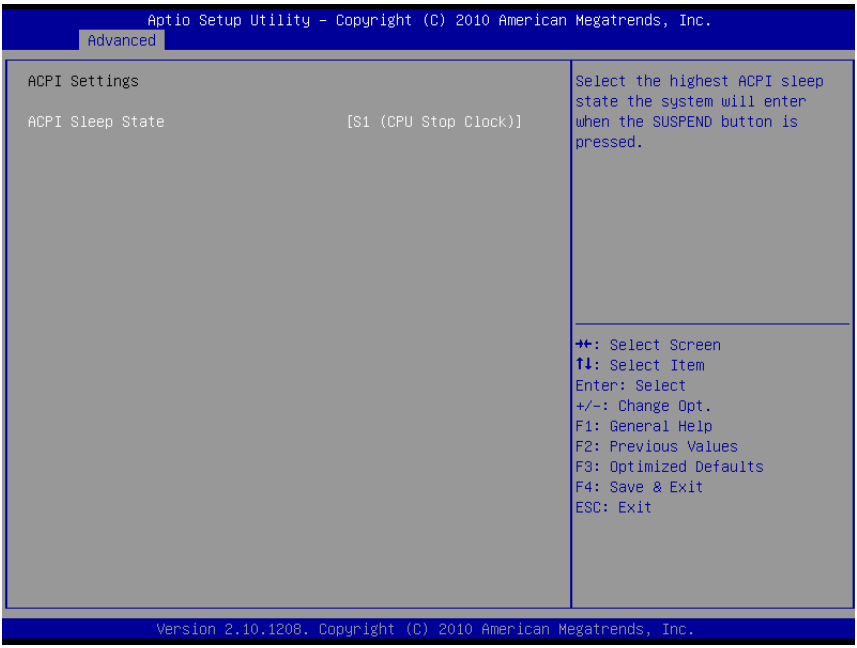
Enables or Disables PCI Device to Generate PERR#. Set this value to Disable/Enable.

SERR# Generation

Enables or Disables PCI Device to Generate SERR#. Set this value to Disable/Enable.

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7.3.2 ACPI Settings



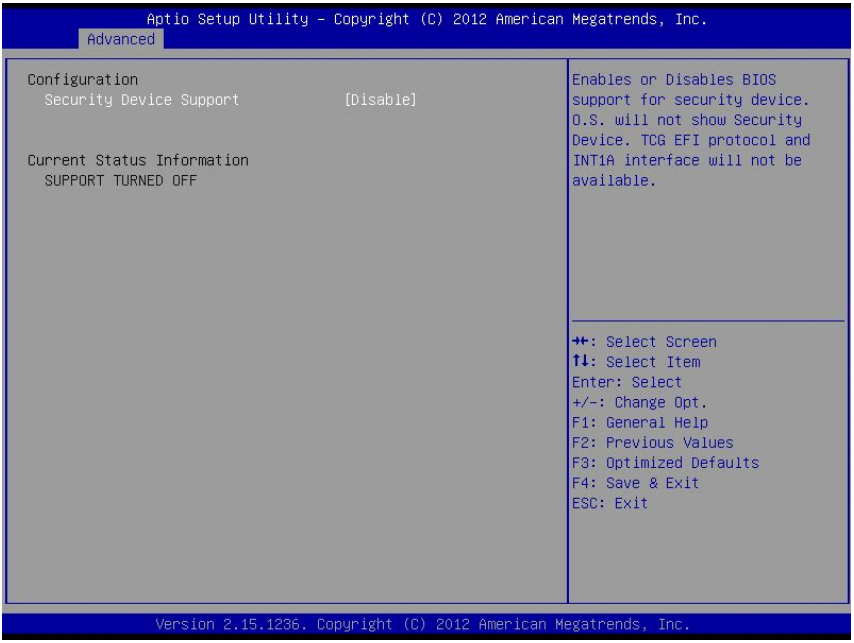
ACPI Sleep State

Select the highest ACPI sleep state the system will enter, when the Suspend button is pressed. Options: S1(CPU Stop Clock), Suspend Disable.

- **S1(CPU Stop Clock):** Power On Suspend - Under this setting the CPU is not executing instructions, all power resources that supply system level reference of S0 are off, system memory context is maintained, devices that reference power resources that are on, and devices that can wake-up the system can cause the CPU to continue to execute from where it left off.

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7.3.3 Trusted Computing



Security Device Support

Enables or disables BIOS support for security device. OS will not show security device. TCG EFI protocol and INT1A interface will be available.

TPM State

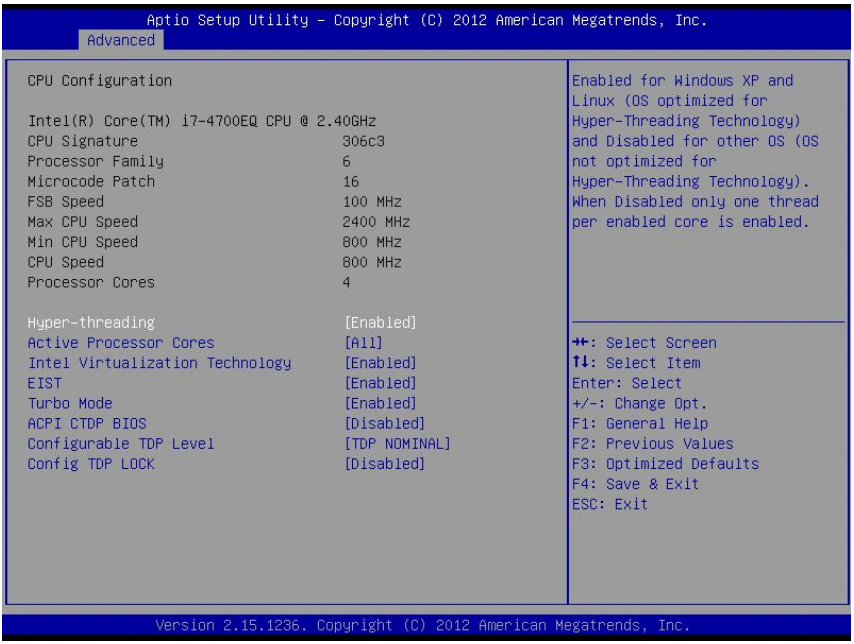
Enable/Disable security device.
Note: Your computer will reboot during restart in order to change state of the security device.

Pending Operation

Schedule an operation for the security device. Note: your computer will reboot during restart in order to change state of the security device.

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7.3.4 CPU Configuration



Hyper-Threading

Enables/disables Hyper-Threading Technology. Enable for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and disable for other OS (OS not optimized for Hyper-Threading Technology.

Active Processor Cores

Number of cores to enable in each processor package. Set this value to All / 1 / 2 / 3.

Intel Virtualization

Enables/disables Intel Virtualization Technology.

EIST

Enable Intel SpeedStep Technology support. Set this value to Enabled/Disabled.

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Turbo Mode

Enable Intel Turbo Boost support. Set this value to Enabled/Disabled.

ACPI CTDP BIOS

Enable ACPI CTDP BIOS support. Set this value to Enabled/Disabled.

Configurable TDP Level

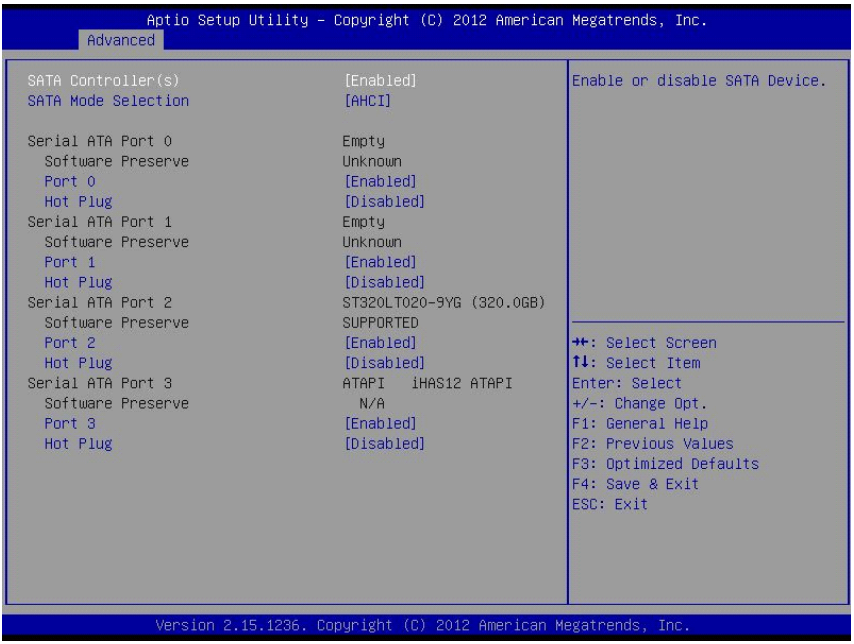
Configure TDP Level. Options: TPD NOMINAL, TDP DOWN, TDP UP, Disabled.

Config TDP LOCK

Enable to lock the configuration of the TDP control register. Set this value to Enabled/Disabled.

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7.3.5 SATA Configuration



SATA Controller(s)

This item enables/disables the SATA Controllers.

SATA Mode Selection

The SATA interface can be configured as legacy IDE, AHCI, or RAID mode.

SATA Port 0-3

Display SATA device name string.

Staggered Spin-up

Appears when SATA mode is set to AHCI. AHCI Support Staggered Spin-up. Set this value to Enable/Disable.

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External SATA Port

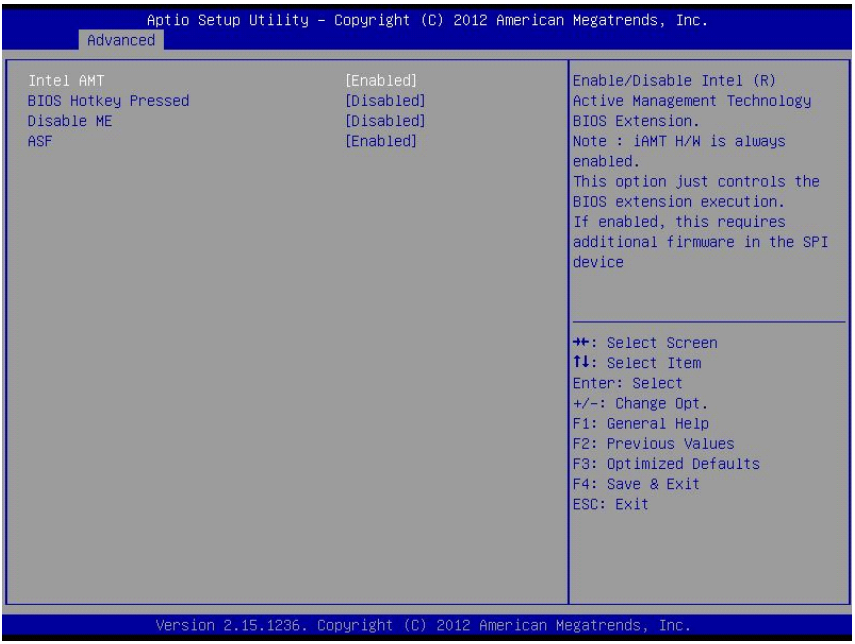
Appears when SATA mode is set to AHCI. eSATA Ports Support. Set this value to Enable/Disable.

Hot Plug

Appears when SATA mode is set to AHCI. SATA Ports Hot Plug support. Set this value to Enable/Disable.

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7.3.6 AMT Configuration



Intel AMT

Enable for Intel Active Management Technology BIOS Extension. Set this value to Enabled/Disabled.

BIOS Hotkey Pressed

Enable BIOS hotkeys. Set this value is Enabled/Disabled.

Disable ME

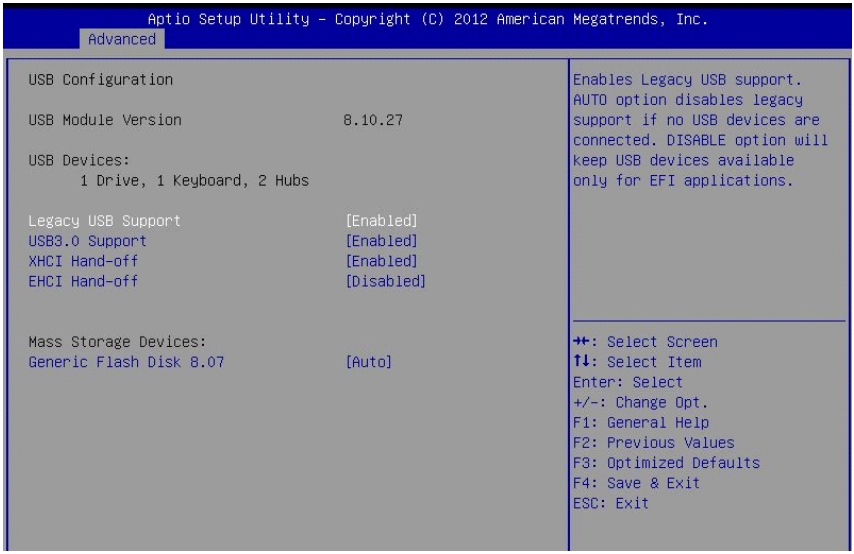
Set Management Engine to soft temporarily disabled. Set this value is Enabled/Disabled.

ASF

Enable Alert Specification Format. Set this value is Enabled/Disabled.

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7.3.7 USB Configuration



Legacy USB Support

Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications. Set this value to Enable/Disable/Auto.

USB 3.0 Support

Enable USB3.0 (XHCI) controller support. Set this value to Enabled/Disabled/Auto.

XHCI Hand-off

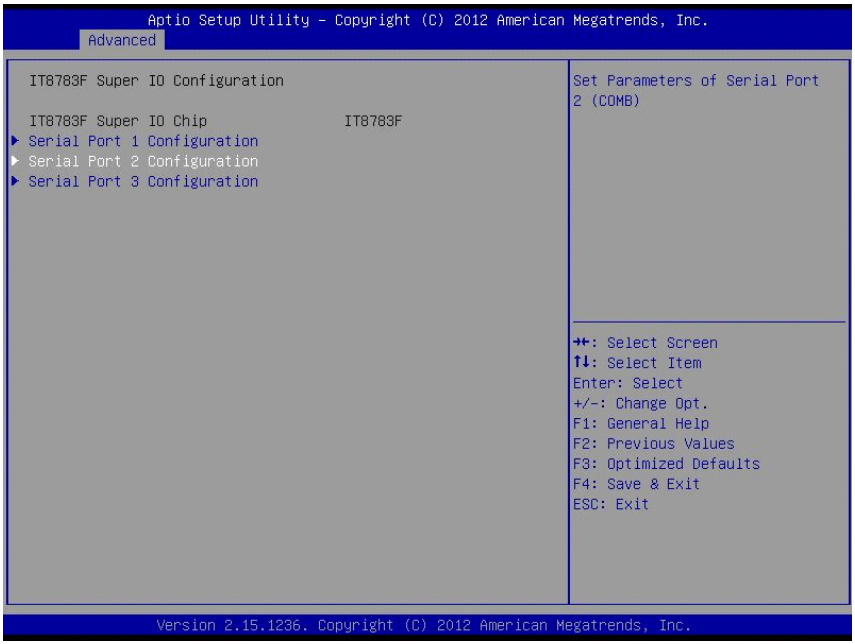
This is a workaround for OS without XHCI hand-off support. The XHCI ownership change should be claimed by the XHCI driver. Set this value to Enabled/Disabled.

EHCI Hand-off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by the EHCI driver. Options: Enable, Disable.

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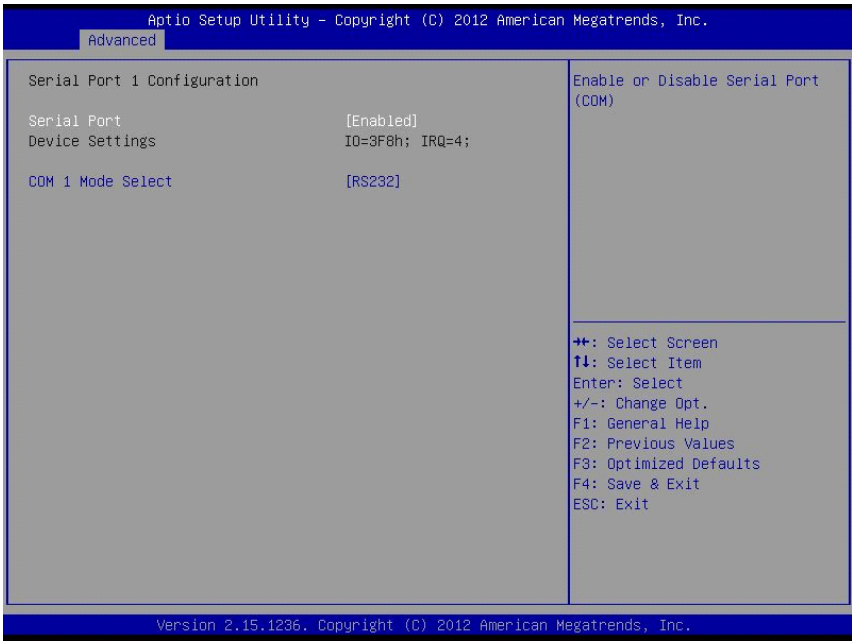
7.3.8 Super IO Configuration



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Serial Port 1-3 Configuration

Set Parameters of serial ports 1,2,3 (COM A,B,F).



Serial Port

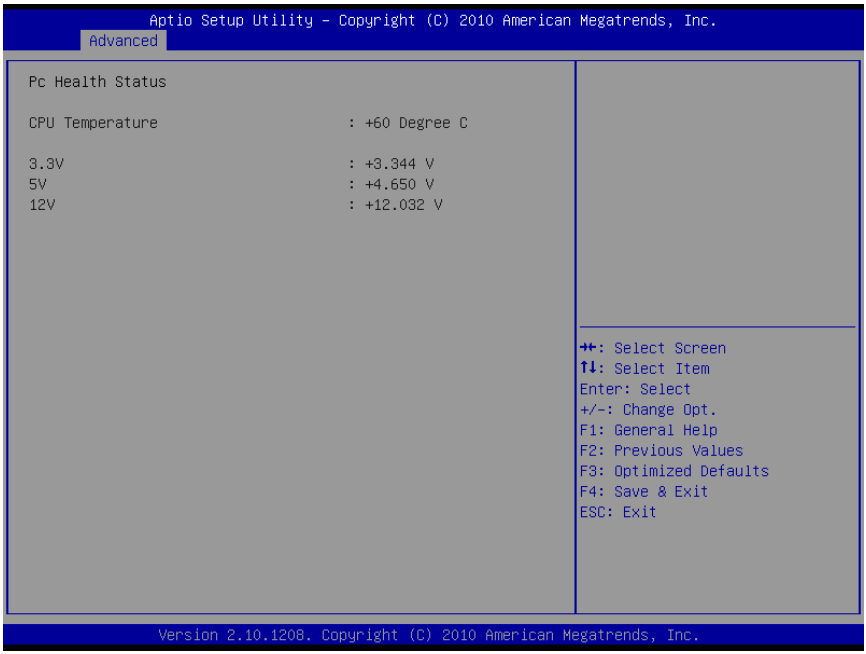
Select current COM port Disable or Enable of serial port 1,2,3 (COMA,B,F). Set this value to Enabled/Disabled.

COMx Mode Select

Select current COM port mode of serial port 1,2 (COMA,B). Set this value to RS232 or RS422.

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7.3.9 Hardware Monitor



CPU Temperature

Display current CPU temperature.

3.3V

Display current system 3.3V voltage.

5V

Display current system 5V voltage.

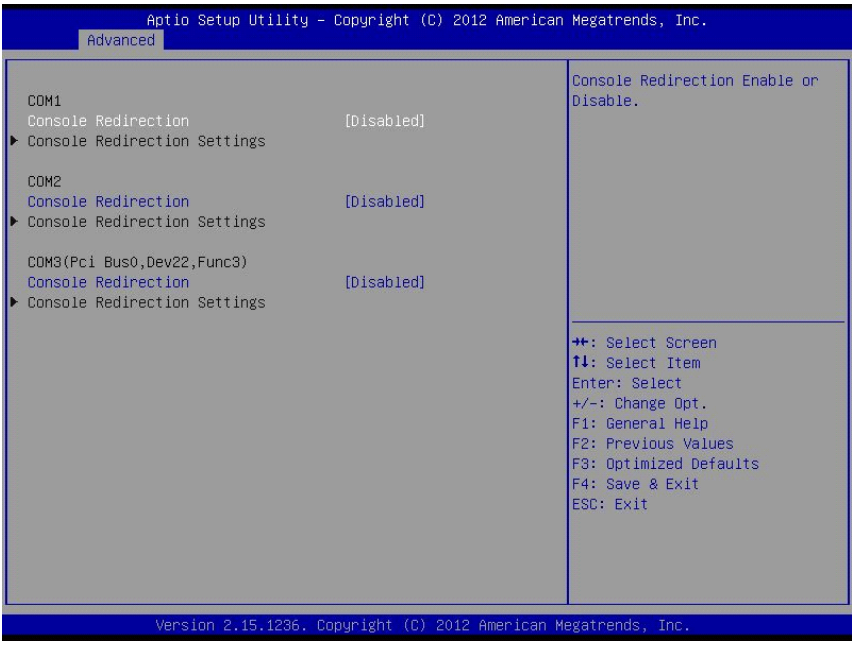
12V

Display current system 12V voltage.

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7.3.10 Serial Port Console Redirection

The settings specify how the host computer and the remote computer will exchange data. Both computers should have the same or compatible settings.



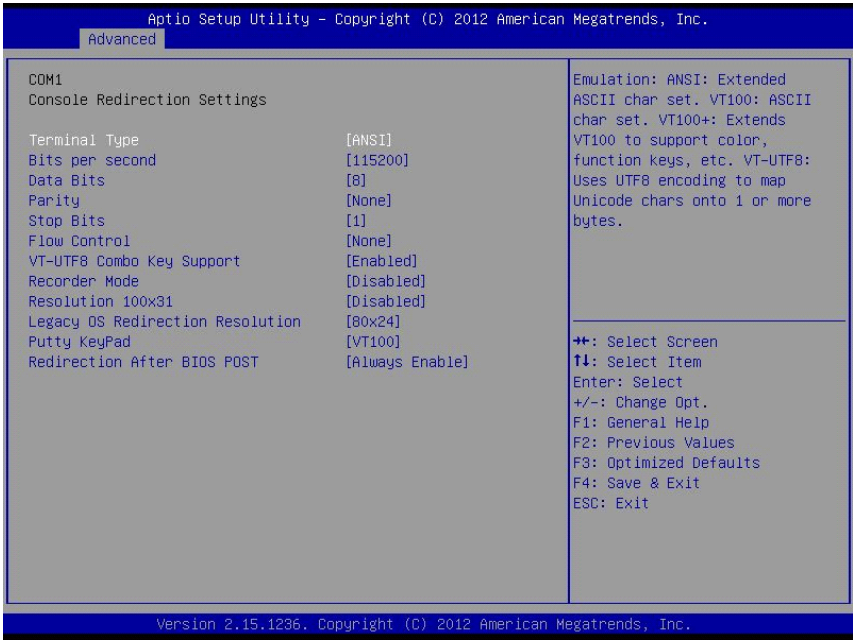
Console Redirection

Enable or disable Console Redirection.

Console Redirection Settings

The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings. The screen is shown below.

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Terminal Type

VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. Options: VT100, VT100+, VT-UTF8, ASNI.

Bits per Second

Select the bit rate (bits/second) you want the serial port to use for console redirection. Options: 115200, 57600, 19200, 9600.

Data Bits

Select the data bits you want the serial port to use for console redirection. Set this value to 7 or 8.

Parity

Set this option to select Parity for console redirection. The settings for this value are None, Even, Odd, Mark, Space.

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Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. Set this value to 1 or 2.

Flow Control

Set this option to select Flow Control for console redirection. The settings for this value are None and Hardware RTS/CTS.

VT-UTF8 Combo Key Support

Enable VT-UTF8 Combination Key support for ANSI/VT100 terminals. The settings for this value are Enabled, Disabled.

Recorder Mode

When enabled, only text will be sent. This is to capture terminal data.

Resolution 100x31

Enables or disables extended terminal resolution.

Legacy OS Redirection Resolution

In legacy OSes, the number of rows and columns supported by redirection. The settings for this value are: 80x24, 80x25.

Putty KeyPad

Select function key and keypad on putty. Options: VT100, LINUX, XTERMR6, SCO, ESCN, VT400.

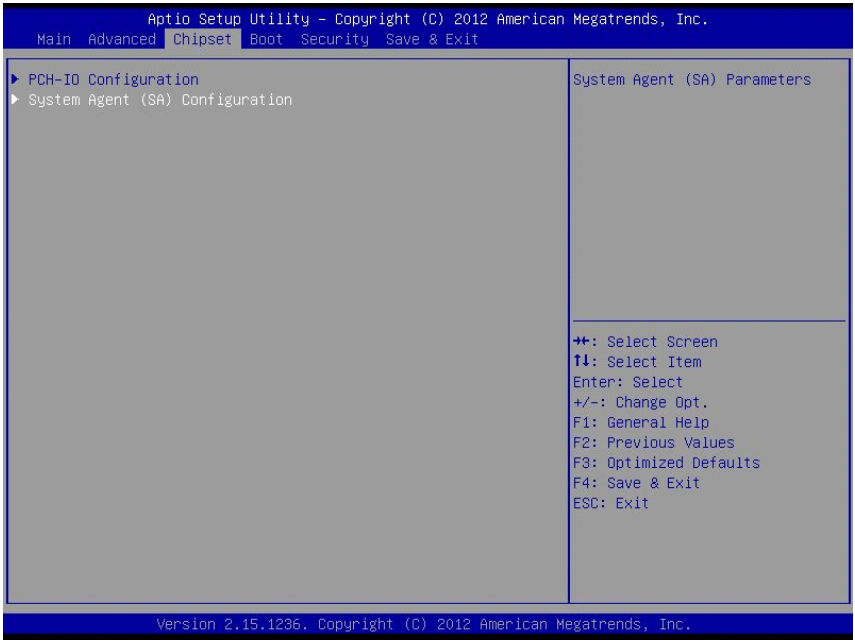
Redirection After BIOS POST

This option sets legacy console redirection. If BootLoader is selected, then legacy console redirection is disabled before booting to legacy OS. The default value is Always Enable (legacy console redirection enabled for legacy OS). Options: Always Enable, BootLoader.

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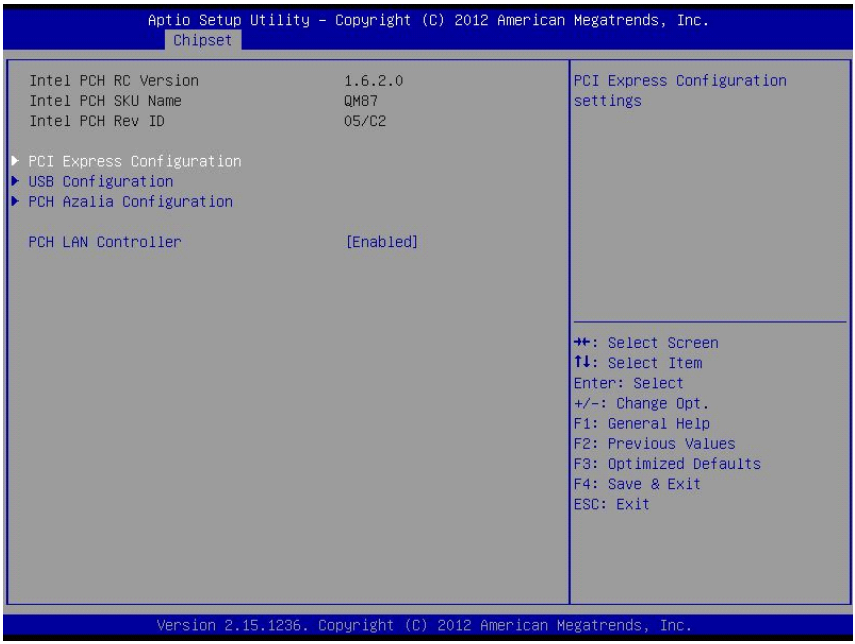
7.4 Chipset Configuration

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of Chipset BIOS Setup options by highlighting it using the < Arrow > keys. The Chipset BIOS Setup screen is shown below.



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7.4.1 PCH-IO Configuration



PCH LAN Controller

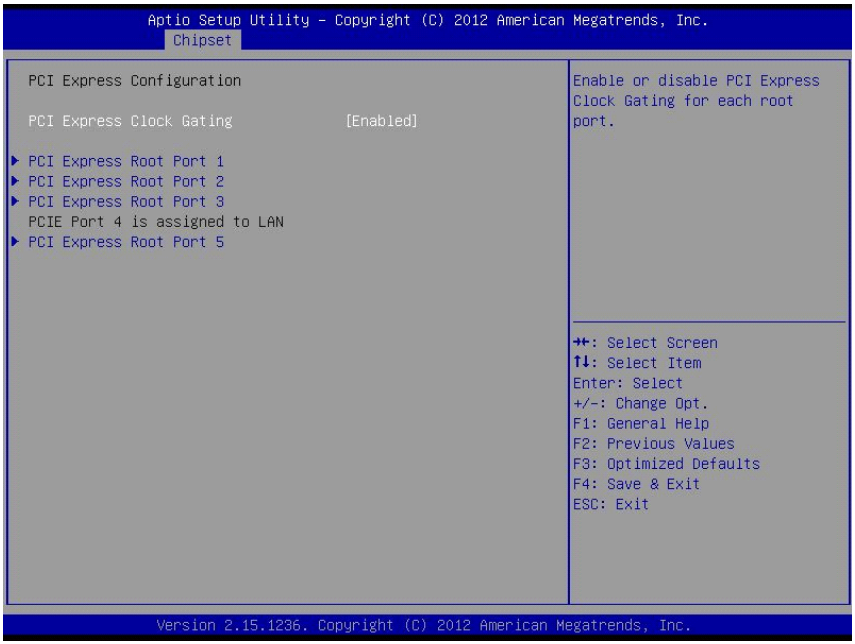
Enable or disable PCH LAN Controller. Set this value to Enable/Disable

PCH Azalia Configuration

Controls detection of Azalia device. Auto will enable the device if present. Options: Auto, Enable, Disable.

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PCI Express Configuration



PCI Express Clock Gating

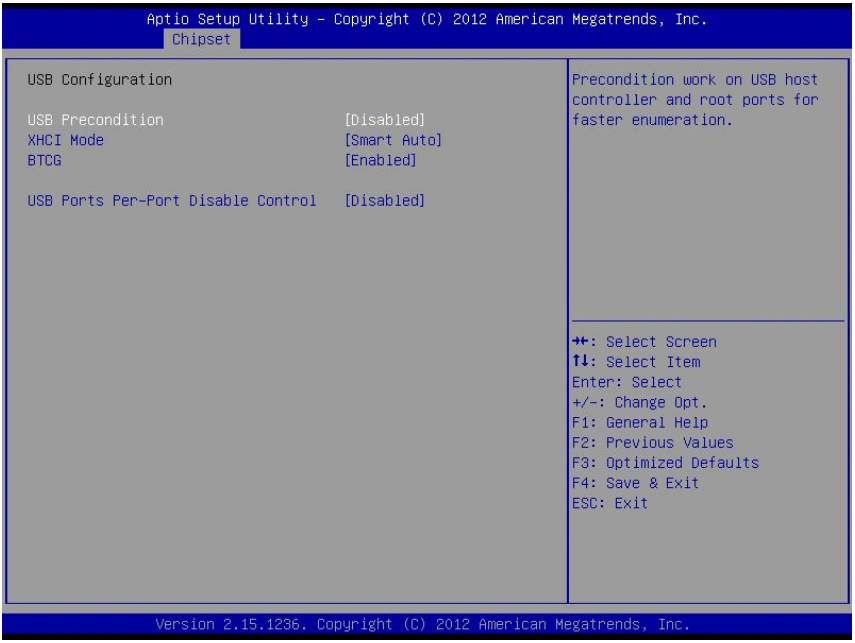
Enable or disable PCI Express Clock Gating for each root port. Set this value to Enable / Disable.

PCI Express Root Port 1,2,3,5

Control the PCI Express Root Ports 1,2,3,5.

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USB Configuration



USB Precondition

Enable precondition on USB host controller and root ports for faster enumeration. Set this value to Enabled/Disabled.

XHCI Mode

Select operating mode of xHCI controller. Options: Smart Auto, Auto, Enabled, Disabled, Manual.

BTCG

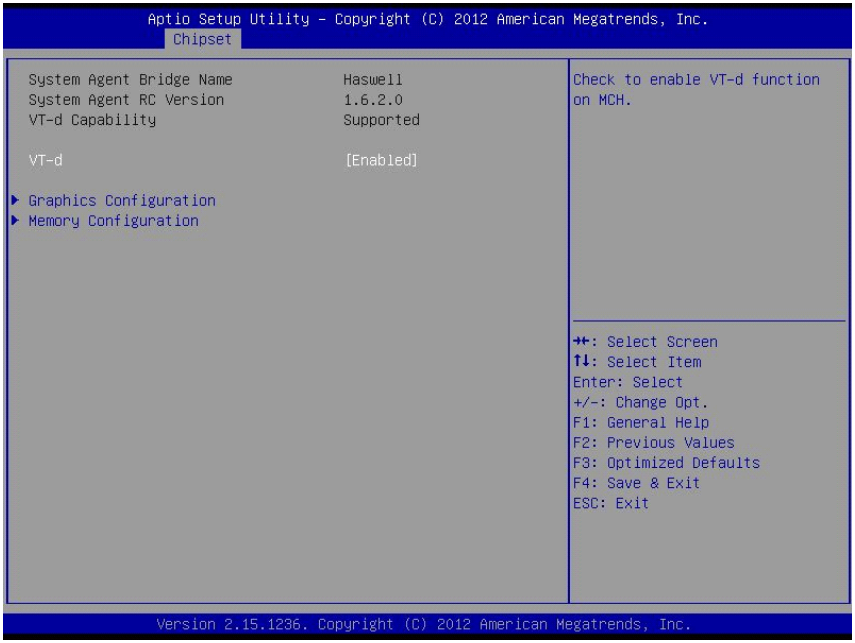
Enable or disable trunk clock gating. Set this value to Enabled/ Disabled.

USB Ports Per-Port Disable Control

Control disabling of each of the USB ports (0~13). Set this value to Enabled/Disabled.

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7.4.2 System Agent (SA) Configuration

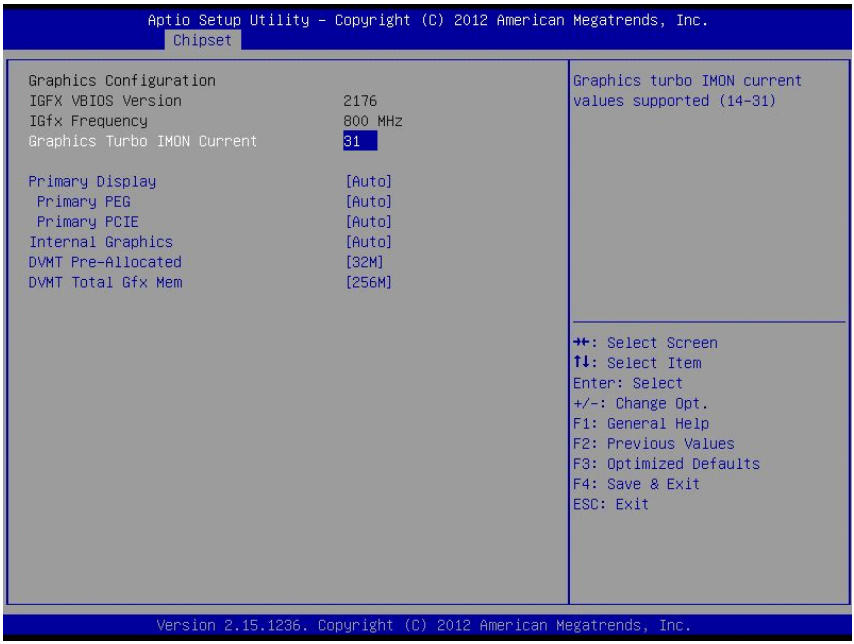


VT-d

Intel Virtualization Technology for Directed I/O. Set this value to Enable/Disable.

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Graphics Configuration



Graphics Turbo IMON Current

Set the value which graphics Turbo IMON supported (14~31).

Primary Display

Allows you to select which graphics controller to use as the primary boot device. Options: Auto, IGFX, PEG, PCIE.

Primary PEG

Select which PEG graphics device should be the primary PEG device. Set this value to Auto/ PEG11/ PEG12.

Primary PCIe

Select PCIe graphics device should be the primary PCIe device. Set this value to Auto/PCIE1/PCIE2/PCIE3/PCIE4/ PCIE5/PCIE6/PCIE7.

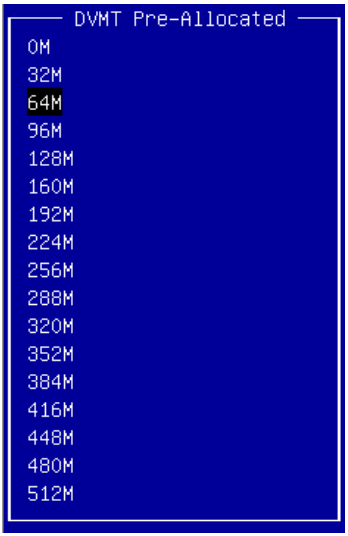
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Internal Graphics

Allows you to select enable/disable.the internal graphics. Options: Auto, Enabled or Disabled

DVMT Pre-Allocated

Select DVMT 5.0 Pre-Allocated (fixed) graphics memory size used by the internal graphics device. Configuration options are shown in the screen below.

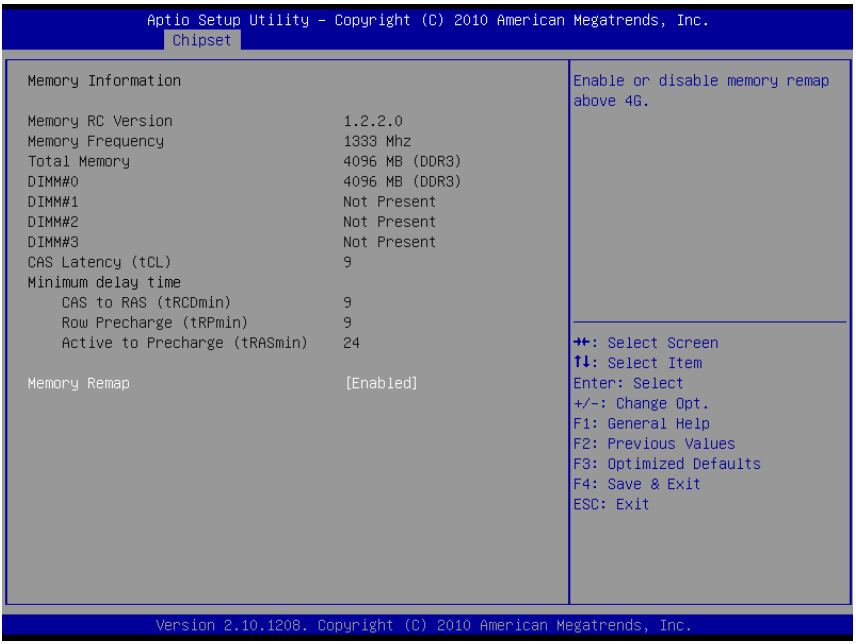


DVMT Total Gfx Memory

Select DVMT 5.0 total graphic memory size used by the internal graphics device. Configuration options are shown in the screen below.



Memory Information



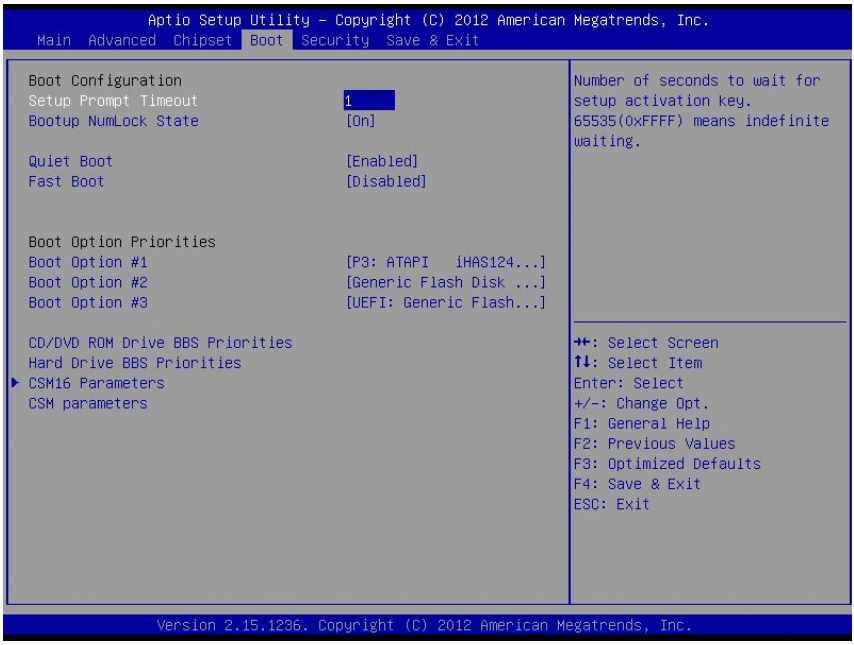
Memory Remap

Enable or disable memory remap above 4G. Set this value to Enable/Disable.

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7.5 Boot Configuration

Select the Boot tab from the setup screen to enter the Boot Configuration screen. You can select any of the items in the left frame of the screen to go to the sub menu for that item. You can display a Boot Configuration option by highlighting it using the < Arrow > keys. The Boot Configuration screen is shown below:



Setup Prompt Timeout

Set number of seconds the system waits for the setup activation key. Selecting 65535 (0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state. Set this value to On/Off.

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Quiet Boot

When this feature is **enabled**, the BIOS will hide normal POST messages during the boot-up sequence. When it is **disabled**, the BIOS will display the normal POST messages.

Fast Boot

Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options. Set this value to Enable / Disable.

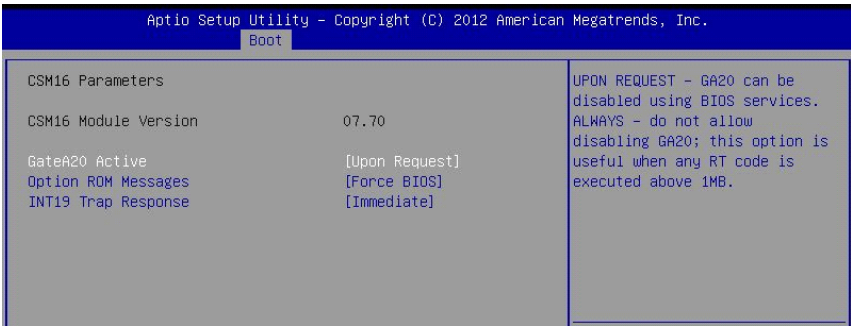
Set Boot Priority

Set Boot Option #1 to #3 boot priority.

Hard Disk Drive BBS Priorities

Specifies the boot device priority sequence from available hard drives.

CSM16 Parameters



GateA20 Active

This option is useful when any RT code is executed above 1MB. Options: Upon Request, Always.

Option ROM Message

Sets option ROM message display mode. Options: Force BIOS, Keep Current.

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INT19 Trap Response

Sets the BIOS reaction on INT19 trapping by option ROM. Options: Immediate, Postponed.

CSM Parameters



Launch CSM

This option controls if CSM will be launched. Set this value to Enabled/Disabled.

Boot Option Filter

This option controls which devices can boot the system. Options: UEFI and Legacy, Legacy only, UEFI only.

Launch PXE OpROM Policy

This option controls the execution of UEFI and Legacy PXE option ROM. Options: Do not launch, UEFI only, Legacy only.

Launch Storage OpROM Policy

This option controls the execution of UEFI and Legacy Storage option ROM. Options: Do not launch, UEFI only, Legacy only.

Launch Video OpROM Policy

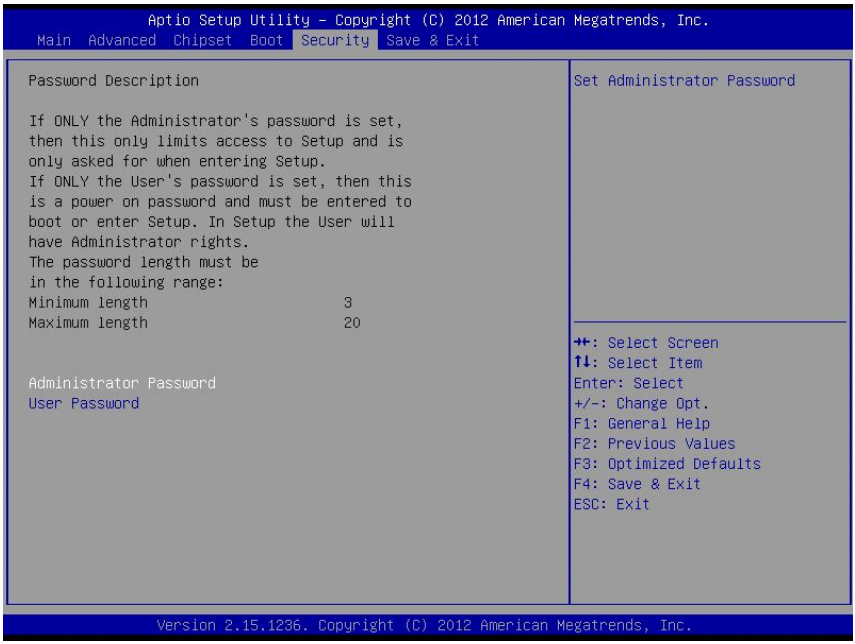
This option controls the execution of UEFI and Legacy Video option ROM. Options: Do not launch, UEFI only, Legacy only.

Other PCI Device ROM Priority

For PCI devices other than network, mass storage and video, the option determines if the PCI option ROM can be launched. Options: UEFI OpROM, Legacy OpROM.

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7.6 Security Setup



Administrator Password

Use this option to set a password for administrators with full control of the BIOS setup utility.

User Password

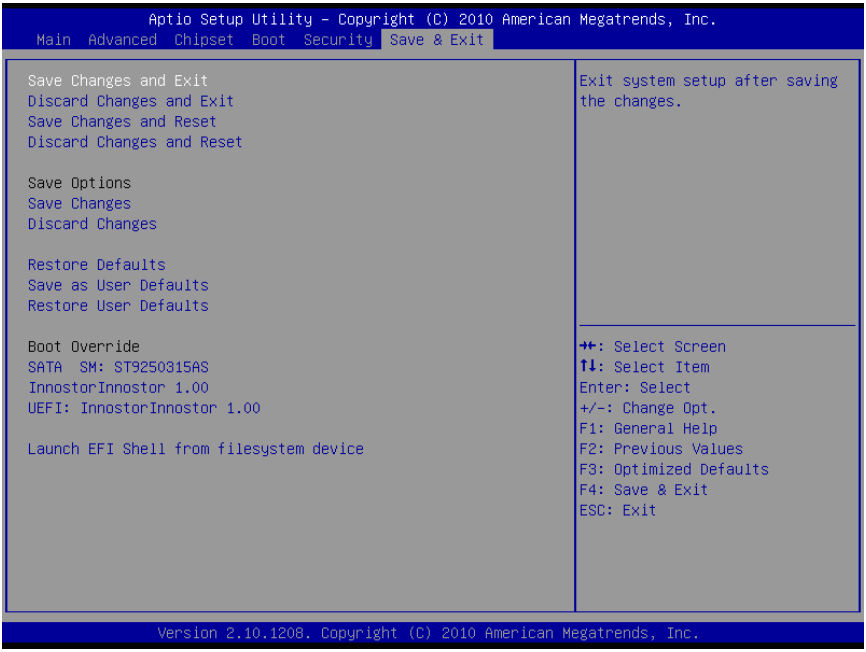
Use this option to set a password for users with limited access to the BIOS setup utility.

If only the administrator's password is set, then this only limits access to setup and is only asked for when entering setup. If only the user's password is set, then this is a power on password and must be entered to boot or enter setup. In setup the user will have administrator rights.

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7.7 Save & Exit

Select the Save & Exit tab from the setup screen to enter the Save & Exit setup screen. You can display a Save & Exit BIOS setup option by highlighting it using the < Arrow > keys. The Save & Exit BIOS setup screen is shown below.



Save Changes and Exit

When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect.

Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration.

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Save Changes and Reset

Reset the system after saving the changes.

Discard Changes and Reset

Reset the system without saving any changes.

Save Changes

Save changes made so far to any of the setup options.

Discard Changes

Discard changes made so far to any of the setup options.

Restore Defaults

Restore/Load Defaults values for all the setup options.

Save as User Defaults

Save changes made so far as User Defaults.

Restore User Defaults

Restore the User Defaults to all setup options

Boot Override

Use the up/down arrow keys to highlight a boot device to immediately exit the BIOS Setup and boot from the selected device.

Launch EFI Shell from file system device

Attempts to Launch EFI Shell application (Shellx64.efi) from one of the available file system devices.

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8 Checkpoints

8.1 Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

8.2 Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading

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Status Code	Description
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization
SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not loaded

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-Memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)

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Status Code	Description
0x1C	Pre-memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other).
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)

Status Code	Description
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error.
0x55	Memory not installed
0x56	Invalid CPU type or Speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	reset PPI is not available
0x5C-0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is stared (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4-0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed

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Status Code	Description
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC-0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started

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Status Code	Description
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE Initialization (South Bridge module specific)
0x74	South Bridge DXE Initialization (South Bridge module specific)
0x75	South Bridge DXE Initialization (South Bridge module specific)
0x76	South Bridge DXE Initialization (South Bridge module specific)
0x77	South Bridge DXE Initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect

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Status Code	Description
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E – 0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)

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Status Code	Description
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

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ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

8.3 OEM-Reserved Checkpoint Ranges

Status Code	Description
0x05	OEM SEC initialization before microcode loading
0x0A	OEM SEC initialization after microcode loading
0x1D – 0x2A	OEM pre-memory initialization codes
0x3F – 0x4E	OEM PEI post memory initialization codes
0x80 – 0x8F	OEM DXE initialization codes
0xC0 – 0xCF	OEM BDS initialization codes

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9 IPMI User Guide

9.1 Introduction

This chapter is written for those who already have a basic understanding of the newest implementation of the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI) specification rev. 2.0.

9.2 Summary of Commands Supported by VPX6000

The table below lists all the commands supported by the IPMC. The right most column indicates if a particular command is mandatory or optional for IPMI 2.0 and VITA 46.11.

Command Name	IPMI v2.0 Specification Section	NetFn	CMD
IPM Device "Global" Commands			
Reserved	NA	App (06h)	00h
Get Device ID	17.1	App (06h)	01h
Cold Reset	17.2	App (06h)	02h
Warm Reset	17.3	App (06h)	03h
Get Self Test Results	17.4	App (06h)	04h
BMC Watchdog Timer Commands			
Reset Watchdog Timer	21.5	App (06h)	22h
Set Watchdog Timer	21.6	App (06h)	24h
Get Watchdog Timer	21.7	App (06h)	25h
FRU Device Commands			
Get FRU Inventory Area Info	28.1	Storage (0Ah)	10h
Read FRU Data	28.2	Storage (0Ah)	11h
Write FRU Data	28.3	Storage (0Ah)	12h

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Command Name	IPMI v2.0 Specification Section	NetFn	CMD
SDR Device Commands			
Get SDR Repository Info	27.9	Storage (0Ah)	20h
Get SDR Repository Allocation Info	27.10	Storage (0Ah)	21h
Reserve SDR Repository	27.11	Storage (0Ah)	22h
Get SDR	27.12	Storage (0Ah)	23h
SEL Device Commands			
Get SEL Info	25.2	Storage (0Ah)	40h
Get SEL Allocation Info	25.3	Storage (0Ah)	41h
Reserve SEL	25.4	Storage (0Ah)	42h
Get SEL Entry	25.5	Storage (0Ah)	43h
Add SEL Entry	25.6	Storage (0Ah)	44h
Clear SEL	25.9	Storage (0Ah)	47h
Get SEL Time	25.10	Storage (0Ah)	48h
Set SEL Time	25.11	Storage (0Ah)	49h

Command Name	VITA 64.11 Specification Section	NetFn	CMD
VITA 46.11 Commands			
Get VSO Capabilities	VITA: section 10.1.3.1	VITA	00h
FRU Control	VITA: section 10.1.3.6	VITA	04h
Get FRU LED Properties	VITA: section 10.1.3.27	VITA	05h
Get LED Color Capabilities	VITA: section 10.1.3.28	VITA	06h

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Command Name	VITA 64.11 Specification Section	NetFn	CMD
Set FRU LED State	VITA: section 10.1.3.30	VITA	07h
Get FRU LED State	VITA: section 10.1.3.29	VITA	08h
Set IPMB State	VITA: section 10.1.3.7	VITA	09h
Set FRU State Policy Bits	VITA: section 10.1.3.9	VITA	0Ah
Get FRU State Policy Bits	VITA: section 10.1.3.8	VITA	0Bh
Set FRU Activation	VITA: section 10.1.3.10	VITA	0Ch
Get Device Locator Record ID	VITA: section 10.1.3.11	VITA	0Dh
Get Fan Speed Properties	VITA: section 10.1.3.12	VITA	14h
Set Fan Level	VITA: section 10.1.3.14	VITA	15h
Get Fan Level	VITA: section 10.1.3.13	VITA	16h
Get IPMB Link Info	VITA: section 10.1.3.17	VITA	18h

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9.3 Communications with IPMC

The VPX6000 communicates with the Chassis Manager through its primary IPMB (System IPMB) and responds to all mandatory commands for respective IPM Controllers (as defined in the VITA 46.11 Specification), as well as some optional ones.

9.4 IPMI Sensors List

Sensors include the mandatory sensors defined by VITA 46.11.

Sensor Number	Sensor name	Normal Reading	Sensor Reading Value of IPMI Get Sensor Reading Command
0	BMC Watchdog	N/A	6Fh (sensor-specific) Timeout action: 000b = no action 001b = Hard Reset 000b = Power Down 011b = Power Cycle 100b - 111b = reserved
1	NA_ADC_P12V	12 V	Threshold Value
2	NA_ADC_P5V	5 V	Threshold Value
3	NA_ADC_P3V3_AUX	3.3 V	Threshold Value
4	NA_ADC_P3V3	3.3 V	Threshold Value
5	NA_ADC_P0V9	0.9 V	Threshold Value
6	NA_ADC_P1V0	1.0 V	Threshold Value
7	NA_ADC_P_VCORE	1.8 V	Threshold Value
8	NA_ADC_P1V05_PCH	1.05 V	Threshold Value
9	NA_ADC_P1V35	1.35 V	Threshold Value
10	NB_ADC_P_VCORE	1.8 V	Threshold Value
11	NB_ADC_P1V05_PCH	1.05 V	Threshold Value
12	NB_ADC_P1V35	1.35 V	Threshold Value
13	NB_ADC_P0V9	0.9 V	Threshold Value
14	NA CPU Core Temp	40 C	Threshold Value
15	NB CPU Core Temp	40 C	Threshold Value
16	NA System Temp	25 C	Threshold Value
17	NB System Temp	25 V	Threshold Value

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9.5 FRU Information

Board Info

Mfg Date/Time = xx/xx/xxxx

Manufacturer = ADLINK

Product Name = VPX-6XXX

Serial Number = PPSxxxxxxx

Part Number = xxxxxxxxxxxx

Product Info

Manufacturer = ADLINK

Product Name = VPX-6XXX

Part/Model Number = xxxxxxxxxxxxx

Product Version = Rev A1

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9.6 Relevant Documents

- ANSI/VITA 46.0-2007 American National Standard for VPX Baseline Standard. (2007).
- ANSI/VITA 46.11-2007 System Management on VPX Draft Revision 0.11. (Nov. 18, 2013).
- ANSI/VITA 46.11-2015 System Management on VPX Draft Revision r022. (Nov. 18, 2013).
- Cortex-M3 Devices Generic User Guide. Issue A. (Dec. 16, 2010).
- IPMI- Intelligent Platform Management Interface Specification Second Generation v2.0 Rev. 1.0. (2004, 2 12).
- IPMI Platform Management FRU Information Storage Definition V1.0 Rev1.1. (1999, 9 27).
- Microsemi PPS BMR-A2F-ATCA Software Architecture Technical Specification, Revision 1.2.0. (April 17, 2013).
- Microsemi SmartFusion Microcontroller subsystem User Guide, Revision 4. (July ,2014).
- Microsemi SmartFusion Programmable Analog User Guide, Revision Draft B. (Dec.,2009).
- Pigeon Point BMR-A2F-VPX Software Architecture Technical Specification. Revision1.2.1. (Jan. 17, 2014).
- PICMG 3.0, Revision 3.0, AdvancedTCA Base Specification. (March 24, 2008).
- The Definitive Guide to the ARM Cortex-M3 Second Edition. (2010).

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Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

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- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.



Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

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Getting Service

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